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Chemistry and Defects in Semiconductor Heterostructures

EDITORS

Mitsuo Kawabe
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Chemistry and Defects in Semiconductor Heterostructures

Symposium held April 24-27, 1989, San Diego, California, U.S.A.

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Preface

The Symposium on *Chemistry and Defects in Semiconductor Heterostructures* was held April 24-27, 1989, as part of the MRS Spring Meeting in San Diego, California. Most of the papers presented at the Symposium are contained in this book. The financial support for this Symposium was provided by the Air Force Office of Scientific Research, the Army Research Office, and Bell Communications Research, Inc.

The intention of the editors was to bring together an interdisciplinary and international group of researchers working on various aspects of semiconductor heterostructures so that we could all learn from each other. In particular, we hoped to forge new links between those who study chemical interactions at heterostructure interfaces and those who are concerned with the effects of interfacial defects on the electrical and optical properties of semiconductor structures. The fact that there must be some relationship between chemical reactivity and defect formation has long been recognized, but as yet there is no detailed understanding of the actual mechanisms involved.

Scientists studying either the causes or the effects of interfacial defects must appreciate all the issues and work closely with each other. Only through such collaboration can the formation of semiconductor interfaces be truly understood and, eventually, their properties controlled. If this Symposium and the resulting book have stimulated only a few such interactions, then we feel that our efforts have been successful.

We thank all those who attended the Symposium and the authors who presented the results of their recent investigations, thereby sparking many lively discussions during the sessions and throughout the meeting. We also thank the session chairs, reviewers, and most especially the MRS staff and program officials for their excellent organization of the Symposium, all of which have made this volume possible.

Mitsuo Kawabe
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PART I

Metal/Semiconductor
Heterostructures I

THERMODYNAMICS, KINETICS AND INTERFACE MORPHOLOGY OF REACTIONS BETWEEN METALS AND GaAs

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ABSTRACT

The chemical stability of interfaces between metals and GaAs was discussed in terms of reaction sequence and diffusion path concepts. The factors which determine interface morphology were also given. These general ideas can be applied to any interfacial reactions between two dissimilar materials.

1.0 Introduction

Essential to the designing of microelectronic devices is the need for connections between active elements and therefore the need for active contacts. The need for reliable, low-resistance, reproducible, and stable ohmic contacts and Schottky barriers is particularly great for III-V compound semiconductors such as GaAs and for solid solutions of III-V compound semiconductors. In addition to exhibiting the appropriate electrical properties, a successful contact needs to be chemically stable. However, the chemical stability and hence the electrical properties of a contact are governed by the thermodynamics, kinetics and interface morphology of phase formation between the metalizing elements and the compound semiconductors.

During the past few years, a large number of experimental results have been reported in the literature concerning the metallization of III-V compound semiconductors, primarily GaAs. These studies have included the identification of the phases formed and to some extent the resulting morphologies when M/GaAs contacts were exposed to specific environments. Frequently, due to the paucity of relevant phase equilibria, thermodynamic, and kinetic data for ternary Ga-M-As systems, a rationalization of these results (some of which appear to be contradictory) has been difficult, if not impossible. The recent studies by us¹⁻¹⁵, Williams and co-workers¹⁶⁻²⁰, Beyers, Kim and Sinclair²¹, and Sands^{22,23} have demonstrated the importance of phase diagrams in the understanding of interfacial reactions between thin-film metals and GaAs. In addition, the concept of diffusion path in ternaries has been introduced by us^{1,5-7,9,10,13,15} to rationalize the phase formation in M/GaAs contacts. The factors which determine phase formation sequences and phase morphologies in terms of thermodynamic and kinetic view points have also been discussed by us.⁵ These ideas have been applied to M/GaAs diffusion couples in both the bulk and thin-film forms. We have found that the reaction sequences and diffusion paths for all M/GaAs couples investigated to-date are similar for the bulk and thin-film cases.

2.0 Interfacial Stability

2.1 Thermodynamic Considerations

It is well-known by now that most metals are not chemically compatible with GaAs.^{1,3,10,21,22,24} Figure 1 shows three typical phase diagrams of Ga-M-As when M is not in thermodynamic equilibrium with GaAs and when the only stable binary phases are Ga₃M, GaM, GaM₃, MAs, M₂As₃ and GaAs. The diagram in Fig. 1(a) depicts the case when the binary phases exhibits limited solubilities of the third component elements. The diagram in Fig. 1(b) depicts the case when the binary phase MAs dissolves a considerable amount of the counter phase "GaM". The symbol "GaM" denotes the unstable

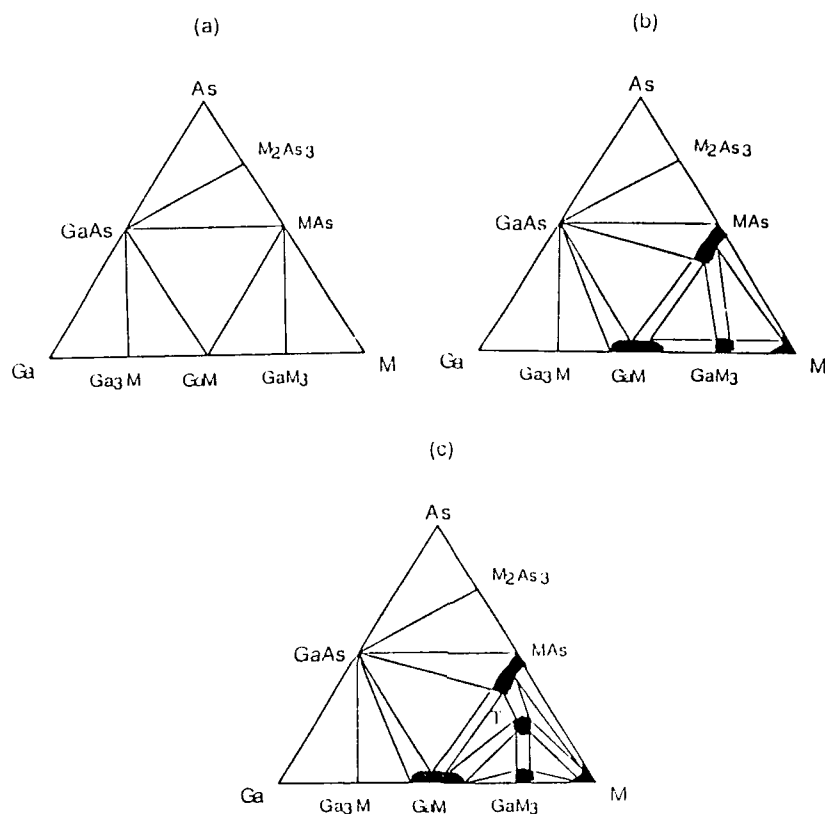


Figure 1.

Three possible phase diagrams of Ga-M-As at constant T and P.

- a. There are no mutual solubilities in any of the binary phases.
- b. There is extensive solubility of Ga in MAs.
- c. There is a ternary phase T along the GaAs-M join.

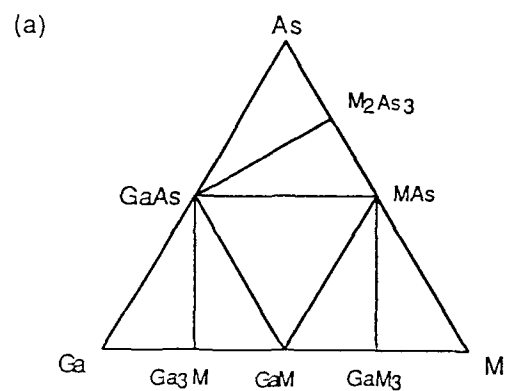
phase GaM which exhibits the MAS structure. The diagram in Fig. 1(c) depicts a case where, in addition to extensive solubilities of MAS, GaM, GaM₃ and (M), there exists a ternary phase T with a composition lying along the GaAs-M join. The appearances of the three types of phase diagrams depend upon the relative stabilities of the competitive phases, i.e. Ga₃M, GaM, GaM₃, MAS, M₂As₃, GaAs and T, the lattice stabilities of the component elements and the intermediate phases, and the thermodynamic solution behaviors of the solution phases. In order to be able to accurately calculate the phase diagrams of Ga-As-M, it is necessary to know the Gibbs free energies of the phases and the solution behaviors of the phases with extensive solubilities. Since most of the data are not available, accurate phase diagram determination is necessary. Several ternary Ga-M-As systems in the composition range of relevance to the metallization of GaAs have been determined by us. It is evident from Fig. 1 that in all three cases, the M/GaAs contacts will undergo chemical reactions when subjected to sufficiently high temperatures. In some cases, a sufficiently high temperature may be only 100°C or even lower. However, in view of the many types of phase equilibria exhibited by Ga-M-As, the kinetics of the reactions for the M/GaAs couples are quite different, as will be discussed in the next section.

2.2 Kinetic Considerations

2.2.1 Diffusion Paths

Thermodynamics tells us what will happen when equilibrium conditions are achieved but does not tell us what combinations of phases may form under actual conditions. For instance, we cannot tell what phases will form when M is in contact with GaAs from the phase diagram given in Fig. 1(a). While only one path is possible in a binary couple, this is not true for a ternary couple. When M is in contact with Ga for a binary Ga-M shown in Fig. 1, the three intermediate phases Ga₃M, GaM and GaM₃ will form, the only possible diffusion path. On the other hand, when M is in contact with GaAs, there is more than one possible path. Figure 1(a) is reproduced as Fig. 2(a) with two possible paths given in Fig. 2(b,c). When M is in contact with GaAs, several phases may form, such as GaM, GaM₃ and MAS. According to Kirkaldy and Brown³⁷, given a specific ternary diffusion couple there is only one diffusion path. Recent experimental studies by van Loo and co-workers⁴³⁻⁴⁶ on oxide/metal systems, Leute⁴⁷ on pseudo-ternary compound semiconductor/compound semiconductor systems, and by us^{1,5-8,10,15} on GaAs/M systems yield results in accordance with this statement. Although it is possible in principle to calculate the diffusion path, it is practically impossible given the current state of our understanding of ternaries such as Ga-M-As. We must depend upon experiments to determine the diffusion paths of GaAs/M couples. If the diffusion path is that given as path I (Fig. 2(b)), MAS would be in contact with GaAs; on the other hand, if path II (Fig. 2(c)) is the diffusion path, GaM would be in contact with GaAs. From a device point of view, it is important to know which of these phases is in contact with GaAs under equilibrium conditions.

Because microelectronic devices are made in the form of thin-films, it is equally important to study the kinetics of thin-film phase formation on GaAs. Let us now refer to Fig. 1(a) or 2(a) for discussion. When a thin-film metal M is deposited on GaAs, the final equilibrium mixture will be GaAs, GaM and MAS. If the diffusion path is that of path I, we will have the final configuration of GaAs|MAS|GaM. On the other hand, if path II is the diffusion path, the final configuration of thin-metal film deposited on GaAs would be GaAs|GaM|MAS. Although there are indications that the results obtained from some bulk and thin-film M/Si binary couples may not be the same²⁵⁻³⁰, the results of our studies on GaAs/M couples are similar for both the bulk and thin-film cases.^{1,5-8,10,15} If discrepancies between the bulk and thin-film studies do occur, additional investigation will be carried out



(b) Path I

GaAs	MAs	GaM	GaM ₃	M
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(c) Path II

GaAs	GaM	MAs	M
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Figure 2. a. A hypothetical Ga-M-As ternary isothermal section.
 b. A possible diffusion path for a couple of GaAs/M.
 c. Another possible diffusion path for a couple of GaAs/M.

to ascertain whether they are intrinsic in nature.

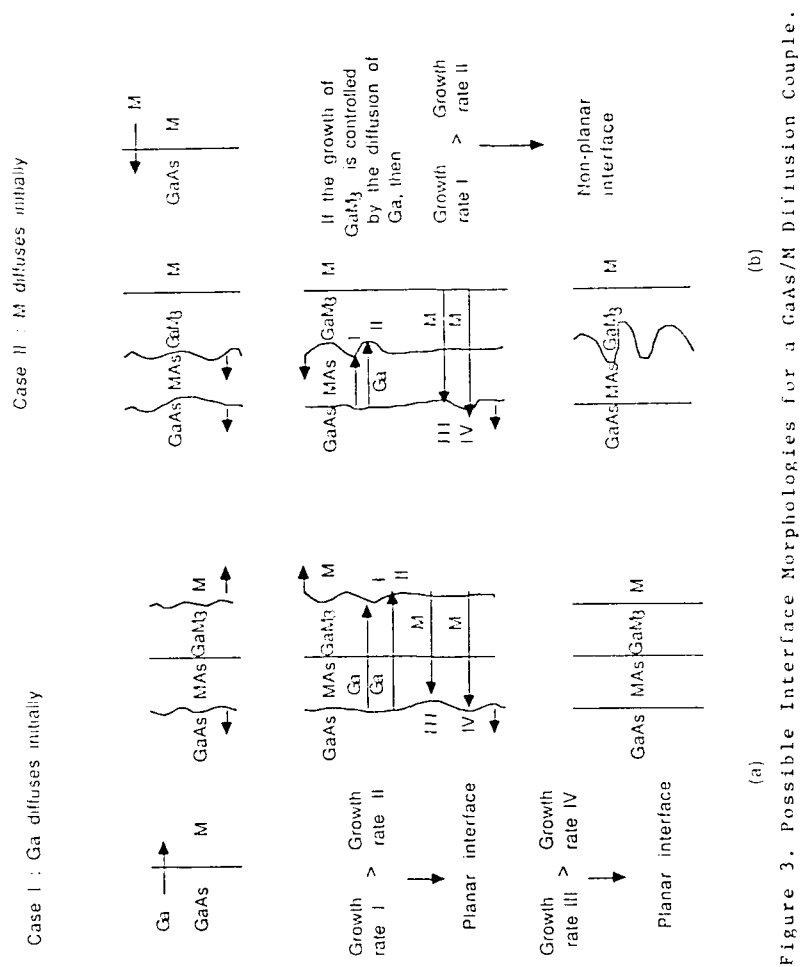
2.2.2 Interface Morphology

Up to this point, we have not discussed the interface morphology, which is determined by the growth kinetics of the phases in a couple. Wagner³¹ has considered the morphological and kinetic aspect of displacement reactions in the solid state. In a later paper, Wagner³² established the criteria for the stability of a flat growth interface. Rapp and co-workers³³⁻³⁵ have utilized this concept to study reactions in M/oxide and M/sulfide couples. Let us now apply these criteria to a GaAs/M diffusion couple under two specific conditions as discussed by Lin et al.⁵ In Fig. 3(a), assuming that the initially predominant moving species is Ga and that As diffuses the slowest, the growth of GaM₃ and MAS would necessarily occur at the GaM₃/M and GaAs/MAS interfaces, respectively. A moving interface is referred to as a growth front. The growth of GaM₃ and MAS is controlled by the diffusion of Ga and M respectively. The flux of Ga arriving at position I exceeds that at position II, resulting in the formation of a planar GaM₃/M interface. Similarly, the flux of M arriving at position III exceeds that at position IV, again resulting in the formation of a planar GaAs/MAS interface. On the other hand in the second case, as is shown in Fig. 3(b), the species M is the predominant moving element for the growth of GaM₃ and MAS. In this case, the growth fronts of GaM₃ and MAS are at the MAS/GaM₃ and GaAs/MAS interfaces, respectively. If the rate-controlling step for the growth of GaM₃ is the diffusion of Ga, then the growth rate at position I is higher than that at position II. Under these circumstances, a planar MAS/GaM₃ interface would be unstable. The situation for the GaAs/MAS interface is the same as that in Fig. 3(a) and therefore the interface remains planar. From the above discussion, it may readily be seen that a knowledge of the predominant moving element and the rate controlling steps to phase growth are the key points to understanding and predicting interface morphology. In fact, we have successfully applied the above concept to the preliminary results obtained for GaAs/Pt^{10,11}, GaAs/Ir^{10,15}, GaAs/Co⁶, GaAs/Ni⁸, and GaAs/Nb.¹⁰

2.2.3 Phase Formation Sequence

The diffusion path of a ternary diffusion couple such as GaAs/M represents the stable phase arrangement between the end phases, i.e. GaAs and M for the GaAs/M couples. However, depending upon the types of phase equilibria and the relative mobilities of the component elements, the phases formed initially and even the phases formed subsequently may not correspond to the stable phase arrangements. Although it is difficult to know in advance precisely the phase formation sequence, we may follow the ideas suggested by Lin et al.⁵ to forecast possible phase formation sequences. The three phase diagrams given in Fig. 1 are reproduced in Fig. 4. Let us assume that the diffusion path corresponds to GaAs|MAS|GaM₃|M for the case shown in Fig. 4(a) and to GaAs|MAS|GaM|GaM₃|M for the cases shown in Figs. 4(b,c). Three possible reaction sequences are given in Fig. 4. Let us now discuss the rationale for forecasting the reaction sequences for the phase diagram in Fig. 4(c).

When a GaAs/M couple is exposed to a high enough temperature, interdiffusion will occur at the interface. Initially the overall composition near the interface should be close to the GaAs and M connection line. Once the amount of foreign elements reaches the sustainable limit of the crystalline solid, new phases nucleate at the interface. According to the phase diagram in Fig. 4(c), the T phase would most likely form first. This behavior is due to kinetics. The composition of the T phase is close to the initial composition at the interface, and therefore less time would be necessary to redistribute the elements in order to nucleate this phase.



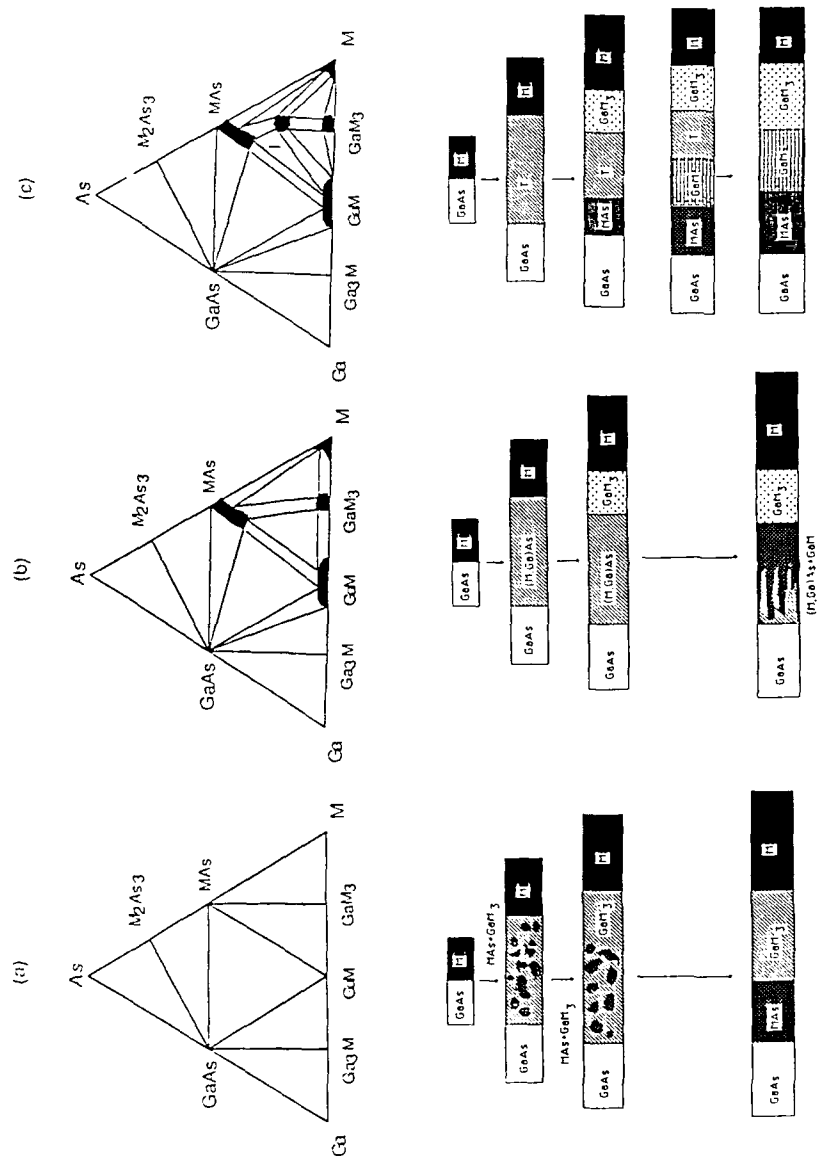


Figure 4. Possible phase formation sequences for three types of Ga-M-As phase diagrams.

We would then have an initial configuration of GaAs|T|M, but none of the interfaces would be at thermodynamic equilibrium. Consequently, more reaction evolution would take place. Although several phases may nucleate and form at the GaAs|T and T|M interfaces, we believe MAS would be the first one to nucleate and grow at the GaAs|T interface. Again, it would take less time to redistribute the elements from T to nucleate and form MAS than would be required to form GaM. At the same time, the phase GaM₃ would probably form at the T|M interface since it is in equilibrium with T and M. The configuration would then be GaAs|MAS|T|GaM₃|M with all of the interfaces at thermodynamic equilibrium.

Although the phases between GaAs and M are now thermodynamically stable, some of these phases may be kinetically unstable. The kinetic stabilities of the phases depend upon the relative fluxes at the various interfaces. Let us suppose that T is kinetically unstable. This is a reasonable assumption since the growth of a ternary phase or a solution phase in the ternary region requires specific elemental flux ratios. Then MAS and GaM₃ would grow at the expense of T with subsequent formation of GaM. The most likely evolution of the reaction sequence would be GaAs|MAS|GaM|T|GaM₃|M with the final stable configuration of GaAs|MAS|GaM|GaM₃|M, the diffusion path.

The preliminary results we have obtained concerning the reaction sequences for GaAs/Co^{2,4,6,9}, GaAs/Ni⁸, GaAs/Pd^{1,10} and GaAs/Pt^{10,11} are consistent with the arguments presented above. We are currently conducting more extensive experimental studies on GaAs/Co, GaAs/Ni and GaAs/Pt to firmly establish the reaction sequences already found in light of the above discussion.

2.2.4 Quantitative Layer-Growth of Phases

Up to this point, we have discussed only qualitative arguments for the formation of phases in a ternary diffusion couple such as GaAs/M. We now present the basic quantitative formulation for the growth of phases formed in a bulk diffusion couple in terms of ternary diffusion theory. Onsager⁴⁸⁻⁵⁰ has shown that the diffusional flux, J_i , in a multi-component system may be expressed as a linear function of the chemical potential gradients. However, because chemical potential gradients are not convenient for experimental analysis, these equations are transformed, making use of the concentration gradients as independent variables. This leads to the generalized form of Fick's first law for a ternary system,

$$\tilde{J}_1 = - \tilde{D}_{11} \frac{\partial C_1}{\partial x} - \tilde{D}_{12} \frac{\partial C_2}{\partial x} \quad [1.A]$$

$$\tilde{J}_2 = - \tilde{D}_{21} \frac{\partial C_1}{\partial x} - \tilde{D}_{22} \frac{\partial C_2}{\partial x} \quad [1.B]$$

where \tilde{D}_{11} and \tilde{D}_{22} reflect the effect of the concentration gradient of a given component on its own flux and \tilde{D}_{12} and \tilde{D}_{21} represent the cross-effects, or the ternary diffusional interactions. The subscript 1 refers to component A (or 1) and 2 refers to component B (or 2). C_1 and C_2 are concentrations and x is a distance coordinate. Combining the above equations with the equations of continuity yields

$$\frac{\partial C_1}{\partial t} + \frac{\partial \tilde{J}_1}{\partial x} = 0 \quad [2.A]$$

$$\frac{\partial C_2}{\partial t} + \frac{\partial \tilde{J}_2}{\partial x} = 0 \quad [2.B]$$

where t denotes time. Substituting Eqs. [1] into Eqs. [2] and neglecting the compositional dependencies of the \tilde{D}_{ij} 's, we have Fick's second law for a ternary system

$$\frac{\partial C_1}{\partial t} = \tilde{D}_{11} \frac{\partial^2 C_1}{\partial x^2} + \tilde{D}_{12} \frac{\partial^2 C_2}{\partial x^2} \quad [3.A]$$

$$\frac{\partial C_2}{\partial t} = \tilde{D}_{21} \frac{\partial^2 C_1}{\partial x^2} + \tilde{D}_{22} \frac{\partial^2 C_2}{\partial x^2} \quad [3.B]$$

Parametric solutions to these equations are of the form

$$C_1 = C_1(\lambda) \quad [4.A]$$

$$C_2 = C_2(\lambda) \quad [4.B]$$

where $\lambda = x/\sqrt{t}$, provided that the boundary conditions of a semi-infinite couple are met. Two important conclusions can be made from these equations. First, a unique solution exists for a given set of boundary conditions, i.e. only one diffusion path exists for a given temperature and pressure. Second, the growth of a phase varies with the square root of time.

Kirkaldy³⁶⁻⁴¹ has solved the basic ternary diffusion equations and furthermore has applied the solution to the growth of a ternary two-phase system. He and his co-workers have not applied the solution to the growth of multi-phase ternary systems. In addition to the works of Kirkaldy and co-workers, other investigators have tackled ternary diffusion in a number of single-phase and simple two-phase systems.

In the case of GaAs/M, the growth of the intermediate phases is more complicated since several phases exist in addition to GaAs and M. Moreover, diffusion coefficients for the component elements in most of the phases are unknown. Our approach to this problem is to obtain diffusion coefficients from the analysis of the layer growth and the concentration gradients within the single-phase regions, if measurable ranges of homogeneity exist for these phases. Jan⁴² has applied the solution to ternary diffusion equations to multi-phase ternary systems. With certain simplifications, he has been able to obtain satisfactory results using the limited experimental results obtained by Schulz¹⁰ for GaAs/Ni and GaAs/Nb.

2.2.5 Bulk vs Thin-Film Couples

In bulk diffusion couples, an infinite supply of the two end phases is realized. This is not the case for a thin-metal film deposited on GaAs. The metal thin-film may be consumed during the growth of the first phase. This situation was discussed briefly toward the end of Section 2.2.1. Except for the limited supply of M in the thin-film couple, similar phase growth sequences and arrangements would occur in bulk and thin-film couples. This correlation has been observed by us for a number of GaAs/M couples, with M being Pd, Pt, Co, Ni, Rh or Ir.^{1,5-8,10,11,13,15} This implies that chemical stability is the primary factor governing phase formation in these systems. The initial and transient phase configurations may be influenced by strain energy (lattice mismatch) and interfacial energies. The final, stable phase configuration, however, will be determined primarily by chemical stability, i.e. equilibrium thermodynamics.

3.0 Summary

Interfacial stability is a key issue and a challenge for the development of new contact materials for GaAs. In general, a kinetically

stable interface may be maintained at room temperature. However, in GaAs technology, processing temperatures can be as high as 800°C. At such high temperatures, one cannot rely upon kinetic factors to stabilize the interfaces. In this paper, a general approach has been provided for the understanding of interfacial stability. The discussions in section 2.0 show that thermodynamic and kinetic factors actually determine the reaction sequences, interface morphologies and final phase arrangements, i.e. diffusion paths. Further study is needed to correlate the chemistry and morphology with electrical properties of interfaces. Such information is very important in the design of electronic devices.

The general concepts of reaction sequence and diffusion path are not only suitable for GaAs/metal interface study but are also applicable to other materials with heterogeneous interfaces. For instance, the interactions between surface film and bulk usually determine the life times of coatings for wear or corrosion resistance; the interfaces between fiber and matrix are highly related to the mechanical properties of structural composites. A basic understanding of interfacial stability is urgently needed for the development of new materials and the improvement of processing parameters.

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A STUDY OF THERMODYNAMIC PHASE STABILITY OF INTERMETALLIC THIN FILMS OF Pt_2Ga , PtGa AND PtGa_2 ON GALLIUM ARSENIDE

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ABSTRACT

Epitaxial thin films of three different Pt-Ga intermetallic compounds have been grown on GaAs by molecular beam epitaxy (MBE). The resultant films have been annealed at various temperatures and then examined using X-ray two-theta diffraction. Both PtGa_2 and PtGa thin films are chemically stable on GaAs under 1 atmosphere of N_2 up to 450°C and 600°C, respectively. Thin films of Pt_2Ga react with GaAs at temperatures as low as 200°C to form phases with higher Ga concentration.

Introduction

The interface chemistry of metal-semiconductor contacts plays an important role in controlling the electrical properties of Schottky barriers and Ohmic contacts [1]. Chemically stable contacts must be formed at the metal-semiconductor interface in order for electronic devices to survive processing procedures and operate reliably in harsh environment applications for long periods of time [2,3]. A possible solution for this interface problem would be to use a contact metal that can coexist with GaAs in bulk thermodynamic equilibrium. Such stable metals can be found by examining ternary phase diagrams, such as the Pt-Ga-As system, which was experimentally elucidated by Tsai et. al. [4] and is illustrated in Fig. 1. The existence of a pseudobinary tie-line between two compounds in the ternary phase diagram implies that the compounds will not react with each other in a closed system, i.e. the bulk compounds are in thermodynamic equilibrium with respect to each other. Therefore, from Fig. 1 it can be expected that PtGa and PtGa_2 will form stable contacts with GaAs but that Pt_2Ga will not. In the present study, these expectations are tested by investigating the phase composition of thin films of Pt_2Ga , PtGa and PtGa_2 on GaAs after annealing to various temperatures.

Film Growth

The Pt-Ga intermetallic films were grown in a MBE chamber with a base pressure of 2×10^{-10} torr and a deposition pressure of approximately 4×10^{-9} torr. The two inch GaAs substrates were introduced via a cryopumped load lock system and mounted on a modified manipulator equipped with radiative heating elements. The samples were cleaned in-situ by heating to a temperature of approximately 525°C. The platinum was evaporated using a Varian 3 KW electron beam evaporator and the gallium was obtained from a Knudsen cell constructed of a pyrolytic boron nitride (PBN) crucible with a tantalum heating element. The fluxes of platinum and gallium were initially tuned to the proper stoichiometry based on empirical knowledge. PtGa_2 can be visually identified by its characteristic golden color, since PtGa_2 is the only Pt-Ga phase that has a band structure similar to that of elemental gold [5]. Neither PtGa nor Pt_2Ga can be easily identified by color. The flux rate from the gallium source was stabilized by temperature control circuits that ensured a constant flux rate for each source power setting. Subsequent depositions have been controlled with a Leybold-Inficon IC-6000 crystal monitor system. To obtain single phase Pt-Ga intermetallic films, the flux ratio of gallium to platinum was adjusted to be slightly Ga rich. Co-evaporation of each Pt-Ga intermetallic proceeded with the substrate held at temperatures ranging from near room temperature to over 500°C at epilayer growth rates ranging from approximately 0.5 to 5 microns/hour.

Composition Analysis

XRD patterns of the films were taken on a Phillips X-ray powder diffractometer, which was interfaced to a microcomputer that controlled the scan rate and collected data at 0.1° intervals with a counting time of 10 seconds at each angle. The total time required for a complete scan (2 θ from 10° to 100°) was about 3 hours and the typical signal-to-noise ratio for a strong diffraction peak was 30 to 1. The d spacings of the PtGa_2 and Pt_2Ga thin films were checked against a reference tabulation [6] to ensure that they were identified correctly. As

no known PtGa JCPDS data exists, the known d-spacings of PtGa [7] were compared with values calculated from the diffraction pattern of the thin film and were found to agree closely. The thin films were annealed for twenty minutes in a quartz tube furnace under a nitrogen atmosphere for temperatures ranging from 100°C to 800°C. In this paper, we present XRD results of annealing studies of the Pt-Ga intermetallic single phase thin films. A complete characterization of these films, including Auger electron spectroscopy (AES) and X-ray photoemission spectroscopy (XPS), will be presented elsewhere [8].

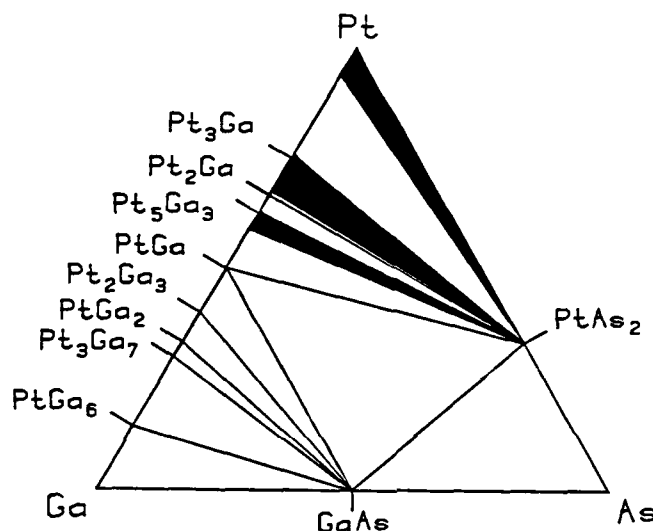


Fig. 1. Solidus portion of the Pt-Ga-As ternary phase diagram at 25°C.

Results and discussion

The grown films were specular, both to the eye and by optical microscopy. Fig. 2 shows typical powder XRD patterns of the three types of intermetallic single phase Pt-Ga thin films grown on GaAs (001) in the as-deposited state. The PtGa and Pt₂Ga thin films have a dominant (210) and (112) reflection, respectively. The PtGa₂ thin films displayed roughly equal intensity (111), (220) and (311) reflections. This would seem to imply that the crystal quality of PtGa and Pt₂Ga thin films is better than that of PtGa₂ films in spite of larger lattice mismatches. XRD patterns of a sample of Pt₂Ga on GaAs annealed to 500°C are shown in Fig. 3. Even at 200°C, a new peak corresponding to the PtGa (210) reflection begins to appear at $2\theta = 41.4^\circ$. In the diffraction patterns of the film heated to high temperatures, new phases, such as PtGa₂ and PtAs₂, begin to form at 300°C and all peaks corresponding to the Pt₂Ga phase eventually disappeared at 500°C. According to the Pt-Ga-As ternary phase diagram, Pt₂Ga is expected to react with GaAs to produce PtAs₂ and PtGa, because there is no tie-line between Pt₂Ga and GaAs. However, annealing in an open system may cause As evaporation resulting from thermal decomposition of PtAs₂ and GaAs. With further loss of As, other Pt-Ga intermetallic compounds, such as PtGa₂ and Pt₃Ga₇, may be produced. This prediction agrees very well with the experimental results: all the peaks correspond to PtGa, PtGa₂, Pt₃Ga₇ and PtAs₂ in the diffraction pattern of the Pt₂Ga thin films on GaAs annealed to 500°C.

Fig. 4 shows XRD patterns of PtGa on a GaAs sample in the as-deposited state and after annealing at various temperatures for 20 minutes each. The diffraction pattern of the PtGa film annealed to 200°C shows that a small peak corresponding to Pt₂Ga (112) beside the PtGa (210) disappeared and the other PtGa peaks became sharper and more intense. This implies that a small amount of unstable Pt₂Ga phase in the PtGa thin film reacted with extra Ga in the film or with the substrate. Annealing improves the crystallinity of the PtGa

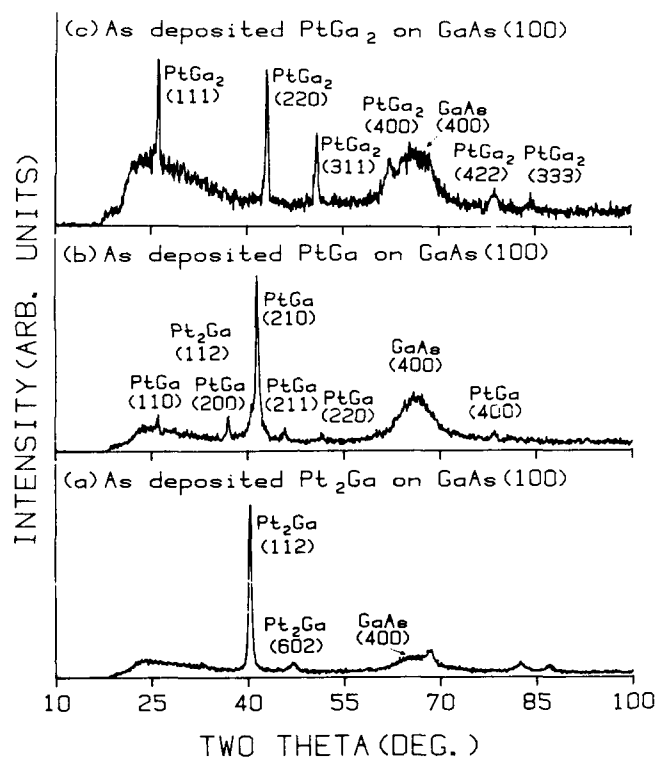


Fig. 2. XRD patterns of the three types of intermetallic single phase Pt-Ga thin films grown on GaAs (100) in the as-deposited state: (a) as-deposited Pt_2Ga on GaAs; (b) as-deposited PtGa on GaAs; (c) as-deposited PtGa_2 on GaAs.

film, since the signal-to-background ratio in the XRD patterns begins to increase as annealing temperature goes up. The diffraction patterns for the PtGa film annealed from 300°C to 600°C were essentially identical, but the signal-to-background ratio began to decrease. Annealing in an open system, such as in vacuum or under inert gas, may cause both PtAs_2 and GaAs to decompose thermally to produce gas phase As species. Therefore, in this case, the PtGa thin film starts to become Ga rich and PtGa_2 and Pt_3Ga_7 are produced, which coexist with PtGa and GaAs. Fig. 5 shows XRD patterns of a sample of PtGa_2 on GaAs heated to 100°C, 300°C, 450°C and 500°C, respectively, along with the pattern of an as-deposited film. The diffraction patterns for the sample were essentially identical up to 400°C. A new peak corresponding to the Pt_3Ga_7 (322) reflection begins to appear in XRD patterns of the sample annealed in the range of 450°C to 500°C. It is possible the PtGa_2 phase begins to react with extra Ga due to As evaporation from GaAs upon annealing.

Conclusions

Single phase thin films of Pt_2Ga , PtGa, and PtGa_2 have been successfully grown on GaAs by MBE. The results of annealing studies are in good agreement with the Pt-Ga-As ternary phase diagram. PtGa_2 and PtGa films are chemically stable on GaAs up to 450°C and 600°C, respectively. However, the Pt_2Ga films start

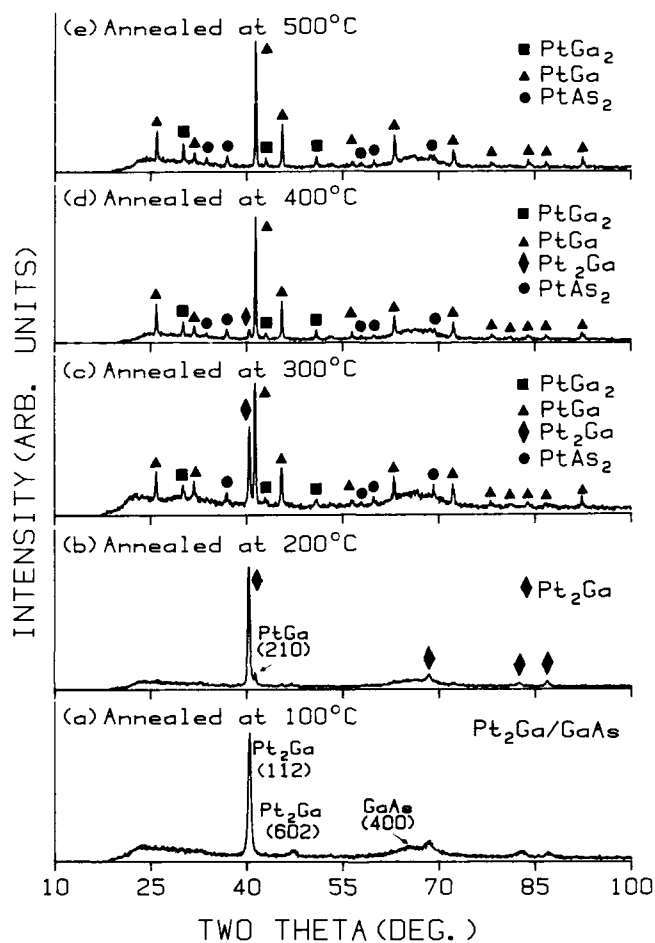


Fig. 3. XRD patterns of Pt_2Ga thin films on $\text{GaAs}(100)$ for sample annealed to (a) 100°C , (b) 200°C , (c) 300°C , (d) 400°C and (e) 500°C .

to react with GaAs even at temperatures of 200°C to produce PtGa , PtGa_2 , Pt_3Ga_7 and PtAs_2 at temperatures of 500°C . It has been shown here that the thermodynamics of bulk materials can be used to control the chemistry at the metal/semiconductor interface. In order to understand the Pt-Ga intermetallic system further, several additional studies including annealing studies under As ambient, temperature dependent TEM and transport measurements of various intermetallic Pt-Ga phases grown by MBE still need to be carried out.

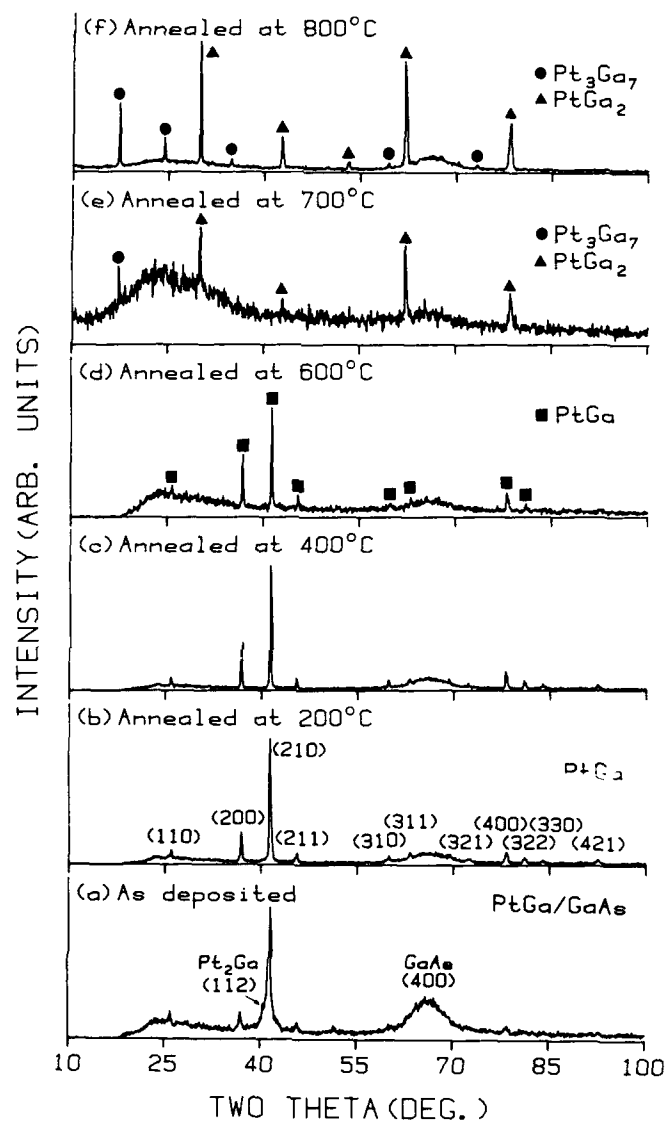


Fig. 4. XRD patterns of PtGa thin films on GaAs (100) for (a) the as-deposited film and after the sample was annealed to (b) 200°C, (c) 400°C, (d) 600°C, (e) 700°C and (f) 800°C.

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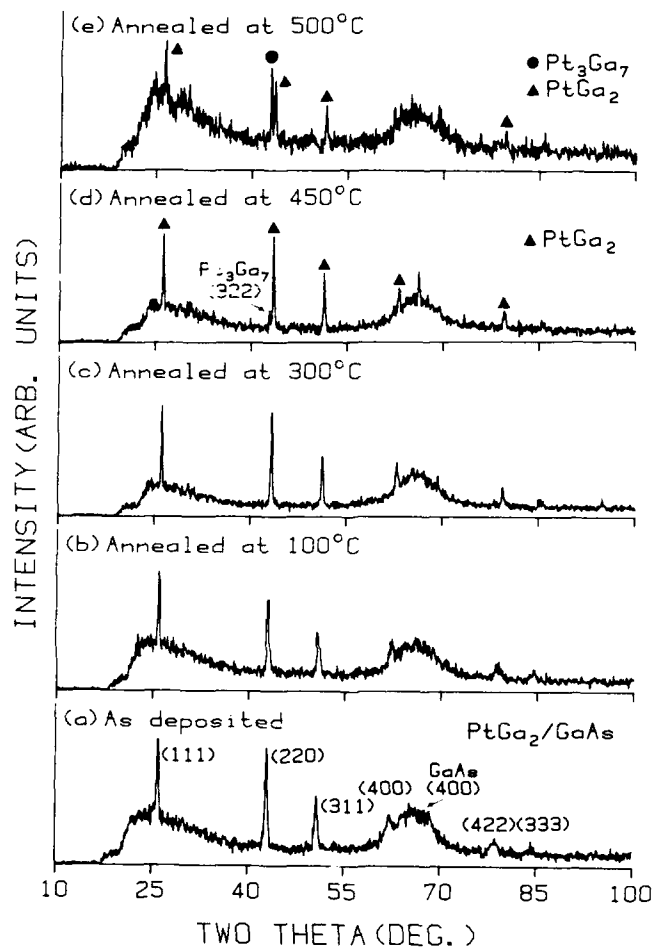


Fig. 5. XRD patterns of PtGa_2 thin films on GaAs (100) for (a) the as-deposited film and after the sample was annealed to (b) 100°C, (c) 300°C, (d) 450°C and (e) 500°C.

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IN-SITU ANNEALING TRANSMISSION ELECTRON MICROSCOPY(TEM) STUDY OF THE Ti/GaAs INTERFACIAL REACTIONS

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ABSTRACT

In-situ annealing TEM experiments were performed on the Ti/GaAs system in order to study the dynamic behavior of interfacial reactions. Both plan-view and cross-sectional samples were investigated in either diffraction and imaging (both conventional and high resolution) modes. During experiments, we observed the following: (a) At the initial stage of reaction, the TiAs phase formed at the original Ti/GaAs interface with a distinct orientation with respect to the substrate; (b) as the reaction proceeded, the TiAs phase formed in a random manner; (c) finally, the liberated Ga species from the GaAs diffused out to the metal film and formed TiGa₂ phase in the plan-view sample similar to the furnace-annealed case. For the cross-sectional sample, however, we did not observe any Ti:Ga phase formation. Instead, we observed the formation of voids both in the Ti film and in the GaAs substrate. The formation of different microstructure between *in-situ* and furnace annealed cases is explained by the sample geometry during annealing.

INTRODUCTION

One of the major problems in developing GaAs-based integrated circuits (IC) has been the formation of reliable, reproducible, and controllable metal contacts. These contacts play a central role in device performance and indeed their importance has prompted major studies of either interface or device properties that are influenced by the metal-semiconductor interfaces.[1,2] One important issue has been the thermal stability.[3] Most metal elements react with GaAs upon exposure to elevated temperatures, resulting in a diffuse, often multiphase interface region. As the electrical properties of the contacts, such as barrier height and contact resistance, are often sensitive to the composition and morphology of the interface, phase formation and reaction kinetics must be fully characterized and understood in order to develop a reproducible contact fabrication process.

Previously, we reported the metallurgical reaction between Ti and GaAs in the temperature range 300-600 °C using a combination of Auger electron spectroscopy(AES), transmission electron microscopy(TEM), energy dispersive x-ray spectroscopy(EDAX), and electrical measurements.[4] In that article, we showed that Ti starts to react with GaAs at about 400 °C, producing a layered Ti/Ti:Ga/Ti₂As/GaAs microstructure. The reaction product phases, for fully reacted films, were identified from electron diffraction patterns as a TiP-type TiAs and a TiGa₂(hexagonal structure: $a=0.569$ nm and $c=0.932$ nm). Macroscopic kinetic information was also provided by measuring the thickness of each reaction product layer in terms of a diffusion controlled growth with an activation energy of 1.75 ± 0.05 eV. In this paper, as an extension of previously reported results, we will discuss microscopic reaction behavior such as the formation of the initial phase and its crystallographic relationship with the GaAs substrate, the sequences of phase formation, and the evolution of microstructure during reaction utilizing the *in-situ* annealing TEM technique.

EXPERIMENTAL PROCEDURES

Commercially available n-type (100) GaAs wafers doped with Si ($1 \times 10^{17}/\text{cm}^3$) were chemically cleaned and 50 nm thick Ti films were electron-beam deposited at a base pressure of about 10^{-8} torr. Plan-view and cross-sectional TEM samples were prepared by following the procedure described by Bravman and Sinclair[5] in which sections are glued, dimpled, and ion-milled. Samples were examined *in-situ* in a Philips 430ST microscope operating at 300 kV. Detail information of the *in-situ* experimental procedures are reported elsewhere.[6,7]

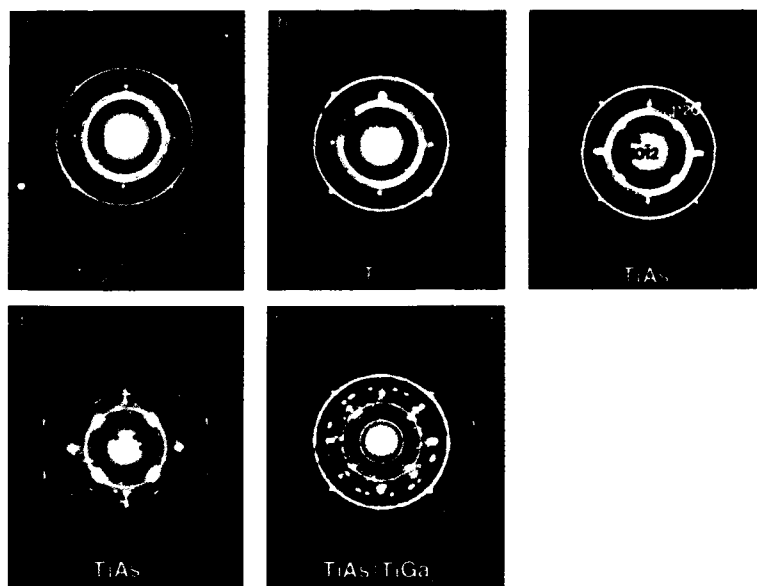


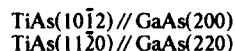
Fig.1 A series of SAD pattern obtained from the plan-view Ti/GaAs sample ((a) as-deposited, (b) 300 °C, (c) 400 °C, (d) 500 °C, and (e) 600 °C). Temperatures were increased step by step and the diffraction patterns were obtained after about 5 min. at each temperature increments. Arrows in the diagram indicate new diffraction effects which appear in each sequence.

RESULTS AND DISCUSSIONS

A. Plan-view Sample

Figure 1 shows a series of selected area diffraction patterns obtained during *in-situ* annealing in the TEM, which demonstrates the sequence of phase formation and its crystallographic relationship with the GaAs substrate as the reaction proceeds. The as-deposited sample (Fig. 1(a)) shows continuous ring patterns of hcp-Ti and the [100] zone axis of the GaAs substrate. Ring patterns can be indexed as (xyz0) type of hcp-Ti indicating that the Ti film forms a strong basal-plane texture. The exact [100] zone axis of GaAs pattern was used to align the TEM sample in the microscope with respect to the electron beam during the experiments. Upon annealing (nominal temperature of about 300 °C), the first change observed in the diffraction pattern (Fig. 1(b)) was the appearance of ring patterns at interplanar spacings of 1.73 and 1.37 Å. These patterns can be indexed as Ti(01 $\bar{1}$ 2) and Ti(01 $\bar{1}$ 3), respectively, indicating that the Ti film is gradually losing its basal plane texture. The results demonstrate that the basal-plane texture formed during film deposition is energetically in an unfavorable state compared to the case when the grains are randomly oriented.

When the sample was further reacted at about 400 °C (Fig. 1(c)), new diffraction spots appeared close to the GaAs(200) and (220) spots. These spots were indexed as TiAs(10 $\bar{1}$ 2) and (11 $\bar{2}$ 0). The appearance of these diffraction spots provides direct evidence that the first phase formed by the reaction is TiAs, and furthermore, the TiAs phase formed at this initial stage of reaction shows a strong orientation relation with the GaAs substrate, namely:



This relationship can be understood from the similar interplanar spacings of those planes ($d_{\text{GaAs}(200)}=2.83 \text{ \AA}$ and $d_{\text{TiAs}(10\bar{1}2)}=2.82 \text{ \AA}$; $d_{\text{GaAs}(220)}=2.00 \text{ \AA}$ and $d_{\text{TiAs}(11\bar{2}0)}=1.83 \text{ \AA}$). However, upon prolonged annealing, this orientation relationship gradually disappeared. In Fig. 1(d), we note that the diffraction spots from TiAs gradually form a ring pattern while the strong intensity spots can still be seen close to the GaAs (200) and (220) spots. Also, note that even those strong intensity spots show a symmetric separation of about 5 degrees from their original positions which indicates that the TiAs (10 $\bar{1}$ 2) and (11 $\bar{2}$ 0) planes are tilted symmetrically with respect to the GaAs(200) and (220) planes. This result demonstrate that the TiAs grains grew in a more random manner as the reaction proceeds, in other words, the energy gained by the formation of an epitaxial layer of TiAs on the GaAs substrate is not significant and can not be the dominant factor for the whole reaction. The identification of any Ti-Ga phase formed during reaction was problematic, so far. Finally, Fig. 1(e) shows the case when the Ti film is completely reacted with GaAs. The diffraction pattern can be indexed as TiAs and hexagonal structure TiGa_2 as was the case for the furnace annealed sample.[4]

B. Cross-Sectional Sample

Figure 2 shows a series of cross-sectional TEM micrographs obtained during *in-situ* annealing of the Ti/GaAs system. Direct observations were made during the experiments that a new layer formed and progressed into the GaAs substrate. Microdiffraction pattern obtained in this layer not only identified it as TiAs but also showed the following orientation relationship between this TiAs and GaAs substrate(Fig. 3) as was shown in plan-view sample:

$$[\bar{1}\bar{1}01]\text{TiAs} // [011]\text{GaAs}$$

$$(1\bar{1}02)\text{TiAs} // (200)\text{GaAs}$$

$$(11\bar{2}0)\text{TiAs} // (022)\text{GaAs}$$

and

$$(02\bar{2}2)\text{TiAs} // (222)\text{GaAs}$$

While the preferred orientation relationship between the GaAs substrate and the reaction product phase formed in contact with it has often been identified in several M/GaAs ternary diffusion

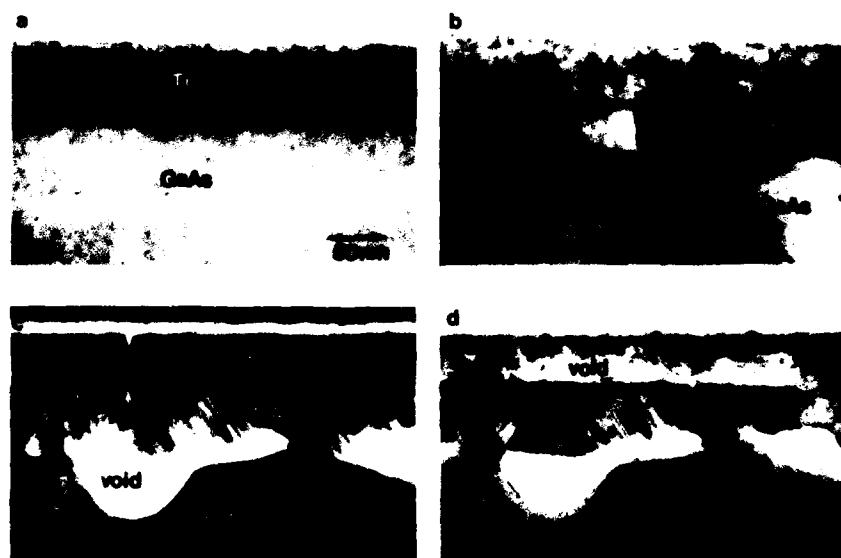


Fig. 2 A series of cross-sectional TEM micrographs obtained during *in-situ* TEM annealing of a Ti/GaAs system ((a) as-deposited, (b) 400 °C, 30 min., (c) 500 °C, 30 min., and (d) 600 °C, 30 min.).

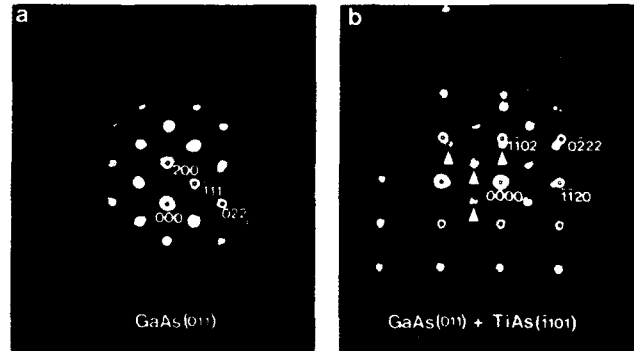


Fig. 3 Microdiffraction patterns of (a) GaAs substrate and (b) GaAs and TiAs obtained from cross-sectional sample. Arrows in (b) indicate the GaAs spots.

couples[8-12], those results do not show the progress of the relationship as the reaction proceeds. On the other hand, our results clearly demonstrate the formation of an epitaxial layer at the initial stages of the reaction and also the progressive changes of this relationship.

When a comparison of the evolution of morphology between the furnace and *in-situ* annealed samples was conducted[6], several differences were observed. First, it was discovered that the TiAs structure formed during *in-situ* experiments, in general, contains a high density of defects (micro-twins) lying parallel to the projection of GaAs (111) plane. This indicates that the formation mechanism of the TiAs layer during the *in-situ* experiments is different from the furnace annealed case. Second, we did not observe any distinct Ti:Ga-layer formed in between Ti and TiAs layer during the reaction, contrary to the furnace annealed case. This raises the question concerning the behavior of Ga, which was presumably liberated upon the formation of TiAs. Finally, when the samples were fully annealed, we observed the formation of voids both at the Ti/TiAs interface and in the GaAs substrate beneath the TiAs layer.

The differences in the evolution of the morphology between the furnace and *in-situ* annealed samples can be understood by considering the geometry of the TEM sample during annealing (Fig. 4). For the furnace annealed case, most of the interfacial reactions occur at the area which is located far from the edge of the sample. And more importantly, since the cross-sectional TEM samples were made after annealing, it is not possible to observe any abnormal effects which

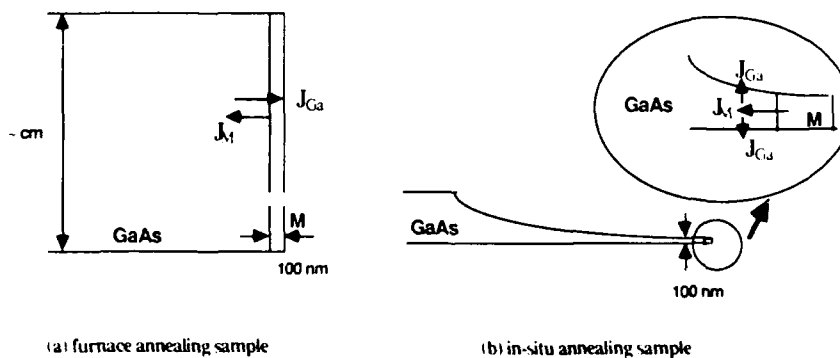


Fig. 4 Schematic diagrams of the sample geometry during annealing. Circled areas are enlarged in (b).

might occur at the edge (See Fig. 4(a)). However, for the case of *in-situ* annealing, most of the interfacial area between Ti and GaAs lay close to the top and bottom surface as the thickness of the TEM sample should be below a few thousand Å for electron beam transparency. Therefore, surfaces can strongly affect the evolution of morphology during the reaction in the latter case.

Considering these surface effects, the difference in the evolution of morphology for the Ti/GaAs reaction can be explained as follows. First, as has been demonstrated by the *in-situ* annealing experiments, the reaction starts by the diffusion of Ti into the GaAs substrate and the formation of TiAs. Second, as a result of this TiAs formation, the reaction liberates Ga species from the GaAs substrate. At the initial stage of the reaction, i.e. when the reaction does not form a continuous layer of TiAs at the interface, these Ga species diffuse to the Ti film in both furnace and *in-situ* annealed cases and forms a Ti(Ga) solid solution. However, once the reaction produces a continuous layer of TiAs, the Ga species behaves in a different manner. For the furnace-annealed case, Ga diffuses through the TiAs layer to the Ti film in order to form the Ti:Ga phase since this reaction is favored from thermodynamic considerations. For the *in-situ* annealed case, however, the Ga tends to segregate on the top and bottom surface of the TEM specimen rather than diffusing through the TiAs layer because of the extremely thin-nature of the TEM sample. High surface energy, short diffusion length to the surface, and fast surface diffusion act as main causes for this Ga segregation. This fast diffusion of Ga to the surface of the sample during the *in-situ* annealing compared to the relatively slow diffusion of Ga through the TiAs layer during the furnace annealing is considered as one of the main causes of those microstructural differences of TiAs. Finally, when there is sufficient accumulation of Ga at the top and bottom surface of the TEM sample, the agglomerated Ga presumably melt due to the low melting temperature of elemental Ga. Furthermore, as the elemental liquid Ga can contain some amounts of As in equilibrium depending on the temperature, it will locally melt the GaAs substrate.[6]

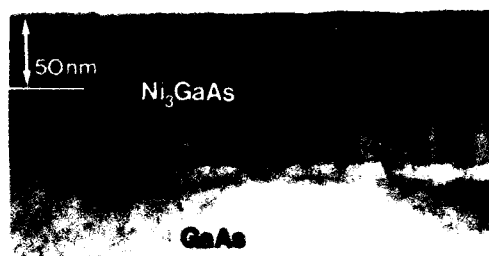
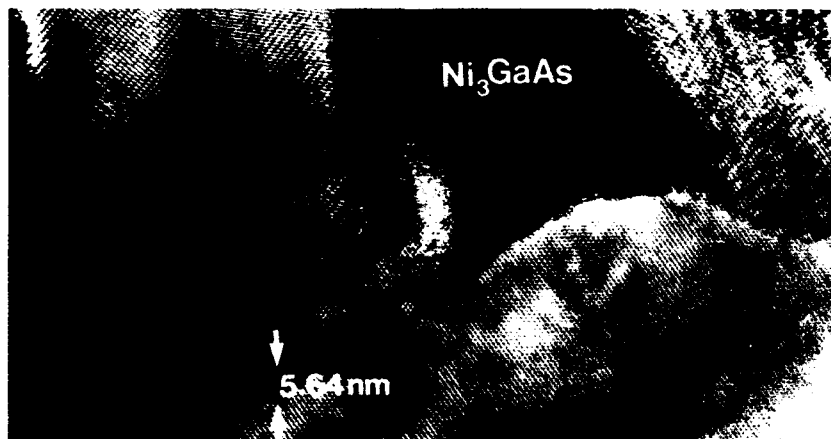


Fig. 5 Cross-sectional micrographs ((a) bright field and (b) high resolution) of the Ni/GaAs system. Micrographs are obtained during *in-situ* annealing at a nominal temperature of 300 °C. In (a), the original Ni/GaAs interface (~ 50 nm from the surface) is shown as a line.



As has been discussed, the evolution of the morphology during *in-situ* annealing experiments of the Ti/GaAs system is strongly affected by the thin nature of the TEM sample. One of the main reasons for this different evolution of the morphology is the different properties of elemental Ga and As as compared to the GaAs compound. For example, if the elemental metal (M) reacts with the GaAs substrate and forms an M_yAs compound while liberating the Ga species, then the Ga species easily accumulates at the surface of the TEM sample and melts. Conversely, if the M forms M_xGa and liberates the As species by the reaction, then the As species easily accumulates and sublimates because of its high vapor pressure. These properties, however, can be useful in deducing the reaction sequence as has been demonstrated.

In order to support these explanations, *in-situ* annealing cross-sectional TEM experiments of the Ni/GaAs system were performed. From the several furnace annealing thin-film diffusion couple experiments [13-15], it has been demonstrated that Ni forms a ternary phase(s) (Ni_2GaAs) first and this ternary phase eventually dissociates into two binary phases ($NiGa$ and $NiAs$) as the reaction proceeds. This result indicates that the interfacial reaction of the Ni/GaAs system does not require a long diffusion length of elemental Ga, unlike the case of the Ti/GaAs system. For this reason, if our explanation that the holes are formed by the segregation of Ga on the top and bottom surfaces of the TEM sample for the Ti/GaAs system is correct, then we should expect that such holes would not be formed in the Ni/GaAs system. It is also expected that the evolution of the morphology in the Ni/GaAs system would be similar to the furnace annealed material.

Indeed, Figure 5 shows a series of cross-sectional TEM micrographs of the *in-situ* annealed Ni/GaAs system in which any holes were not observed in the GaAs substrate while extensive reaction was taking place. During annealing, it was also directly observed that the reactions occurred primarily in the GaAs substrate [6,7], indicating that Ni was the prominent diffusing species. The reaction product phase was identified as the Ni_3GaAs ternary phase by measuring the d-spacings and the angles of the planes from the high resolution electron micrograph (Figure 5b). [15]

Interestingly, when this Ni/GaAs sample was annealed at a higher temperature (nominally 550 °C), it was observed that a hole was formed in the metal film (Fig 6). It has been known from furnace annealing experiments that the $NiAs$ phase, formed by the dissociation of Ni_2GaAs , disappears during high temperature annealing (above 500 °C) in a vacuum by the sublimation of As. [16] The sublimation of arsenide phase during vacuum furnace annealing was also reported in the Pd/GaAs system. [17] Therefore, we can suggest that the formation of hole in this experiment is due to the sublimation of As from the $NiAs$. The results of *in-situ* TEM annealing of Ni/GaAs, therefore, are considered similar to that of furnace annealing and, more importantly, strongly support our explanation of the *in-situ* annealed Ti/GaAs system results.

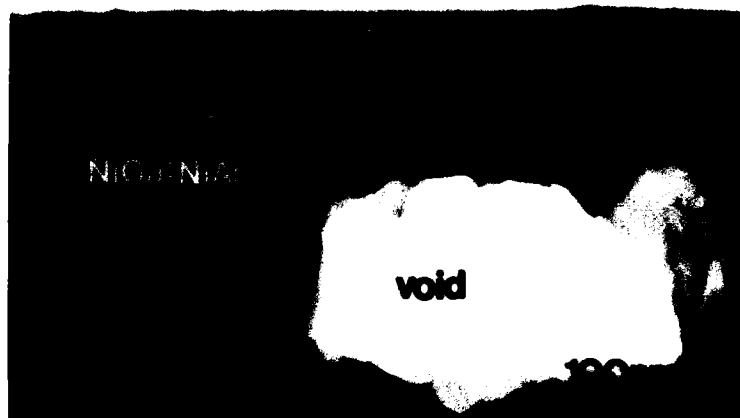
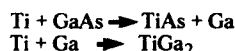


Fig. 6 Cross-sectional micrograph of the Ni/GaAs system. Samples were *in-situ* annealed in the microscope at the nominal temperature of 550°C.

CONCLUSIONS

From the *in-situ* annealing experiments, we noted the following:

- (1) Interfacial reaction of the Ti/GaAs system occurred by the prominent diffusion of Ti into GaAs substrate by the formation of TiAs. The TiAs phase formed at the initial stages of the reaction showed a strong orientation relationship with the GaAs substrate. This relationship, however, disappeared as the reaction progressed.
- (2) The reaction sequences of the Ti/GaAs system, for the furnace annealed case, can be deduced as following:



- (3) It has been demonstrated that the *in-situ* annealing TEM experiments are useful in deducing reaction sequences of M/GaAs systems.

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CORRELATIONS BETWEEN ELECTRICAL PROPERTIES AND SOLID-STATE REACTIONS IN Co/n-GaAs CONTACTS: A BULK AND THIN-FILM STUDY

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ABSTRACT

A fundamental and comprehensive approach has been taken to study Co/GaAs interfacial reactions, using phase diagram determination, bulk and thin-film diffusion couple studies, and electrical characterization. Phase formation sequences and interfacial morphologies are found to be similar in bulk and thin-film couples. Thermodynamic and kinetic analyses are used to rationalize the contact formations. The electrical properties of the contacts are correlated to the phase formation sequences and phase diagram information.

INTRODUCTION

Thermodynamic, kinetic, morphological, and electrical properties of metal contacts on compound semiconductors each have an effect upon the performance of devices. Among these factors, electrical characteristics are of main concern. However, the remaining three factors may not be neglected when designing electrical devices. Only thermodynamically stable and morphologically uniform contacts can ensure electrically reliable devices. Equilibrium phase diagrams provide information concerning which compounds and compositions have stable tie-lines to III-V semiconductors. Lince et al. ⁽¹⁾, Beyers et al. ⁽²⁾, Sands ⁽³⁾, and Lin et al. ⁽⁴⁾ have demonstrated the importance of phase diagrams in selecting stable contacts and for rationalizing M/GaAs contact reactions. However, a phase diagram alone does not provide all of the information necessary for understanding contact formation. The final phase configurations and interfacial morphologies are also governed by the kinetics of the system, including reaction mechanisms, diffusion species, and phase formation sequences. This information can best be obtained from bulk diffusion couple studies. Therefore, to fundamentally understand and rationalize the interfacial reactions between Co and GaAs and to correlate the associated electrical properties, a comprehensive approach using phase diagram determination, bulk and thin-film diffusion couple studies, and electrical characterization is necessary. Such an approach has been taken in the present study.

EXPERIMENTAL PROCEDURE

The details of sample preparation and experimental techniques for phase diagram and bulk diffusions couple studies have been reported in our earlier publications ^(5,6).

Undoped, semi-insulating ($\rho > 10^7 \Omega\text{-cm}$) and Si-doped ($2\text{-}4 \times 10^{17} \text{ cm}^{-3}$) (001) GaAs wafers were used for thin-film study and electrical measurements, respectively. Prior to deposition, GaAs wafers were degreased in acetone and trichloroethylene, etched in a 50% HCl solution for 2 min, rinsed in deionized H_2O , and then dried with N_2 gas. Cobalt films of 40-100 nm in thickness were deposited onto the wafers by electron beam evaporation under a vacuum of 10^{-7} torr. Samples were then encapsulated in 7 mm quartz tubes which were subsequently evacuated to a pressure of 10^{-4} torr. In order to reduce the residual oxygen pressure within the ampoules, high-purity titanium sheets were encapsulated in the quartz tubes along with the samples. The titanium sheets and samples were situated at opposite ends of the ampoules. The Ti ends of the samples were heated to 450 °C for 10 minutes, after which time the samples were isolated from the Ti getters by further sealing of the tubes. Most of the samples were annealed at temperatures of 200-800 °C for 1 h. Some samples were annealed at low temperatures for longer periods in order to study phase stability and reaction kinetics. TEM, XTEM, EDS, AES, and ESCA were used to characterize the phase formation sequences, morphologies and interfacial structures. For electrical characterizations, circular dots 0.5 mm in diameter were patterned on the post-annealed sample

surfaces using photolithography and wet etching techniques. Back-side ohmic contacts were formed by sintering thermally evaporated Au-Ge (12%) films under a forming gas (Ar+10% H₂) at 420 °C for 3 min. Ohmic contacts were formed prior to Schottky metallization for samples annealed below 400 °C and after metallization for samples annealed above 400 °C.

Forward I-V characteristics were used to determine the Schottky barrier heights of the contacts in terms of the thermionic-emission theory, using the equations

$$J = J_s [\exp(qV/nkT) - 1] \text{ A cm}^{-2} \quad (1)$$

$$n = q/kT (dV/d\ln J) \quad (2)$$

where J_s is the saturation current density, which can be determined from a plot of $\ln J$ vs V , n is the ideality factor, V is the applied voltage, T is the absolute temperature, and k is the Boltzmann constant. The barrier height ϕ_b^{I-V} is related to J_s by the equation

$$J_s = A^{**} T^2 \exp[-q(\phi_b^{I-V} - \nabla\phi)/kT] \text{ A cm}^{-2} \quad (3)$$

where A^{**} is the effective Richardson constant (8.16 A cm⁻² K⁻² for n-GaAs), $\nabla\phi$ is the image force lowering, and $(\phi_b^{I-V} - \nabla\phi)$ is the effective ϕ_b to current transport. Hence, the actual Schottky barrier height ϕ_b^{I-V} (at zero bias) as measured by the I-V method contains an image force correction.

According to the one-sided abrupt junction model, a plot of C^{-2} vs applied reverse bias voltage V can be described by the equation

$$C^{-2} = 2 (\epsilon q N_D)^{-1} (V_d - V - kT/q) \text{ F}^{-2} \text{ cm}^{-2} \quad (4)$$

where N_D is the bulk donor density as determined from the slope of a plot of C^{-2} vs V , and ϵ is the GaAs dielectric constant. The intercept V_i on the voltage axis is related to the diffusion potential by $V_i = V_d - kT/q$. Thus, $\phi_b^{C-V} = V_i + \delta + kT/q$, where the δ is the Fermi level energy of the neutral bulk with respect to the conduction band. In the present study, N_D was determined to be $3.6 \times 10^{17} \text{ cm}^{-3}$, and therefore $\phi_b^{C-V} = V_i + 0.056 \text{ eV}$.

RESULTS AND DISCUSSION

Figure 1 shows the initial stages of both bulk and thin-film contact formations. For a bulk couple annealed at 450 °C for 10 days, the SEM micrograph and corresponding cross-sectional concentration profiles shown in Fig. 1(a) reveal that the initial phase formed was Co(Ga₄₈As₅₂). For a thin-film couple annealed at 340 °C for 1 h., the cross-sectional TEM micrograph presented in Fig. 1(b) and EDS analysis indicate the presence of a similar initial phase. TEM diffraction patterns from plan-view samples show that this initial, highly oriented phase adopts the CoAs crystal structure. It was reported to be a ternary phase, Co₂GaAs^(7,8). However, our phase diagram study of this system at 600 °C⁽⁵⁾, the results of which are given in Fig. 1(c), showed that while the CoAs phase has extensive solubility of Ga, about 19 mol% of CoGa in CoAs, there is no ternary phase. Therefore, this so-called ternary phase, Co₂GaAs, is only a supersaturated solid solution of α -CoAs (B31). As pointed out by Lin et al.⁽⁹⁾, kinetically, in a M/GaAs diffusion couple, if M is the dominant diffusion species, a phase with composition near the M-GaAs connection line on the phase diagram is favored to form first. This first-nucleated phase is most likely to be a ternary compound or a solid solution phase with the crystal structure of a binary phase and extensive ternary solubility since the redistribution of components needed to form such phases is minimized. Kirkendall voids appeared in both Figs. 1(a) and 1(b), suggesting that, indeed, Co is the dominant diffusion species. Furthermore, from a pseudobinary CoGa-CoAs

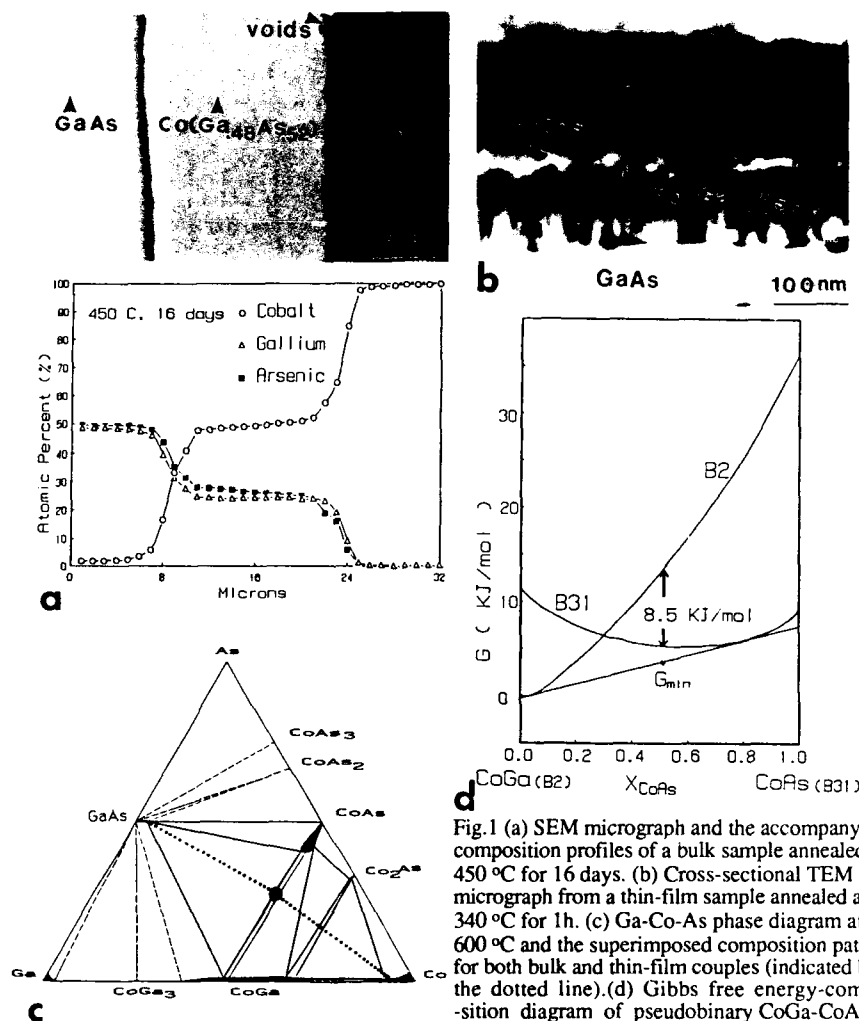


Fig. 1 (a) SEM micrograph and the accompanying composition profiles of a bulk sample annealed at 450 °C for 16 days. (b) Cross-sectional TEM micrograph from a thin-film sample annealed at 340 °C for 1h. (c) Ga-Co-As phase diagram at 600 °C and the superimposed composition path for both bulk and thin-film couples (indicated by the dotted line). (d) Gibbs free energy-composition diagram of pseudobinary CoGa-CoAs.

Gibbs free energy-composition diagram, as shown in Fig. 1(d), it is apparent that the free energy of forming a supersaturated phase with the CoAs crystal structure is only slightly higher than that of forming the equilibrium phases, but much lower than that of forming a phase with the CoGa structure. Thus, the formation of a supersaturated initial phase with the CoAs structure, $\text{Co}(\text{Ga}_{48}\text{As}_{52})$, is thermodynamically and kinetically anticipated. The phase configurations across the diffusion couples can be denoted by the dotted line shown in Fig. 1(c) using the diffusion path concept^(4,10). The paths are the same for bulk and thin-film couples at this stage.

The supersaturated phase is undoubtedly metastable. Upon annealing for longer times or at a higher temperature, decomposition would occur, lowering the overall free energy of the system to a minimum, G_{\min} as shown in Fig. 1(d).

Figure 2(a) shows an SEM micrograph and concentration profile for a bulk couple annealed at 500 °C for 10 days. In this couple, a CoGa layer scattered with CoAs has started to form near the

Co/Co(Ga₄₈As₅₂) interface. For thin-film couples annealed at 400 °C for 1 h., a complicated TEM diffraction pattern (Fig. 2(b)) indicates the coexistence of textured, untextured, and amorphous phases, meaning that the Co(Ga₄₈As₅₂) has started to decompose into CoGa and CoAs from the outer surface and that Ga has diffused outward to react with oxygen, forming an amorphous β -Ga₂O₃ layer. Thus, at this transient stage, the composition paths for the bulk and thin-film couples can be denoted by the solid and dotted lines, respectively, as seen in Fig. 2(c).

Upon annealing at 600 °C for 3-32 days, the Co(Ga₄₈As₅₂) in bulk diffusion couples decomposes completely into CoGa and CoAs, forming an eutectoid-like structure. As seen in Fig. 3(a), both CoGa and CoAs are in contact with GaAs. For thin-film couples annealed at temperatures higher than 450 °C, as demonstrated in an earlier publication⁽¹¹⁾, this eutectoid-like decomposition simply ends with CoGa and CoAs each being in contact with GaAs, rather than the formation of a layered structure. This final interface morphology is shown in Fig. 3(b). The final composition paths, i.e., diffusion paths, for bulk and thin-film couples are shown in Fig. 3(c). From the above discussion it is apparent that the phase formation sequences, interfacial morphologies, and diffusion paths are similar in both bulk and thin-film couples.

The dependence of ϕ_b^{I-V} , the ideality factor n and ϕ_b^{C-V} on annealing temperature is shown in Fig. 4. Only slight variations in ϕ_b^{I-V} , n and ϕ_b^{C-V} were observed in the samples from the as-deposited state (0.75, 1.24, and 0.87, respectively) up to 300 °C anneals (0.76, 1.2, and 0.86, respectively). These are essentially the characteristics of Co/n-GaAs contacts. The deviation of the ideality factor from 1 ($n \sim 1.2$) may be attributed to the presence of a thin native oxide layer at the Co/GaAs interface.

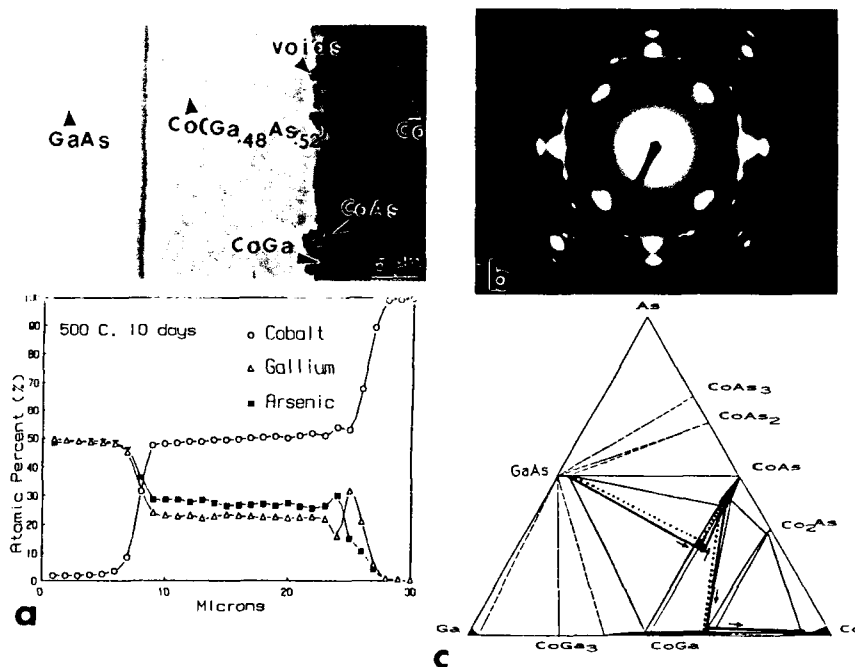


Fig. 2 (a) SEM micrograph and the accompanying composition profiles of a bulk sample annealed at 500 °C for 10 days. (b) TEM diffraction pattern from a thin-film sample annealed at 400 °C for 1 h. (c) Composition paths for both bulk and thin-film diffusion couples represented by the solid and dotted lines, respectively, on the Ga-Co-As phase diagram.

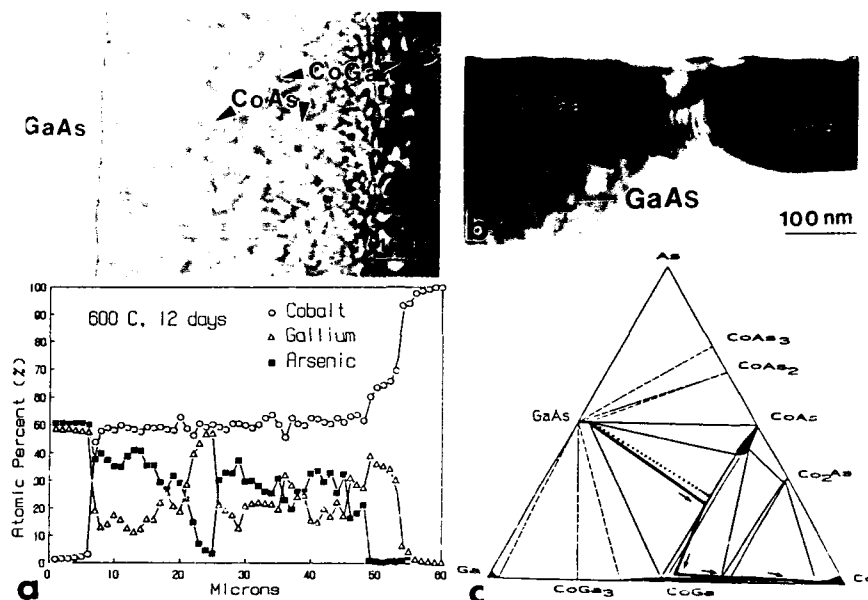


Fig. 3 (a) SEM micrograph and the accompanying composition profiles of a bulk sample annealed at 600 °C for 12 days. (b) Cross-sectional TEM micrograph of a thin-film sample annealed at 750 °C for 1h. (c) The final diffusion paths for bulk and thin-film couples denoted by the solid and dotted lines, respectively, on the phase diagram.

A decrease in barrier heights and ideality factors was observed in the temperature range of 340-400 °C. The lowest ϕ_b^{I-V} , n , and ϕ_b^{C-V} values are 0.74, 1.12, and 0.8, respectively. This may be attributed to the formation of the initial phase, $\text{Co}(\text{Ga}_{48}\text{As}_{52})$. As discussed above, the interfacial reactions are dominated by the inward diffusion of Co. Therefore, the resulting $\text{Co}(\text{Ga}_{48}\text{As}_{52})/\text{GaAs}$ interface would essentially be free from contamination. This has been verified using AES depth profiles⁽¹¹⁾. Thus, the improvement of the ideality factor is due to the elimination of the native oxide.

For the samples annealed in the temperature range of 450-600 °C, an apparent increase in ϕ_b^{I-V} and ϕ_b^{C-V} (up to 0.78 and 0.87, respectively) was observed. This is due to the decomposition of $\text{Co}(\text{Ga}_{48}\text{As}_{52})$ into CoGa and CoAs, which results in the formation of so-called "mixed phase contacts"⁽¹²⁾ or "parallel contacts"⁽¹³⁾. It should be noted that while the I-V characteristics start to degrade at temperatures higher than 600 °C, a drastic increase in ϕ_b^{C-V} has been observed for samples annealed at temperatures higher than 600 °C. Previous morphological investigations⁽¹¹⁾, have shown that better CoGa and CoAs epitaxies and uniform interfacial morphologies are obtained in samples annealed at 600-750 °C. Therefore, morphological non-uniformity is not the cause of this phenomenon. However, our phase diagram results⁽⁵⁾ show that there is a slight solubility of Co in GaAs, about 2 at.% at 600 °C. This is equivalent to a tremendous dopant concentration, $\sim 2.2 \times 10^{20} \text{ cm}^{-3}$. Co as a dopant in GaAs is known to create deep acceptor levels in the band gap^(14,15), which may act as recombination centers. The effects of recombination and trapping of electrons may play a major role in explaining the observed phenomena.

In addition, the appreciable discrepancy between ϕ_b^{I-V} and ϕ_b^{C-V} at temperatures lower than

500 °C is conjectured to be due mainly to the significant contribution of tunneling effects, since moderately doped materials were used ($2-4 \times 10^{17} \text{cm}^{-3}$ in the present case). Further analysis of the transport properties of the sintered Co/GaAs diodes is in progress.

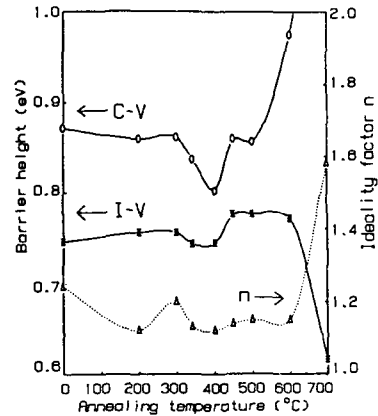


Fig. 4 The dependence of ϕ_b^{I-V} , ϕ_b^{C-V} , and n on the annealing temperature.

CONCLUSIONS

Thermodynamics and kinetics play governing roles in Co/GaAs interfacial reactions. Phase diagram and bulk diffusion couple studies provide a theoretical basis for rationalizing phase formation sequences and interfacial morphologies. The phase formation sequences, interfacial morphologies, and diffusion paths are found to be similar in bulk and thin-film couples. Thus, the thermodynamic and kinetic behavior observed in equilibrium bulk diffusion couples can be used to predict the interfacial phenomena which would appear in thin-film couples. The electrical properties of Co/GaAs contacts are closely related to the phases formed at the interfaces.

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THE GROWTH RATES OF INTERMEDIATE PHASES IN Co/Si DIFFUSION COUPLES: BULK VERSUS THIN-FILM STUDIES

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ABSTRACT

Bulk diffusion couples of Co/Si were annealed at 800, 900, 1000, 1050 and 1100 °C for periods ranging from 24 hours to one month. Growth rates of the intermediate phases, Co₂Si, CoSi and CoSi₂, as well as the composition profiles across the couples were determined by optical microscopy and electron probe microanalysis (EPMA). Using the solution to the multi-phase binary diffusion equations and the experimental data, the interdiffusion coefficients for Co₂Si, CoSi and CoSi₂ are obtained as a function of temperature. The activation energies obtained are 140, 160 and 190 KJ/mole for Co₂Si, CoSi and CoSi₂, respectively. The generally small interdiffusion coefficient of CoSi₂ and its high activation energy cause the growth rate of CoSi₂ to be extremely small at low temperatures.

The interdiffusion coefficients for Co₂Si, CoSi and CoSi₂ at 545 °C are obtained by extrapolation of the high-temperatures data. Using these data and solving numerically the diffusion equations with the appropriate boundary conditions, the growth of Co₂Si, CoSi and CoSi₂ is calculated as a function of time. The calculated results are in good agreement with the experimental data reported in the literature. This study demonstrates clearly that the initial absence of the CoSi₂ phase is due to diffusion-controlled rather than nucleation-controlled kinetics. This phenomenon may be quite common in many thin-film metal/Si couples.

1.0 INTRODUCTION

Three intermediate phases exist in the binary Co-Si system below 1170 °C. These phases are Co₂Si, CoSi and CoSi₂. In a bulk Co/Si diffusion couple subjected to a sufficiently high temperature, the three phases will grow parabolically with time. On the other hand, in thin-film Co/Si diffusion couples annealed at low temperatures, a very different behavior is observed^{1,2}. There is no initial growth of CoSi₂. Furthermore, the Co₂Si phase, after initial growth, subsequently shrinks and is eventually completely consumed. Its disappearance coincides with the appearance of CoSi, i.e., there is sequential growth of Co₂Si, CoSi and CoSi₂. Sequential growth occurring in this type of couple has been rationalized in the literature^{3,4,5} as being due to the presence of a nucleation barrier for phases such as CoSi₂. However, the absence of this phase in a thin-film Co/Si couple may not be due to the difficulty of nucleation. It may instead be the result of diffusion-controlled kinetics, in view of the relatively small interdiffusion coefficient of CoSi₂ and the limited supply of Co in the couple. The objective of this study is to calculate the growth of Co₂Si, CoSi and CoSi₂ in thin-film couples and compare the calculated results with experimental data reported in the literature. This study will demonstrate whether the initial absence of CoSi₂ is due to nucleation- or diffusion-controlled kinetics. Moreover, this approach may be extended to the study of formation and growth of intermediate phases in other thin-film diffusion couples.

In order to calculate the growth rates of the intermediate phases in thin-film couples, the interdiffusion coefficients must be known for each of the phases. Since these coefficients were unavailable for the Co-Si system, it was necessary to determine them experimentally. This was accomplished by studying high-temperature bulk Co/Si diffusion couples. Optical microscopy and electron probe microanalysis (EPMA) were used to determine interface compositions and positions and composition profiles of the intermediate phases. Multi-phase interdiffusion theory (using the semi-infinite boundary condition) was used to determine the interdiffusion coefficients. These values were then extrapolated to 545 °C and were used to calculate the growth of the intermediate phases in thin-film Co/Si couples, using multi-phase diffusion theory with the appropriate boundary conditions.

2.0 REVIEW OF MULTI-PHASE DIFFUSION THEORY

The basic quantitative formulae for the growth of intermediate phases formed in a binary diffusion couple can be found in the literature^{6,7,8}. In addition to applying Fick's first law and the equation of continuity to each intermediate phase, an interface mass balance equation must be imposed to account for the movement of the interfaces between the intermediate phases and for the growth of each phase. Thus, the following three equations are necessary to define a multi-phase interdiffusion process:

Boundary Conditions: Bulk vs. Thin-film

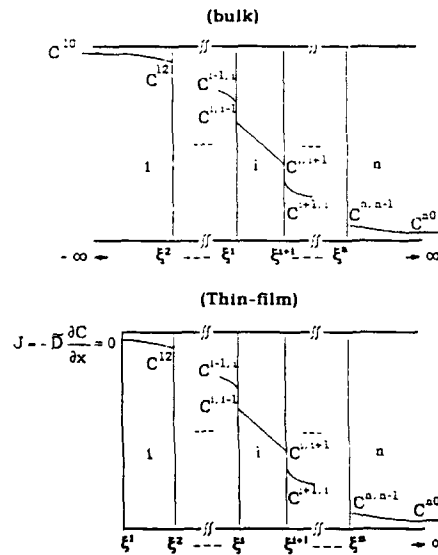


Fig. 1. Comparison of the boundary condition for bulk and thin-film cases.

zero flux, but the composition changes continuously with time. In the thin-film case, the problem is solved numerically⁹ since there is no analytical solution to the diffusion equations.

3.0 EXPERIMENT

To prepare the bulk diffusion couples, a 5 mm diameter Co rod was cut into 2 mm thicknesses. <111> oriented, n-type, single crystal Si was cut into 5x5x3mm pieces. Both materials were polished down to 0.03 μm Al₂O₃ powder, cleaned in 1:10 HCl solution and rinsed in deionized water. The oxides were removed using a 1 minute etch in 1:1 HF solution. Samples were again rinsed in deionized water and blown dry with N₂ gas. The Co and Si slices were then pressed tightly together between silica rods within silica tubes and sealed under a 15 mtorr vacuum. The bulk diffusion couples were annealed at 800, 900, 1000, 1050 and 1100 °C for 24 hours to one month. After annealing, the samples were mounted in epoxy molds, polished and examined by optical microscopy and EPMA.

$$\bar{J}^i = -D^i \frac{\partial C^i}{\partial x} \quad (1)$$

$$\frac{\partial C^i}{\partial t} = -\frac{\partial \bar{J}^i}{\partial x} \quad (2)$$

$$(C^{i,i-1} - C^{i-1,i}) \frac{d\xi^i}{dt} = (\bar{J}^{i,i-1} - \bar{J}^{i-1,i}) \quad (3)$$

where \bar{J}^i , D^i and C^i are the diffusional flux, the interdiffusion coefficient and the concentration for the i th phase, x is a

distance coordinate and ξ^i is the interface of the i th and $(i+1)$ th phases as shown in Fig. 1. For a bulk diffusion couple, the semi-infinite boundary condition can be applied, yielding the solutions given in literature^{6,7,8}. For a thin-film couple, the basic equations describing the diffusion behavior are the same. However, in the thin-film case, since the metal film is finite, the supply of the metal material is limited, and the boundary condition for the thin film differs from that of the bulk (Fig. 1). In the bulk case, the boundary conditions of a semi-infinite couple are met, i.e. the concentrations of the components remain constant with time at the surfaces of the end members, 1 and n in Fig. 1. In the thin-film case, the supply for one of the end members, i.e. the metal in the case of Co/Si is finite. The appropriate boundary condition at the surface of the metal is

4.0 RESULTS AND DISCUSSION

Optical examinations of the bulk Co/Si diffusion couples annealed at high temperatures indicate that the reaction kinetics are diffusion-controlled (Figs. 2 and 3). The parabolic growth constants are plotted as a function of $1000/T$ in Fig. 4. Using these data and the

concentration profiles across the diffusion couples, values of \tilde{D} 's for Co_2Si , CoSi and CoSi_2 were obtained (Fig. 5). As shown in Fig. 6, the calculated concentration profile of a bulk Co/Si couple annealed at 1000°C for 87 hrs is in accord with the experimental data. Values of \tilde{D} 's obtained for the three cobalt silicides are presented in Fig. 5 as a function of reciprocal temperature. Values of \tilde{D} for Co_2Si are the largest while those of \tilde{D} for CoSi_2 are the smallest. In view of the highest activation energy for CoSi_2 , its \tilde{D} value decreases much faster with decreasing temperature than those of CoSi and Co_2Si . In fact, at 500°C the value of \tilde{D} for Co_2Si is more than three orders of magnitude greater than that of CoSi_2 .

The growth of an intermediate phase is controlled not only by its own interdiffusion coefficient but also by those of its two neighboring phases. As shown in Fig. 4, the growth rate of Co_2Si is higher than that of CoSi at low temperatures. However, at about 650°C , its growth rate is lower than that of CoSi . The growth rate of CoSi_2 is the lowest but becomes much lower at lower temperatures. At about 500°C , it is about three orders of magnitude lower than those of Co_2Si and CoSi . The results shown in Figs. 4 and 5 clearly demonstrate that the rates of growth

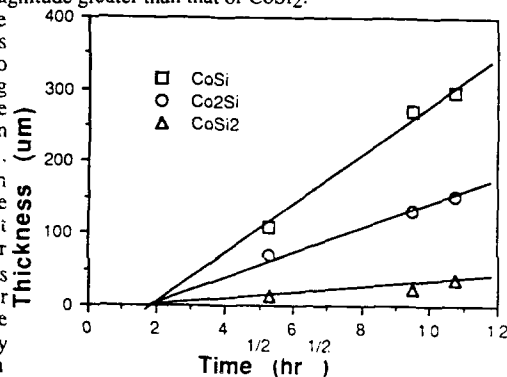


Fig. 2. Growth of the intermediate phases annealed at 1050°C .

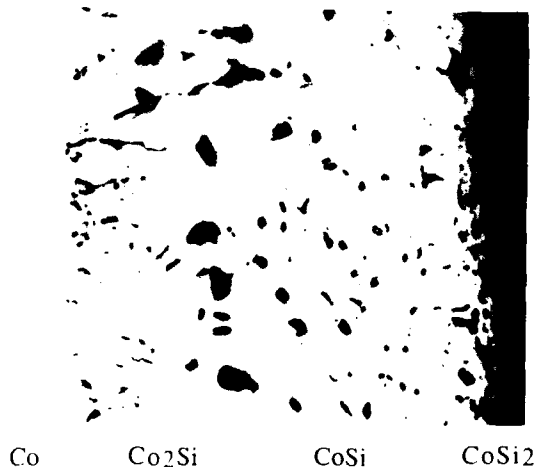


Fig. 3. Optical micrograph of a Co/Si bulk diffusion couple annealed at 1050°C for 90 hrs, 250X.

depend not only on the interdiffusion coefficient of the phase in question but also those of its two neighboring phases.

Also shown in Fig. 4 are the thin-film data of Lau et al². Within the scatter of the data, there is reasonable agreement between the two sets of data. The higher growth constant in the case of the thin-film couple is reasonable since there may be a higher concentration of grain boundaries in the thin-film couples.

Having determined the values of \tilde{D}^i for Co_2Si , CoSi and CoSi_2 at high temperatures, their values at 545 °C are obtained by extrapolation (see Fig. 5) . Using these data, the growth of Co_2Si , CoSi and CoSi_2 is obtained numerically by solving the diffusion equations with the appropriate boundary conditions as mentioned in section 2.0. The calculated results are shown in Fig. 7 as a function of $t^{1/2}$ at 545 °C. Since the data of van Gurp and Langereis¹

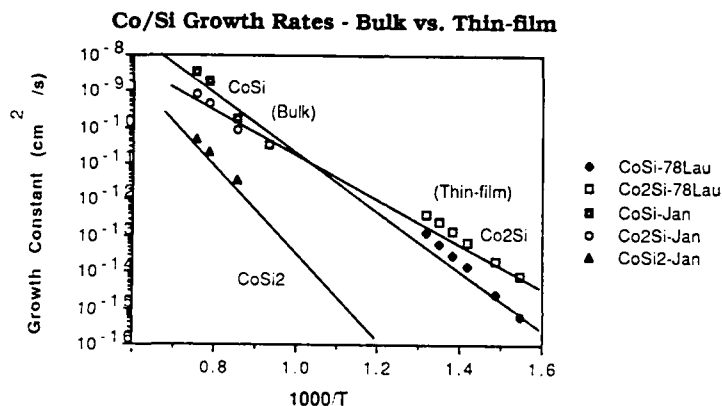


Fig. 4. Growth rates of the intermediate phases in Co/Si couples.

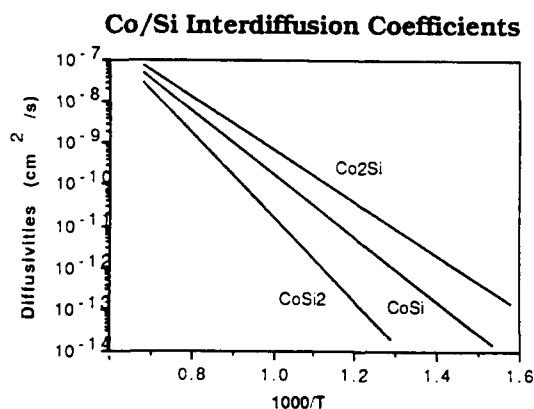


Fig. 5. Interdiffusion coefficients of the intermediate phases in Co/Si couples.

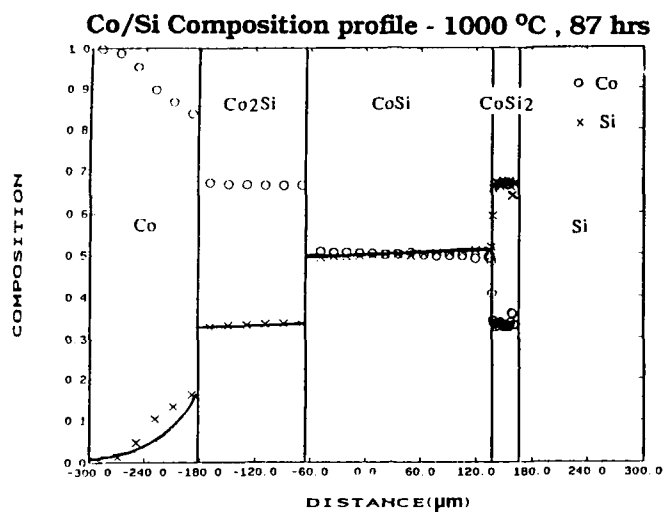


Fig. 6. Concentration profile for a bulk Co/Si diffusion couple annealed at 1000 °C for 87 hrs: comparison between experimental data and calculated values.

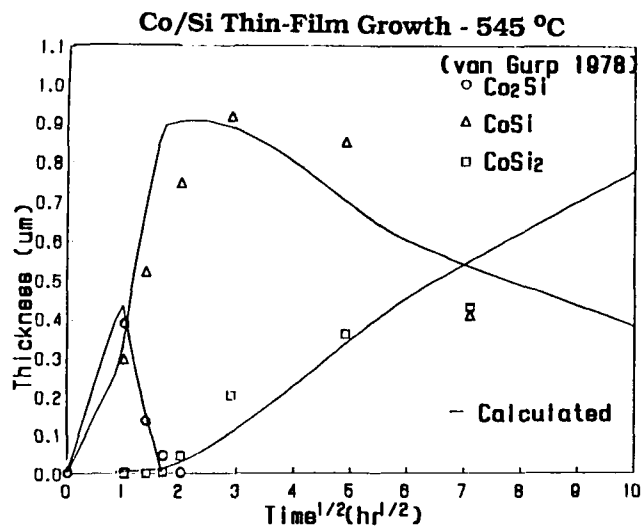


Fig. 7. Growth sequence of the intermediate phases in thin-film Co/Si couples, annealed at 545 °C; 4500 Å initial Co film.

are expressed in term of x-ray intensities, the calculated values for absolute thickness are normalized to the intensity of CoSi at $t \sim 1$ hr. As shown in the figure, the calculated growth rates of Co₂Si, CoSi and CoSi₂ are in accord with the experimental data. CoSi₂ does not grow until Co₂Si is consumed. Subsequently, the growth rate of CoSi₂ increases while that of CoSi decreases. Eventually, CoSi will be consumed, with CoSi₂ being the only remaining phase in addition to Si. The calculation shows that the amount of CoSi₂ formed initially is three orders of magnitude smaller than those of Co₂Si and CoSi.

5.0 CONCLUSION

The present study demonstrates quantitatively that the kinetics of reaction between bulk and thin-film diffusion couples of Co/Si are the same. Moreover, we believe this to be true for all diffusion couples provided the surface conditions are the same for the bulk and thin-film cases. Otherwise, the existence of extrinsic factors will affect the growth kinetics.

The sequential growth of Co₂Si, CoSi and CoSi₂ in thin-film Co/Si couples is predicted from multi-phase diffusion theory based on a knowledge of the interdiffusion coefficients for all the phases. The initial absence of CoSi₂ in the thin-film couples is due to diffusion-controlled kinetics, rather than nucleation-controlled kinetics. This phenomenon may be encountered more frequently than is commonly realized in metal/silicon thin-film couples.

We are currently carrying out bulk diffusion couple measurements of Ni/Si in order to obtain interdiffusion coefficients for the intermediate Ni-Si phases. Once we have obtained the necessary data, we will extend the same approach to calculate the growth of phases in thin-film Ni/Si couples. The calculated results will be compared with the data reported in the literature.

6.0 ACKNOWLEDGEMENTS

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INVESTIGATION OF THE INTERFACE INTEGRITY OF THE THERMALLY STABLE WN/GaAs SCHOTTKY CONTACTS

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ABSTRACT

WN_x/GaAs Schottky contacts formed by reactive sputtering were found to be thermally stable up to an annealing temperature of ~900 °C. The interface morphology and structure of this contact under high temperature annealing conditions (> 700 °C) have been investigated by transmission electron microscopy (TEM) and x-ray diffractometry techniques. For the as-deposited samples, the thin film had an amorphous structure. After annealing at high temperatures, the amorphous phase transformed to α-W and W₂N phases. However, the contact interface remained thermally stable up to 850 °C. Cross-sectional TEM micrographs revealed that annealing at temperatures above 850 °C resulted in the formation of 'pockets' beneath the interface. This phenomenon has been correlated with the electrical properties of the contacts, e. g., an enhancement of the barrier height of the contact. Comparisons between the interface morphology of this system and other refractory metal nitride contacts (e. g., TiN/GaAs) are also presented.

INTRODUCTION

One of the most important processing steps in the fabrication of GaAs MESFET's using the self-aligned technique involves ≥800 °C post-implant annealing to activate the implanted dopants in the GaAs substrate after the formation of the gate contact. A number of investigations have shown that refractory metal silicides and nitrides are excellent candidates for the thermally stable gate metals needed in the self-aligned technology due to their high thermodynamic stability and low resistivity [1]. Recently, the study by Zhang et al. [2] showed that the refractory metal nitrides (NbN, TiN and ZrN) used as Schottky gate metals are very promising not only because of their high thermal stability and low resistivity, but also because of their improved electrical characteristics after annealing at high temperatures up to 900 °C. Tungsten (W), its silicide (WSi_x) and nitride (WN_x) have also received attentions from researchers. This is especially true for tungsten nitride (WN_x), since WN_x has lower resistivity than tungsten silicide, and can be formed easily by reactive sputtering from a pure W target in Ar/N₂ atmosphere. Yu et al. [3] recently reported a systematic study on the structural and electrical characteristics of WN_x/GaAs contacts under various annealing conditions, e. g., different nitrogen content in the films, annealed with or without a capping layer, and annealed in As overpressure and a flowing N₂ ambient.

In this study, TEM and x-ray diffractometry (XRD) were used to investigate the interface structure and morphology of the WN_x/GaAs contacts. The results of this structural study are correlated with the electrical characteristics.

EXPERIMENTS

Undoped and Si-doped ($N_D = 1.5 \times 10^{17} \text{ cm}^{-3}$) GaAs wafers with (100) orientation were prepared for WN_x deposition by degreasing in organic solvents, etching in $\text{HCl:H}_2\text{O}$ solution, rinsing in de-ionized water and drying with nitrogen gas. Prior to loading into the deposition chamber, the wafers were dipped in a $\text{NH}_4\text{OH:H}_2\text{O}$ solution for 1 min. for removal of the native oxide from the GaAs surface. The WN_x films ($\sim 200 \text{ nm}$) then were deposited on the GaAs substrates by reactive dc sputtering. The total gas pressure was kept at 10 mTorr during the deposition. The relative partial pressure of nitrogen was used to control nitrogen content in the as-deposited WN_x films. In this work, the partial pressure of nitrogen was 20%.

The WN_x samples were annealed under different conditions. A set of samples were capped with an SiO_2 layer ($\sim 100 \text{ nm}$) by chemical vapor deposition. The samples were then furnace annealed (FA) at $700\text{--}850^\circ\text{C}$ for 30 min. under an As-overpressure or in flowing N_2 . Some of the capped samples were annealed at 850 , 900 and 950°C for 10 seconds in a flowing Ar ambient in a halogen lamp rapid thermal annealing (RTA) system.

Cross-sectional samples were prepared by the standard techniques for TEM investigations [4]. The study of the interface structure and morphology of the WN_x/GaAs contacts before and after RTA was performed in a Philips EM400 TEM and a JEOL 200CX TEM. A Siemens D500 x-ray diffractometer was also used to characterize the structure of the samples before and after annealing, and to confirm the TEM results on a macroscopic scale.

RESULTS AND DISCUSSIONS

The interface morphology and structure of the WN_x/GaAs contacts have been studied by TEM. Figure 1 shows the TEM images of cross-sectional samples before and after RTA at 850°C , 900°C and 950°C . For the as-deposited sample, the interface was relatively flat and no native oxide was observed. The structure of the as-deposited WN_x thin film with 20% N_2 was studied by the selected area diffraction technique. Figure 2a shows a selected area diffraction pattern for this as-deposited sample in which a $\beta\text{-W}$ amorphous ring pattern is superimposed on the $[110]$ GaAs diffraction pattern. Since this diffraction pattern was taken from the interface area where the amorphous film had a thickness of only $\sim 15 \text{ nm}$, only the strongest 210 reflection from the $\beta\text{-W}$ amorphous film is visible. $\beta\text{-W}$ has a cubic structure with a lattice parameter $a_0 = 0.5050 \text{ nm}$.

The interface morphology of the sample after RTA at 850°C is shown in Fig. 1b. The interface in this case was not flat, and there was some evidence that interface interdiffusion occurred during annealing. It is likely that some of the Ga and As atoms diffused into the WN_x film locally, and some As atoms may have diffused out along the grain boundaries in the film. RTA at 850°C resulted in a crystallization of the as-deposited amorphous film. The crystallized grains in the film have been identified to be $\alpha\text{-W}$ and W_2N by XRD and electron diffraction techniques. As can be seen in Fig. 2b, a $[\bar{1}11]$ $\alpha\text{-W}$ diffraction pattern from one $\alpha\text{-W}$ single grain is superimposed on the $[110]$ GaAs diffraction pattern. Note also that 110 $\alpha\text{-W}$ diffraction spots from another $\alpha\text{-W}$ grain shown on the left of the diffraction pattern are only a few degrees from the 111 diffraction spots of W_2N . This may indicate an epitaxial relationship between this $\alpha\text{-W}$ single grain and the W_2N grain since the lattice mismatch between the 110 $\alpha\text{-W}$ d-spacing (0.2238 nm) and the 111 W_2N d-spacing (0.2382 nm) is only 6.2%. Both $\alpha\text{-W}$

and W_2N have a cubic structure with lattice parameters 0.3165 nm and 0.4126 nm, respectively. From the x-ray and electron diffraction analysis, the majority phase in the film was α -W with a smaller amount of W_2N (20% of W_2N reported by Yu et al. [3]).

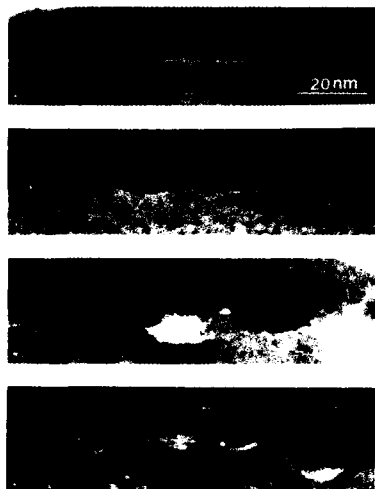


Fig.1. Transmission electron microscopy images of cross-sectional $WN_x/GaAs$ samples (a) as-deposited, (b) after RTA at 850 °C, (c) RTA at 900 °C, and (d) RTA at 950 °C.

After RTA at 900 °C, the interface of the $WN_x/GaAs$ contacts became very rough with pocket-like protrusions formed under the original interface of the $WN_x/GaAs$ contact as shown in Fig. 1c. These pockets have an amorphous-like appearance as has been observed for $TiN/GaAs$ contacts after annealing at temperatures above 800 °C [5]. The average width of the pockets is ~15 nm, and the average penetration depth of the pockets into the substrate is about 10 nm. It is expected that some W_2As_3 phase may be formed on the top of the pockets by outdiffusion of As atoms from the substrate. However, electron and x-ray diffraction results do not show any $W_{Bsub}2As_3$ patterns. This may be due to the very small amount of this phase present in the film.

RTA at 950 °C resulted in a very rough interface as shown in Fig. 1d. As shown in this figure, many more pocket-like protrusions were formed as compared with 900 °C RTA so that there is now no spacing left between them. This indicates that a significant interface interdiffusion has occurred during the 950 °C RTA. By measuring the lattice spacings from the phase at the top of these pockets in Fig. 1d, it was clear that the phase in intimate contact with GaAs was W_2N since only two phases, α -W and W_2N , were present in the thin film as indicated by electron and x-ray diffraction analysis. It is likely that both Ga and As atoms diffused along the grain boundaries in the thin film to the surface since diffusion in grain boundaries is much faster than in the bulk. Outdiffusion of Ga and As atoms apparently requires an annealing temperatures above 850 °C because the first appearance of pockets beneath the original interface was after 900 °C RTA.

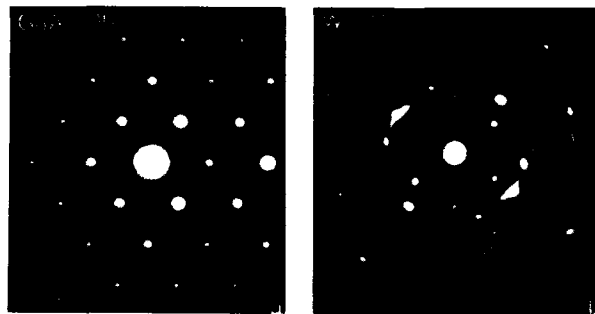


Fig.2. Electron diffraction patterns from (a) the as-deposited sample, and the sample after RTA at 850 °C.

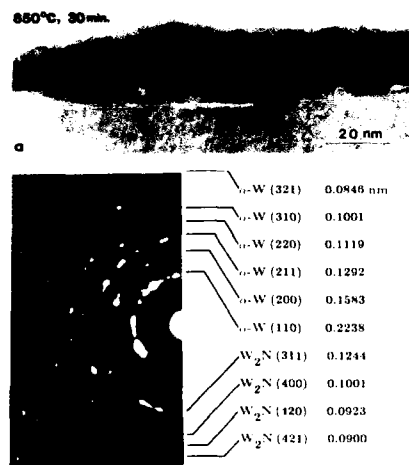


Fig.3. (a) TEM image of the capped WN_x /GaAs sample after FA at 850°C for 30 min., (b) Electron diffraction pattern from the thin film of the same sample.

For the samples subjected to FA at 850°C for 30 min. with and without SiO_2 caps, the interface morphology was almost identical with that after 850°C RTA. This implies that annealing time at 850°C is not an important variable compared to annealing temperature in determining the interface morphology. Figure 3a shows the interface morphology of the capped WN_x /GaAs sample after annealing at 850°C for 30 min. From this bright field TEM image, the interface can be seen to be similar to that of 850°C RTA annealed samples. In some regions the GaAs substrate was consumed by outdiffusion during annealing. The phase in intimate contact with the GaAs was again found to be W_2N by measuring the lattice spacings in Fig. 3a. This confirms the prediction by Yu et al. [3]. Figure 3b shows the selected area diffraction pattern taken from the film only. The rings in this diffraction pattern

were found to correspond to α -W and W_2N

phases. From the relative intensities of the diffraction rings, α -W was the major phase in the film.

Results from the TEM cross-sectional samples did not show any difference in the interface morphology between the capless samples annealed in an As overpressure and the capped sample in a flowing N_2 ambient after furnace annealing at 850°C for 30 min. XRD was also used to study the structure of WN_x /GaAs samples before and after annealing under different conditions, e. g., capped or capless, annealing in an As-overpressure or a flowing N_2 gas. Figure 4 shows the x-ray spectra from the capped (a) and capless (b) samples after annealing at 850°C in a flowing N_2 gas and an As overpressure, respectively. The spectrum from the capped sample indicates that the thin film consists of a mixture of phases, α -W and W_2N . Note that the GaAs (200) diffraction

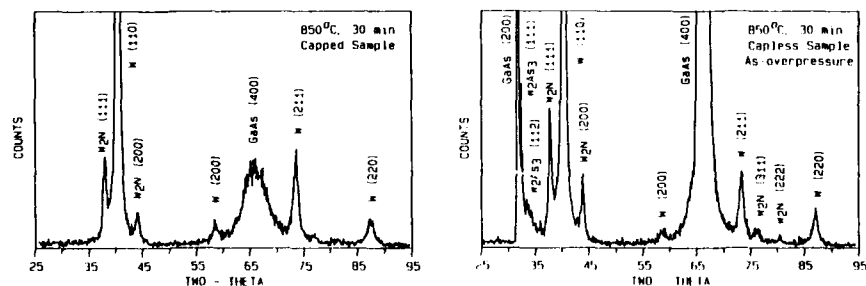


Fig.4. X-ray diffraction spectra of the samples after 850°C FA for 30 min. (a) capped, and (b) capless.

peak did not appear, and also the GaAs (400) peak has a very low intensity due probably to misorientation of the GaAs substrate from a (100) plane, or the large thickness of the film formed on the GaAs substrate. Compared to the spectrum from the capped sample, the spectrum from the capless sample shows additional peaks corresponding to W_2As_3 . Based on a previous Rutherford backscattering spectrometry (RBS) study [3], it is believed that this W_2As_3 phase was formed on the surface of the thin film by the reaction of W on the surface of the film and an As overpressure during annealing. It is also interesting to note that the diffraction intensity of W_2N in the capless sample is higher than that of in the capped sample. This is also in good agreement with the previous RBS study [3].

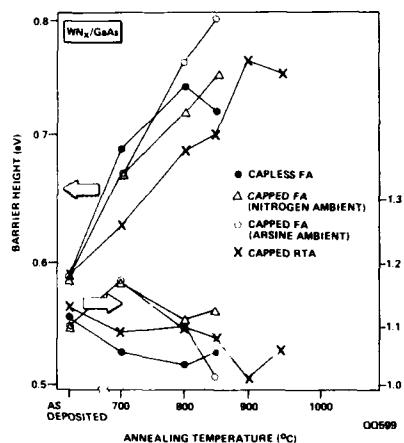


Fig.5. Plots of Φ_b and n as a function of annealing temperature under different annealing conditions for $WN_x/GaAs$ diodes.

Figure 5 shows the electrical characteristics of the $WN_x/GaAs$ contacts before and after annealing in different conditions in the temperature range of 700-850 °C for FA and 700-950 °C for RTA. Yu et al. discussed the effects of nitrogen and annealing conditions on the thermal stability and barrier height of the $WN_x/GaAs$ contacts [3]. The barrier height enhancement with annealing temperatures below 700 °C is attributed to the removal of sputtering damage and consumption of the native oxide at the interface. The reasons for the increase of the barrier height in the nitride contact systems after annealing at temperatures above 700 °C have been a subject of speculation in the literature: (1) the formation of a metal/ p^+ -GaAs/ n -GaAs contact by incorporation of nitrogen into the substrate [2]; (2) the charge states of Ga vacancies formed near the interface [3]; (3) the effective electronegativity of the phase in intimate contact with GaAs [3]. The correct explanation is still not clear.

The results of this investigation show that most of the interface is in intimate contact with W_2N after annealing, and the interface is stable up to 850 °C. It is interesting to note that the pocket-like protrusions were formed above a critical temperature 900 °C RTA as also found for the $TiN/GaAs$ contact where the first appearance of the pockets occurred after 500 °C RTA. The formation of pockets can be explained by outdiffusion of As or Ga and As. This loss of As or Ga and As can change the electronic structure, and create electrically active defects at or near the interface which might result in the barrier height enhancement. For example, it could create a p^+ -GaAs thin layer surrounding the pockets [5], or it may change the pinning position of the Fermi-level in the GaAs band gap by loss of As as discussed elsewhere [6].

In summary, the interface morphology and stability of the $WN_x/GaAs$ contacts before and after annealing at high temperatures (> 700 °C) under different conditions have been investigated by TEM and XRD analysis. The as-deposited WN_x film has been found to be β -W with an amorphous structure. Annealing at temperatures up to 850 °C

did not change the interface morphology significantly under all annealing conditions, but amorphous β -W transformed to α -W and WN_x phases, with WN_x in intimate contact with the GaAs substrate. Pocket-like protrusions beneath the original interface were observed after RTA at temperatures above 900 °C. Outdiffusion of As or Ga and As along the grain boundaries is considered to be the most likely explanation for the formation of these pockets. These pockets may be partly responsible for the enhancement of barrier height after RTA at temperatures above 850 °C.

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PHASE FORMATION IN THE Pt/InP THIN FILM SYSTEM

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ABSTRACT

InP substrates with 40nm metal films of Pt were encapsulated in SiO₂, and isochronally annealed up to 600 °C in flowing forming gas. The composition and morphology of the phases that formed were studied using x-ray diffraction, Rutherford Backscattering, and transmission electron microscopy.

Results show that the Pt/InP system begins interacting at 300 °C. TEM analysis of the 350 °C anneal shows unreacted Pt and additional polycrystalline phases, with no observed orientation relationship with the substrate. The Pt layer has been completely consumed by 400 °C, with a uniform reacted layer indicated by RBS. At high temperatures (between 500 °C and 600 °C), the reaction products are PtIn₂ and PtP₂. The two phases show a tendency for phase separation, with a higher concentration of PtP₂ at the InP/ reacted layer interface. The phosphide phase also shows a preferred orientation relationship with the substrate.

INTRODUCTION

The metal/semiconductor interface provides electrical contact with the device. These contacts must maintain appropriate electrical characteristics (Ohmic or Schottky) throughout the lifetime of the device. The characteristics are generally dependent on the phases and the morphology of the metal/semiconductor interface [1-6]. If the metal reacts with the substrate, the electrical characteristics of the device may be degraded. Reaction with the metal layer can lead to the formation of electrically active defects in the substrate, or to the formation of new interfacial phases with undesirable electrical properties [1, 2, 3]. If extensive chemical reaction occurs, the definition of the contact dimensions will be difficult to maintain, which is critical for integrated semiconductor devices. A rough interface results in uneven penetration into the substrate, and an unpredictable contact depth [7].

In order to obtain the desired electrical properties of a metal/semiconductor contact, an understanding of the metallurgical behavior of the system is essential. If the metallurgical behavior of the system is known, then the electrical properties of the system can be better controlled. For example, direct deposition of metal-III compounds that are stable in contact with the III-V substrate may inhibit undesirable reactions with the semiconductor [8, 9]. For other systems, annealing may initiate reactions which lead to desirable microstructures [5]. The ideal metal/semiconductor system will be stable at both the fabrication and operation temperatures, or will react to give the most desirable end products and microstructure [9].

Currently, GaAs is the most widely used binary III-V compound, and its interactions with various metal contacts have been extensively investigated [6]. InP is not common as a binary material, although indium and phosphorous are important components of more complex systems. Their interactions with metal contacts have only begun to be studied [10].

The Pt-InP system is the subject of this investigation. Binary phase diagrams (e.g. Pt-In and Pt-P) do not fully describe the nature of possible reaction products in these systems. This study will provide information on the interactions of these III-V elements with Pt overlayers. Using this information, extrapolation to ternary and quaternary III-V materials (e.g. GaInP, GaInAs, and GaInAsP) may be possible.

EXPERIMENT

(100) InP substrates were degreased, etched in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (5:1:1), rinsed in deionized H_2O , and blown dry in N_2 . The Pt overlayers were produced by electron-beam evaporating 40nm of Pt onto the InP substrates. They were encapsulated with SiO_2 prior to annealing to inhibit outgassing of phosphorus. The specimens were heat treated in an (95:5) $\text{Ar}:\text{H}_2$ atmosphere using various annealing schedules, ranging from 200 °C to 600 °C, and from 30 to 60 minutes. 600 °C was chosen as the upper bound for annealing, as decomposition of the compound semiconductor substrate is difficult to control at higher temperatures. The SiO_2 caps were removed with a (10:1) distilled H_2O :buffered HF solution.

The specimens were examined by a combination of X-Ray Diffraction (XRD) using a Siemens Kristalloflex Diffractometer (Cu K α), Rutherford Backscattering Spectrometry (RBS) using a 1.95MeV $^4\text{He}^+$ beam, and Transmission Electron Microscopy (TEM) using Philips 301 and 400 microscopes operating at 100kV.

RESULTS

Pt/GaAs

For comparative purposes, this section summarizes the work of previous investigations on the Pt/GaAs system. Pt begins reacting with the GaAs substrate at $\sim 250^\circ\text{C}$ [11], with an intermediate phase distribution of Pt, Pt_3Ga , PtAs_2 , and GaAs [12]. After annealing at higher temperatures ($>400^\circ\text{C}$, 10-20 minutes), the phase distribution is PtGa, PtAs_2 , and GaAs [11-13]. This phase distribution is also reached for lower temperature, long term anneals (350 °C, 20 hours) [13]. The PtAs_2 phase exhibits a preferred orientation relationship with the substrate [13]. Both PtAs_2 and GaAs are cubic structures, with a lattice mismatch of 1.8%; these values are within an acceptable range for a textured or epitaxial relationship [13]. Further annealing leads to a coarsening of the preferred grains, and a roughening of the $\text{PtAs}_2/\text{GaAs}$ interface [14].

Pt/InP

X-ray diffraction indicates that by 500 °C, the reaction is essentially complete, with little change evident for 550 °C and 600 °C anneals. The XRD spectra for these temperatures match the standard powder diffraction spectrum for PtIn_2 ; the extra peaks

can be accounted for by PtP_2 (figure 1).

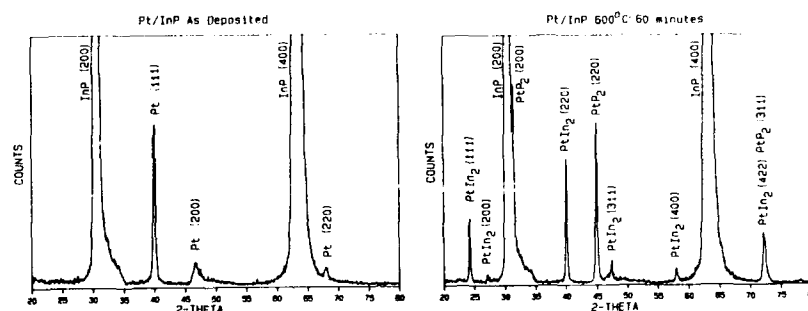


Figure 1. X-ray diffraction spectra for Pt/InP, as-deposited and 600 °C 60 minute anneal.

Rutherford backscattering spectra from these samples indicated that there was some reaction between the Pt and InP for the 300 °C anneal, and that substantial reaction occurred by 350 °C, with approximately 26nm of InP consumed. By 400 °C, the Pt layer had been completely consumed, as indicated by a homogeneous distribution of Pt, In, and P in the reacted layer (figure 2). At temperatures above 500 °C, the ratio of the Pt reacted to InP approaches 1:1, as would be expected for a combination of PtIn_2 and PtP_2 .

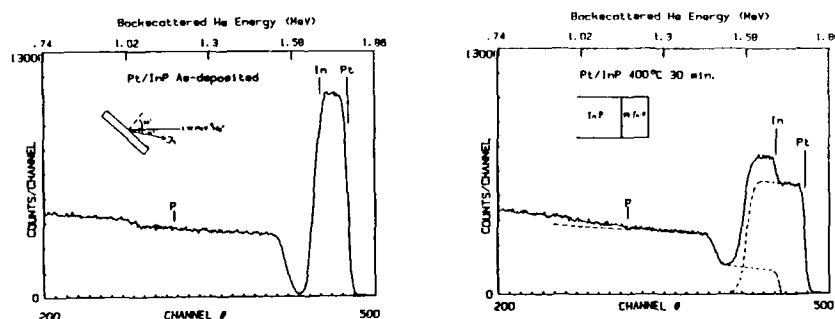


Figure 2. RBS spectra of Pt/InP, as-deposited and 400 °C 30 minute anneal.

TEM studies after the 350 °C anneal showed a polycrystalline microstructure with an average grain-size of 10nm, as compared to 20nm for the as-deposited Pt layer (figure 3). Electron diffraction indicated the presence of unreacted Pt and additional

polycrystalline phases. In the 400 °C specimen, TEM showed a polycrystalline microstructure, with some large lath-like grains (20nm by 200nm) in a textured polycrystalline matrix. Identification of the phases present is in progress.

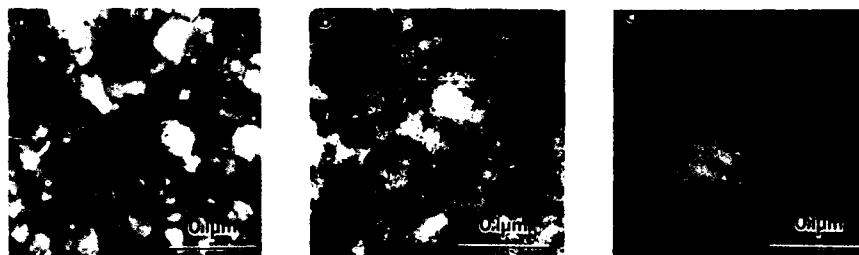


Figure 3: TEM micrographs of plan-view Pt/InP specimens. a) as deposited, b) 350 °C, c) 400 °C:30 minutes.

The XRD results for the 550 °C, 30 minute anneal were corroborated by TEM studies. Microdiffraction patterns confirm the presence of PtP₂ grains. The reacted layer has a coarse-grained, polycrystalline microstructure, with a grain size on the order of 50nm to 70nm (figure 4). The interface with the InP substrate is rough. Selected area diffraction of the 550 °C specimen showed that the PtP₂ phase exhibits a preferred orientation relationship with the substrate. TEM studies of these samples are continuing to determine the morphology of the PtIn₂ phase.



figure 4: TEM micrograph of cross-sectional Pt/InP specimen, 550 °C:30 minute anneal.

DISCUSSION

Both the RBS and XRD results for the Pt/InP system indicate that the reactions for this system can be divided into three stages: initial reaction- 300 °C to 350 °C; intermediate stage- 375 °C to 400 °C; and, final stage- 500 °C to 600 °C. At low temperature, InP and Pt react to form polycrystalline phases with no observed preferred

orientation. During the intermediate stage, all three components of the system become intermingled, forming a polycrystalline phase with a preferred orientation with the substrate, and a coarse-grained second phase.

One of the goals in studying the annealing behavior of the Pt/InP system was to determine the stable compounds and their morphology for high-temperature anneals. The stable phases in this system, for the annealing conditions between 500 °C and 600 °C, are PtP_2 and PtIn_2 (figure 5). For this temperature range, the reacted layer has a coarse grained, polycrystalline microstructure, with a grain size between one third to one half the reacted layer thickness. The phosphide layer exhibits a preferred orientation relationship with the InP substrate. Both PtP_2 and InP are cubic structures, with a lattice mismatch of 3%.

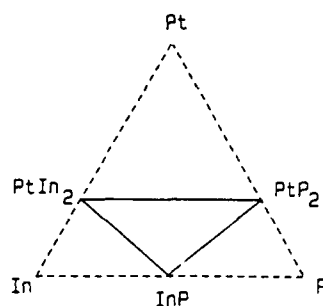


Figure 5. Stable tie-triangle indicated by the results for anneals between 500 °C and 600 °C.

In summary, the Pt/InP and Pt/GaAs systems show similar features after annealing. Both ultimately form layered microstructures, with a Pt-III compound concentrated at the surface, and an intervening Pt-V compound near the substrate. In both cases, the Pt-V compound has a preferred orientation relationship with the substrate. Pt/GaAs begins interacting at a lower temperature (250 °C vs. 300 °C) than does Pt/InP, and attains the final, stable phases earlier (400 °C vs. 500 °C) for similar annealing times and film thicknesses. Additionally, the Pt-Ga and Pt-As phases show a tendency for phase segregation even for the initial reactions, while at intermediate temperatures, the Pt, In and P are completely intermingled.

The phase segregation behavior of these systems indicates which of the elements is the dominant diffusing species. In the case of Pt/GaAs, both Pt and Ga are mobile from low temperature; Ga diffuses into the Pt to form Pt-rich compounds, while Pt diffuses into the substrate to form PtAs_2 . The behavior of the Pt/InP system, however, indicates two different stages of atomic mobility: at low to intermediate temperatures, only Pt can diffuse readily, while at higher temperatures, both Pt and In are diffusing. In the first stage, the Pt diffuses into the substrate to form an intermixed layer, while at the higher temperatures, the In diffuses out into the Pt, resulting in phase segregation similar to Pt/GaAs.

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COMPARISON OF Pd/InP AND Pd/GaAs THIN-FILM SYSTEMS FOR DEVICE METALLIZATION

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ABSTRACT

Results of the interaction of 40-nm Pd films on chemically-cleaned InP substrates at temperatures from 175 to 650°C are reported. Comparisons are made with previous results from studies of Pd thin-films on GaAs. For both systems, the reaction began upon deposition of the metal. Ternary phases were found after annealing at temperatures up to 250°C. At 450°C and higher, the PdIn or PdGa phase was dominant because of loss of volatile P or As. Possibilities for making ohmic contacts based on these systems are discussed.

INTRODUCTION

For III-V semiconductor devices, standard metal contacts are based on Au-Ge eutectic materials. Ohmic properties are achieved by heating the films to the eutectic temperature, thus forming the contact by a liquid phase dissolution and growth process. The morphology of these contacts is very rough and irregular, often with deep protrusions into the underlying semiconductor. Furthermore, the metallurgy of systems with four or more components is quite complicated and not well understood. Knowing the nature of the interactions in relatively simple metal-III-V (M-A-B) ternary systems or M-AB pseudo-binary systems is a good first step toward understanding more complicated metallization schemes. At present, phase formation data on these systems are scarce. This study focuses on Pd/InP thin-film interactions, examining the phases that form as a function of temperature, determining their morphologies, and comparing these results to existing data from the Pd/GaAs system.

EXPERIMENTAL PROCEDURE

Sulphur-doped n^+ ($n = 5 \times 10^{18} \text{ cm}^{-3}$) InP wafers in [100] orientation were degreased, etched in $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (5:1:1) for 2 min, rinsed in deionized water, and blown dry with N_2 . Palladium was deposited to a thickness of 40-nm by electron beam evaporation in a vacuum of 10^{-6} Torr. Samples were annealed for 30 min in flowing forming gas (95% Ar - 5% H_2) at temperatures from 175 to 650°C. Samples to be annealed at 250°C and higher were capped first on both sides with a 200-nm SiO_2 layer formed by plasma-enhanced chemical vapor deposition. It is estimated that the sample temperature did not exceed 200°C during this step. The results reported were obtained by transmission electron microscopy (TEM) using a Philips 400 electron microscope operated at 100 kV. Specimens for TEM were prepared in plan view by chemical-thinning from the back side of the wafer with a chlorine

- methanol solution. Cross-section specimens were dimpled to about 5 μm thickness with a South Bay Technology Model 515 dimpler. Final thinning was done in a Gatan ion mill operated at 2.5 kV with Ar^+ ions at an angle of 11.5° and a total beam current of 0.5 mA.

RESULTS

Low Temperature Reactions

Diffusion of Pd into the InP had begun upon deposition. Curing of the epoxy used to bond the cross-section specimen of this material required heating to 100°C for 30 min. A TEM image of this specimen is shown in Figure 1. There is a smooth, continuous, 15-nm amorphous layer between the unreacted Pd and the InP substrate. The reacted layer must have grown as a result of the heating, but Auger electron spectroscopy confirmed the presence of an interdiffused layer in the as-deposited sample.¹

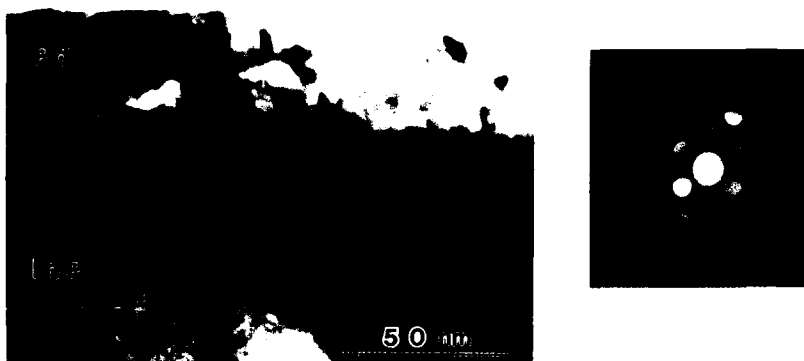


Figure 1 Cross-sectional TEM image of Pd/InP sample as received. Reaction between the metal and substrate has begun with formation of an amorphous phase.

Annealing at 175°C for 30 min resulted in a continuous film with amorphous character as shown in Figure 2. The edge of the film still in contact with the InP substrate had recrystallized in a continuous band about 1 μm wide with a grain size of about 60-70 nm. These regions yielded polycrystalline diffraction patterns with strong texture. The strongest reflections were indexed as the tetragonal phase, Pd_5InP , previously reported by El-Boragy and Schubert² as $\text{Pd}_{72}\text{In}_{14}\text{P}_{14}$ with lattice parameters, $a = 0.3928 \text{ nm}$, $c = 0.6917 \text{ nm}$. The morphology of this phase indicates that the amorphous to crystalline transformation was limited by nucleation. The transformation occurred only in those areas in contact with the InP substrate. After annealing at 250°C , crystallization of the reacted layer was complete. Three orientations of the Pd_5InP phase were found.

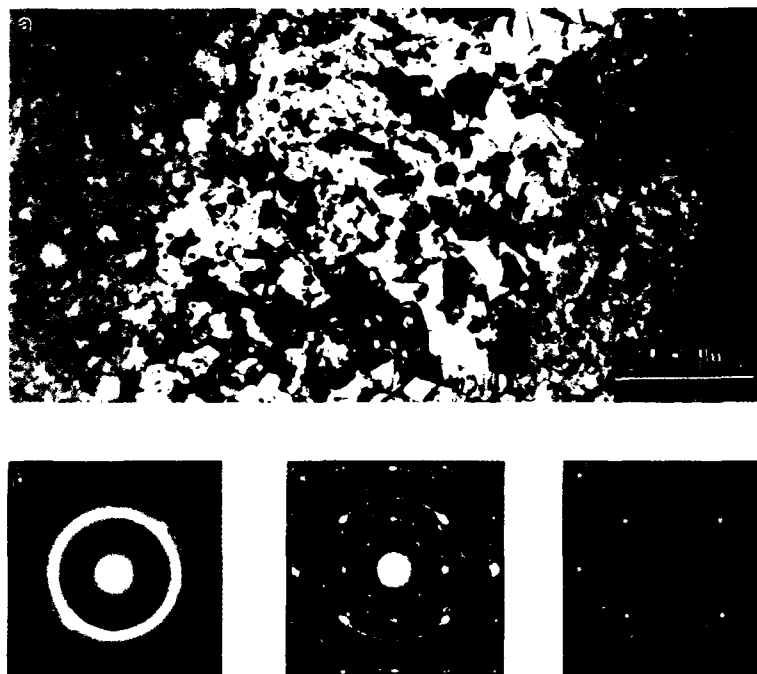


Figure 2 (a) Plan-view TEM micrograph of a Pd/InP sample after annealing at 175°C for 30 min. The thickness of the sample increases from left to right. Selected area diffraction patterns showing that (b) most of the film is amorphous and that (c) the region in contact with the substrate has transformed into poly-crystalline Pd₅InP with a preferred orientation to (d) the InP substrate.

High Temperature Reactions

After annealing at temperatures from 450 to 650°C, the reacted layer had agglomerated into islands, with the largest ones ranging in size from 200 (450°C) to 600 (650°C) nm. Diffraction patterns from the 650°C sample showed PdIn reflections with two dominant orientations.

Figure 3 shows the image of the 650°C material viewed in cross-section. The InP interface is very rough on a scale of about 60 nm. The large dark areas are PdIn. There are voids and regions of low density amorphous material between the PdIn islands and, in some areas, also separating the islands from the substrate. In other areas the PdIn islands are in direct contact with the InP. Microdiffraction revealed interatomic distances of about 0.231 and 0.130 nm for the amorphous phase. These agree well with InPO₄. Additional details about Pd/InP phase formation can be found in Reference 1.

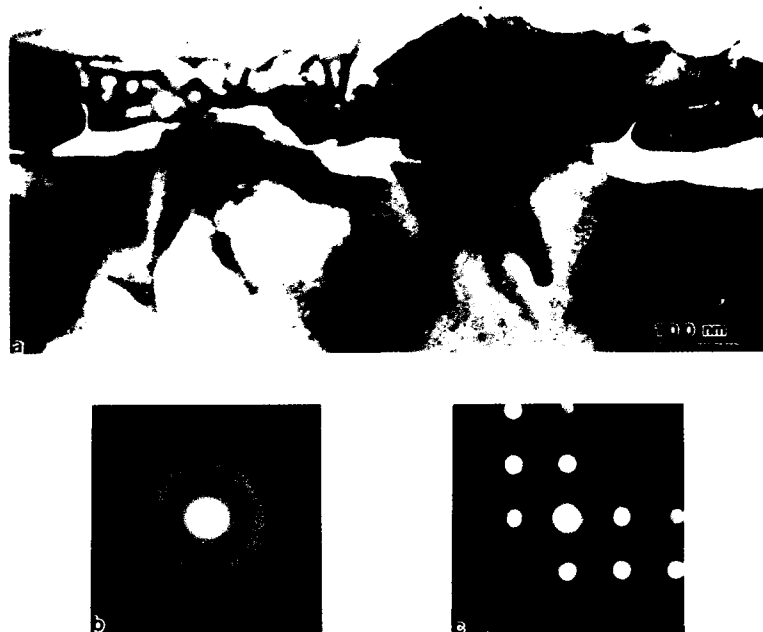


Figure 3 Pd/InP annealed at 650°C for 30 min shown in cross section (a). Microdiffraction reveals that the regions with many voids are amorphous (b) and that the darker regions are PdIn (c).

DISCUSSION

Comparisons between Pd/InP and Pd/GaAs

The phase formation sequences for the Pd/InP and Pd/GaAs systems are summarized in Table I. Upon deposition, both form ternary phases in spite of the native oxide layer on the substrate. For Pd/GaAs, this phase has hexagonal structure and nominal composition Pd_xGaAs , $2.5 < x < 4$.^{3,4} For Pd/InP, the as-deposited phase is amorphous with a similar Pd concentration ($\text{Pd}_{4.8}\text{InP}$). After annealing at 250°C, Pd_xGaAs transforms to another ternary phase, Pd_4GaAs , with a different hexagonal structure.⁴ For Pd/InP, the amorphous ternary phase crystallizes into tetragonal Pd_5InP at 250°C.

Uncapped Pd/GaAs samples, annealed at temperatures approaching 500°C in either vacuum or forming gas contained only PdGa in the reacted region because of sublimation of the As.^{3,5} For samples capped with SiO_2 , As-containing phases were also observed at temperatures as high as 600°C.⁵ Very thin Pd films (12 nm) annealed at 600°C resulted in a reacted layer comprising single-grain islands of Pd_4GaAs .⁵ Thicker Pd films (60 nm), annealed at 500°C, yielded both PdGa and PdAs₂ phases.⁵ For Pd/InP samples with a 40 nm Pd layer, annealed at 450 - 650°C in forming gas, we found islands of PdIn interspersed with InPO_4 , indicating sublimation of P in spite of the cap.

TABLE I
Summary of Pd/InP and Pd/GaAs Reactions

<u>Temperature</u>	<u>Pd (40 nm)/InP</u>	<u>Pd (50 nm)/GaAs</u>
As-Deposited	Pd _x InP (amorphous)	Pd _x GaAs (Phase I) (hexagonal)
250°C	Pd ₅ InP	Pd ₄ GaAs (Phase II) and some remaining Phase I
300°C		Pd ₂ Ga and PdAs ₂
450°C and higher	PdIn, InPO ₄ , and voids	PdGa and voids

Possibilities for Ohmic Contacts

Marshall, et al.⁶ and Sands, et al.⁷ have made ohmic contacts with good metallurgical properties based on two-stage annealing of the layered structure: Si (or Ge)/M/AB. They have described a process by which M-AB reactions at low temperatures produce an intermediate M_xAB phase. Subsequent annealing at higher temperatures causes decomposition of the intermediate phase, epitaxial regrowth of AB, and formation of M-Si (or M-Ge) phases. Experiments with the Ge/Pd/GaAs⁶ and Si/Pd/GaAs⁸ systems have yielded ohmic contacts with low resistance after processing at temperatures as low as 375°C. The contacts were laterally uniform with a penetration depth on the order of 10 nm.

Preliminary results on a Ge/Pd/InP metallization⁹ show some similarities to the reactions described above. After the first-stage annealing at 180°C, a continuous, amorphous, ternary Pd_xInP layer was formed. After deposition of Ge and further annealing at 205 and 325°C, the amorphous phase decomposed, and a layered structure was formed as shown in Figure 4. The results suggest that epitaxial regrowth of InP may have occurred. Further studies are underway to confirm these results, test the stability of this structure, and determine the electrical characteristics of the contact. It is interesting to note that Chen, et al.¹⁰ have reported good ohmic properties ($\rho = 1.27 \times 10^{-5} \Omega\text{-cm}^2$) and thermal stability for Ge/Pd/InP metallizations annealed at 300 to 500 °C.

CONCLUSIONS

Upon deposition, Pd reacts readily with both InP and GaAs substrates, easily penetrating the native oxide layer.

Thin-film Pd/InP and Pd/GaAs systems have similar phase-formation sequences, beginning with ternary phases at low temperatures.

At high temperatures, loss of P or As is difficult to prevent. The reacted layer contains the binary phases, PdIn or PdGa.

Formation of ternary phases with equal amounts of Group III and Group V elements at low temperatures make the Pd/InP and Pd/GaAs systems both good candidates for formation of ohmic contacts by a two-stage solid-phase epitaxial regrowth reaction.

ACKNOWLEDGEMENTS

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PART II

Metal/Semiconductor
Heterostructures II

A KINETIC PHASE DIAGRAM FOR ULTRATHIN FILM Ni/Si(111): AUGER LINESHAPE RESULTS

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ABSTRACT

We have used Auger spectroscopy to monitor chemical reactions during solid phase epitaxy by contact reaction in the Ni/Si(111) ultrathin film system. We show that coexisting phases may be separated by numerically fitting the composite Si LVV lineshape using a linear combination of single phase "fingerprint" spectra. Systematic measurements of coverage and temperature conditions are compiled into a kinetic phase diagram. Comparison with conventional (1000Å) thin film data suggest that the reactions forming Ni_2Si and NiSi at $> 20 \text{ Å}$ thickness are bulk diffusion limited, while surface diffusion dominates at lower coverage. On the other hand, the formation of NiSi_2 appears to be nucleation limited at all coverages, with dramatic variations in reaction rate with film thickness. This is discussed in terms of a competition between surface and bulk free energies.

BACKGROUND

Solid phase epitaxy (SPE) by contact reaction in metal/semiconductor films is a topic of considerable technological and scientific importance. SPE is commonly employed for metallization processes and in the formation of Schottky barrier and ohmic contacts [1,2]. A great deal is known empirically about this process, yet relatively little of predictive value has been established; quantitative models of kinetic processes are lacking. The thermodynamic description of such a system is straightforward: the absolute minimum in free energy corresponds to a dilute solution of metal in the substrate, while there exist also in most cases, several local minima corresponding to stable compounds usually with narrow stoichiometry limits. The sequence of phases that form during thermal annealing is entirely determined by kinetic processes [3,4]. These are generally classified as "diffusion" or "interface reaction" processes depending on which is rate limiting. If diffusion is rate limiting, then the sequence of phases formed in a binary couple is a regular progression of metal poorer compounds, with essentially all stable compounds appearing in the sequence [5]. However, if interface reactions are rate limiting, stoichiometries may be skipped. Diffusion processes are well characterized in thin film reactions but "interface reaction" processes are not. This is because the latter, which are typically nucleation rate limited, are exceedingly sensitive to structure and chemical properties of the interface on the atomic scale [6,7], and this information is not readily obtainable with conventional thin film techniques such as Rutherford Backscattering.

The above describes the motivation for studying reactions in ultrathin ($<50\text{\AA}$) silicide films. For such thin overlayers, the interface is physically exposed for scrutiny with a variety of surface sensitive probes with submonolayer sensitivity, such as Auger, photoemission, electron diffraction, etc. A related subtle point is that the interface reactions become *kinetically isolated*, by which we mean that diffusion processes become exceedingly fast when surface or other "short circuit" paths are available, as will be described in this article. Thus the temperature and structural dependencies of interface reactions may be studied directly.

Silicides are exemplary model systems in which one can isolate electronic or structural parameters of interest. As such they have been widely studied, especially nickel and cobalt silicides which can be grown as truly single crystal overlayers [8]. Unfortunately, the nature of reactions, even in the heavily studied Ni/Si(111) ultrathin film system, remains poorly understood. For example, the structure formed at room temperature and low coverage ($<10\text{\AA}$) remains contentious, with claims of NiSi_2 using Surface EXAFS [9], transmission high energy electron diffraction (THEED) [10] or low energy ion backscattering (ICISS) [11]; or NiSi using XPS [12]; or Ni_2Si using RBS [13] or RHEED [14]. The picture becomes even more confused if one includes annealing and other preparation variables. We mention two generic difficulties in conducting experiments of this nature. First, there are in general multiple coexisting phases during annealing, and unless the technique(s) used can quantitatively separate these, ambiguity will result. Secondly, there are multiple variables such as film thickness, time, and temperature as well as reaction path dependencies that affect the structures formed. These variables must be systematically explored or controlled in order to get a coherent picture of the reaction process.

METHOD AND RESULTS

The Si(111) substrate was cleaned with a methanol rinse then heated in-situ to 1250°C for about 1 minute, after which the Auger spectrum showed a C/Si ratio of $< 0.2\%$. Nickel was deposited at a rate of $4\text{\AA}/\text{minute}$ from a foil heated by electron bombardment. Thickness of metal deposited was calibrated using Ni/Si peak heights cross-referenced to RBS data performed under identical conditions [13]. Auger signals were measured as $E^*N(E)$ spectra using a floating electrometer to record the output of a single pass CMA analyser. The excitation source was a coaxial electron gun operated at 2.5 kV and $\sim 2\text{mA}$ current. For all these experiments, nickel was deposited at room temperature, followed by annealing for 3 minutes in steps of 75° , and cooling for measurement. RHEED patterns were recorded essentially simultaneously with the Auger lineshapes. A portion of these results has been described previously, but here we emphasize the Auger data and present a coverage vs. temperature kinetic phase diagram [15].

We first measured the Ni/Si peak height ratio during uptake and annealing. From the relatively slow attenuation of the Si substrate signal during room temperature deposition of 0 to 12 Å coverage, it was inferred that either islands are growing or a reaction was taking place. Above this coverage, the growth mode changed, as signified by a more rapid attenuation. During annealing the Ni/Si ratio first fell dramatically near 150 C, then fell more slowly at higher temperatures with no pronounced plateaus that might signify single phase structures. This is understood to result from multiple coexisting phases, as described in the introduction.

The coexisting phases may be separated by examining the Si LVV Auger lineshape. We note that Auger lineshape spectroscopy is more useful than photoemission for the problem at hand since the latter tends to emphasize the nickel derived d-band states, while the Auger measurement is very sensitive to changes in s-p bonding and ignores the nickel d-bands. On the other hand, calculations of the two-hole CVV spectra are quite complicated and are not readily compared with measured data, at least for highly correlated systems [16]. We bypass this problem by fitting the data with linear combinations of measured "fingerprint" spectra. In doing so, most of the difficulties of "quantitative" Auger measurement, such as inelastic scattering, variable backscattering factor, detector resolution, etc. are avoided [17]. The single phase reference compounds are prepared and identified in-situ by analysis of their RHEED patterns and by requiring that the spectra be invariant over a large range of coverage and temperature.

A typical $dN(E)/dE$ spectrum is shown in Fig. 1. This corresponds to a 2 Å deposition annealed to 570 C, which results in islands of B-type NiSi_2 surrounded by clean Si substrate, as has been observed with RBS under similar conditions [18]. The 4 fitting parameters are the amplitudes of the Ni_2Si , NiSi , NiSi_2 and clean Si reference spectra. An iterative non-linear least squares fitting procedure contained within the ASYST programming language was used to find a best fit, as measured by the rms residuals, which are plotted in the lower panel of Fig. 1. A typical peak value of the residuals is ~ 2% of the measured peak intensity. The best fit fractional amplitudes in this case were $\text{Si} = 0.55$ and $\text{NiSi}_2 = 0.45$. The sum of fractional amplitudes is not constrained and generally lies within 10% of unity, which gives some assurance that the fitting process is working.

Fig. 2 (top panel) shows the fractional weights of the silicides during annealing of a 4 Å overlayer. At 200 C the surface is an essentially contiguous layer of Ni_2Si . The RHEED pattern is diffuse. This transforms into B-type NiSi_2 at ~ 400 C. In addition, NiSi appears in a narrow temperature range near 320 C.

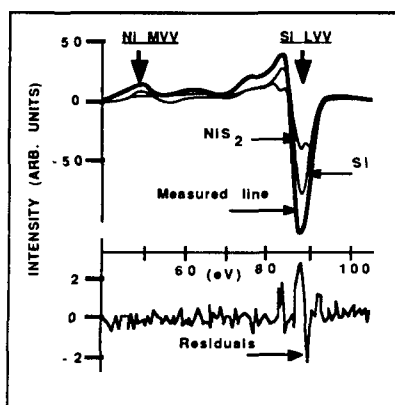


Figure 1. Auger $dN(E)/dE$ lineshape for a 2 Å deposition annealed to 560 C. The two fingerprint spectra (Si and NiSi₂) are shown with their respective fractional weights of 0.45 and 0.55, together with the measured line. Residuals (measured minus fingerprint spectra) are shown in the lower panel.

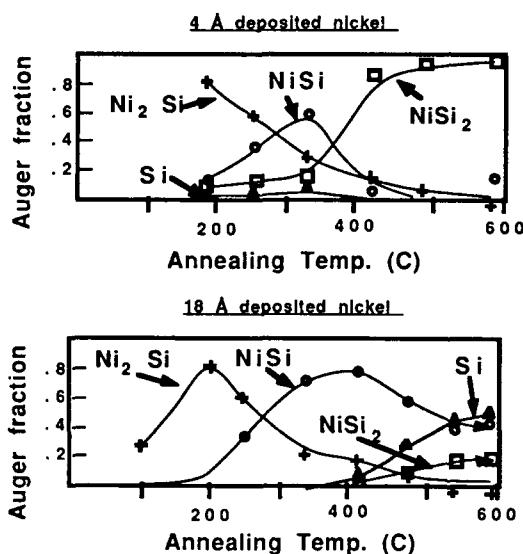


Figure 2. Auger annealing curves for 4 Å (top panel) and 18 Å depositions (bottom panel) showing the fractional weights of Ni₂Si, NiSi, NiSi₂ and Si after 3 minute anneals at the temperatures shown.

Fig. 2 (bottom panel) shows the results of annealing a 18 Å overlayer. At 100 C the surface is predominantly Ni, as indicated by the attenuation of all silicon Auger signals. The RHEED pattern shows 3D islands of nickel with a grain size of ~ 15 Å. At 200 C the Auger signal is mostly Ni₂Si, and the RHEED pattern shows 3D islands of Ni₂Si- δ . From 300 to 500 C the Auger signal is mostly NiSi and the RHEED pattern is

diffuse. For $T > 500$ C the Auger signal is mostly Si and NiSi_2 , and the RHEED pattern shows A-type NiSi_2 .

A few comments on these results in context of other experiments is appropriate. First, our observation of Ni_2Si formation at room temperature agrees with recent RBS experiments [18], but disagrees with recent THEED experiments [10]. We suggest that Ni_2Si may not be visible in the latter case, due either to beam irradiation effects or to the fine dispersion (small grain size) of the Ni_2Si , whose diffuse scattering might be invisible compared to the large thermal diffuse and inelastic background from transmission through the substrate. Secondly, we believe the Si Auger signal at high coverage and high temperature corresponds to an ordered epitaxial "cap". Similar effects have been seen previously in other silicide systems [19,20]. It is interesting that this appears not to occur for the B-type NiSi_2 . We speculate that it is kinetically prevented due to the perfect isolation of the surface from the substrate for certain coverages of NiSi_2 .

Lastly, regarding the NiSi Auger signal for the 18 Å overlayer, we believe that it is probably representative of the volume of the overlayer (even though Auger probes only the surface layers) since it exists over a rather large range of temperature that coincides with results from conventional thin film experiments. For thinner films (~ 4 Å) the temperature range over which NiSi is seen is much smaller. We believe in this case the Auger signal may represent only the surface stoichiometry or even be an artifact of the fitting procedure, since the NiSi spectrum very closely resembles a linear combination of Ni_2Si and NiSi_2 .

KINETIC PHASE DIAGRAM

The kinetic phase diagram resulting from the Auger lineshape measurements is shown in Fig. 3. The boundaries between phases is drawn at the points where a given Auger component reaches 0.5 in fractional weight. This is not an equilibrium phase diagram; All structures are retained upon cooling. This diagram is understood to represent the chemical state of the surface layers of the thin film, while the volume of the film may be different, as described above. For example, the Ni region clearly represents a layer of nickel on top of Ni_2Si , and the "Si cap" region represents a layer of Si on top of NiSi_2 . Overall this diagram is in excellent agreement with a similar diagram we published earlier based solely on RHEED measurements, with, of course, additional information about chemical state and disordered phases from the Auger measurements [21].

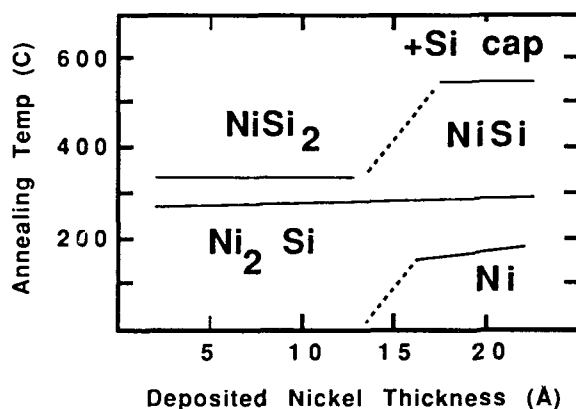


Figure 3. Kinetic phase formation diagram based on Auger lineshape data. Transformation temperatures are determined by the points where a given Auger lineshape component exceeds 0.50 in fractional weight.

We would like to interpret the transformation temperatures (T_f) which are the boundaries between phases in this diagram. For this it is useful to extrapolate well known results from conventional thin film studies of the same system. It is known that Ni_2Si and NiSi form through bulk diffusion limited reactions at temperatures near 275 and 350 C respectively in 1000 Å films [22,23]. Assuming the same reaction mechanisms, one can easily extrapolate these transformation temperatures to the ultrathin film regime, using the absolute measurements of diffusivity. In doing so, we find that Ni_2Si and NiSi would form at temperatures of 180 C and 280 C respectively. On the other hand, the formation of NiSi_2 in 1000 Å films is nucleation limited and occurs "explosively" at ~ 800 C [7,24]. This reaction has no explicit dependence on film thickness, and in that sense would still occur near 800 C in the ultrathin films.

In comparing with our data, we find that the formation temperatures for Ni_2Si and NiSi for 20 Å films are in remarkably close agreement with the extrapolated values, and conclude that these reactions are probably bulk diffusion limited. However, we notice that T_f for Ni_2Si becomes dramatically lower for films thinner than 20 Å. This may be understood as a switch from bulk to surface (or other defect mediated) diffusion, which is generally orders of magnitude faster than bulk diffusion, and takes place when the overlayer is no longer contiguous [25]. Such a process has been described from a somewhat different viewpoint in RBS experiments [13].

It remains to explain the dramatic lowering of T_f for NiSi_2 in the ultrathin films. In classical nucleation theory, the rate of formation of critical sized nuclei is exponentially activated with an energy barrier given by

$$\Delta G^* = (\Delta\sigma)^3 / (\Delta G - \Delta H)^2$$

where $\Delta\sigma$ is the energy cost of making new interfaces (while losing the old ones), ΔG is the volume free energy gain and ΔH is the volume strain energy cost [4,26,27]. All three of these factors appear to change with coverage in the ultrathin film situation. For example, the reactions below 10 Å thickness are from Ni_2Si to NiSi_2 , while those at higher coverage are from NiSi to NiSi_2 , changing the ΔG term. In addition ΔG may include the heat of crystallization if the parent phase is amorphous or consists of highly strained grains. Likewise the $\Delta\sigma$ term is distinctly lower for coherent vs incoherent interfaces. Both types are present at various coverages in the range from 0 to 20 Å [10,21]. Finally, the ΔH term is sensitive to lattice mismatch, which is 1% for NiSi_2 , 2% for Ni_2Si -theta, 3% for Ni_2Si -delta and 26% for NiSi , each referred to the substrate unit cell area [28]. Although one does not have actual numbers to put into such a formulation, and the classical theory is undoubtedly an oversimplification, one does have the possibility to vary these terms (possibly individually) in the silicide ultrathin film systems. In any case, events conspire to lower T_f for the NiSi_2 phase monotonically (probably discontinuously) as one goes to thinner films in the region below 30 Å.

One final comment concerns the much studied B-type to A-type NiSi_2 transition occurring near 13 Å. This transition is merely a symptom of the low temperature precursor reactions as shown on the kinetic phase diagram, so a proper explanation must involve an understanding of these precursor states. Explanations based on a Si to NiSi_2 reaction are probably groundless [29]. It has recently been observed that the Ni_2Si -theta phase is directly correlated with the A-type NiSi_2 phase [10,15]. This is helpful, yet there remains the fundamental problem of explaining the formation of the Ni_2Si -theta phase as well as other phases occurring at lower and higher coverages.

SUMMARY

We have shown that one can monitor chemical reactions in ultrathin film metal/semiconductor systems using numerical Auger lineshape decomposition. Through systematic measurements of coverage and temperature conditions one can connect the results from monolayer level studies with results from 1000Å thin film experiments. In ultrathin films the "interface reactions" are "kinetically isolated", which, in the case of Ni/Si(111) has allowed observations of a switch from bulk to surface diffusion and a dramatic variation in the rate of nucleation limited

reactions. It is hoped that through such studies one can begin to make predictive models of interface reactions in metal/semiconductor systems.

ACKNOWLEDGEMENTS

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QUATERNARY PHASE EQUILIBRIA IN THE Ti-Si-N-O SYSTEM: STABILITY OF METALLIZATION LAYERS AND PREDICTION OF THIN FILM REACTIONS

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ABSTRACT

During high temperature circuit fabrication, metallization layers can come in contact with both solids and gases. Their stability can be addressed with the aid of phase equilibria. Using the Gibbs phase rule as a basis, a method for generating phase diagrams for multicomponent systems can be established. This procedure is described and illustrated by reference to the quaternary phase diagram of Ti-Si-N-O. This phase diagram can then be used to predict stability and/or reactions in metallization layers and thin films.

INTRODUCTION

In a self-aligned silicide (salicide) process involving Ti [1,2,3], the Ti is deposited onto Si. An 800-900°C anneal results in the formation of TiSi_2 . Prior to deposition of Al metal on TiSi_2 , a TiN barrier layer is formed by exposing the silicide to a nitriding ambient. Both TiSi_2 and TiN are then in contact with the adjacent oxide. This situation is shown schematically in Figure 1. The interaction of TiSi_2 , TiN and SiO_2 involves four elements and hence quaternary phase diagrams are necessary to study the reactions, if any, in the system.

The calculation of ternary phase diagrams and their application to understanding the processing of silicides and integrated circuit materials has been demonstrated for instance by Beyers [4,5,6]. We proceed further by calculating the phase diagram for a quaternary system, Ti-Si-N-O. The stability of the various metallization layers can then be easily understood. Conversely, thin film reactions involving the four elements can also be predicted. As an example, we refer to the Ti/SiON reaction studied by Morgan *et al.* [7].

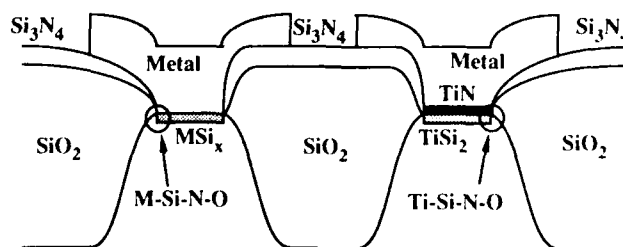


Figure 1: Schematic cross-section of a bipolar junction transistor, showing regions where quaternary phase equilibrium is important.

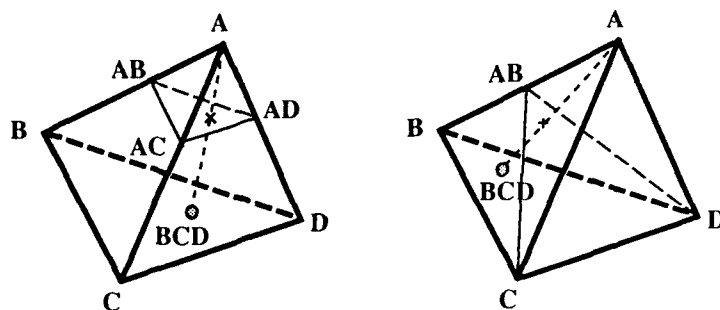
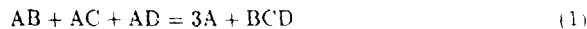


Figure 2: Schematic quaternary (A-B-C-D) phase diagrams showing either the existence of a tie-line or a tie-plane, but not both.

THERMODYNAMICS

At constant temperature and pressure, the Gibbs phase rule predicts a maximum of four phases in equilibrium in a four component system. The graphical representation of the equilibrium phases as a function of composition, i.e. the phase diagram, is achieved by plotting the tie-lines (two-phase equilibrium) and tie-planes (three-phase equilibrium) in a regular tetrahedron, the four corners of which represent each of the pure components. Tie-tetrahedra, bounded by four tie-planes (each of which in turn is bounded by three tie-lines), represent four phase equilibrium, and fill the entire tetrahedron volume without overlapping. Schwartzman *et al.* [8] have used the fact that in a quaternary phase diagram, a tie-line cannot cross a tie-plane for the simple reason that at the point of their intersection, there would be five phases in equilibrium. This, of course, violates the Gibbs phase rule. This situation is shown schematically in Figure 2.

Thermodynamics provides a framework to predict which of the two, the tie-line or the tie-plane, exists. A balanced reaction is written such that three phases (say AB, AC and AD) react to form two products (say A and BCD).



The change in Gibbs free energy for the reaction, ΔG , at the temperature and pressure in question is calculated by taking the difference of the sums of free energies of formation of the products and the reactants. Thus

$$\Delta G = (3G_A + G_{BCD}) - (G_{AB} + G_{AC} + G_{AD}) \quad (2)$$

where G_A , G_{BCD} , G_{AB} , G_{AC} and G_{AD} are the Gibbs free energies of formation of phases A, BCD, AB, AC and AD respectively. A tie-line exists between A and BCD if $\Delta G < 0$. Otherwise, a tie-plane connects AB, AC and AD. The entire phase diagram can be calculated by taking into account all the possible combination of reactants and products. A computer program has been written to perform this rather tedious exercise. Having calculated all the tie-lines and tie-planes, the program plots the same in a regular tetrahedron.

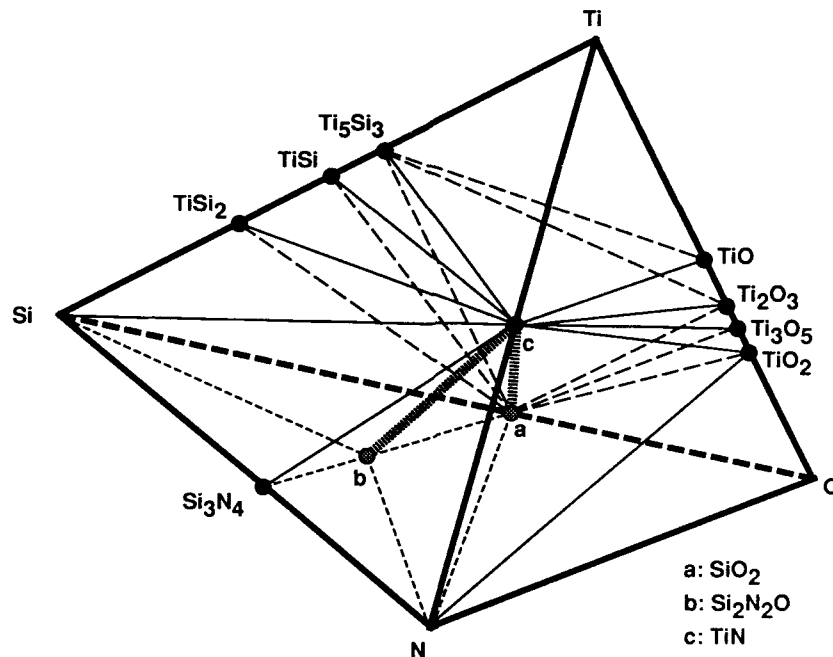


Figure 3: The calculated Ti-Si-N-O quaternary phase diagram ($T = 700-1000^\circ\text{C}$). Thin solid or dashed lines represent the tie-lines on the faces of the tetrahedron (i.e. ternary systems) and the thick dashed lines are the interior (quaternary) tie-lines.

THE Ti-Si-N-O SYSTEM

Before calculating a quaternary phase diagram, it is important to have calculated all the four ternary phase diagrams that make up the quaternary system. The Ti-Si-O, Ti-Si-N, Ti-N-O, and Si-N-O phase diagrams will be first discussed. Each of these ternaries is represented on one of the faces of the tetrahedron, thus giving rise to the exterior portion of the quaternary phase diagram (Figure 3). The Gibbs free energy values used in the calculation were taken from Barin and Knacke [9].

The calculated Ti-Si-O phase diagram is in agreement with that of Beyers [4]. Even though the SiO_2 involved in thin film reactions is amorphous, and thus metastable, its free energy of formation is comparable to that of crystalline SiO_2 [4]. The free energy data for cristobalite were thus used in the calculations. The absence of a tie-line between Ti and SiO_2 implies that a thin film of Ti is unstable on a SiO_2 substrate. The titanium silicides are expected to be stable on SiO_2 since there exist tie-lines between the silicides and SiO_2 .

An examination of the Ti-Si-N phase diagram immediately reveals that TiN is a dominant phase in this system—tie-lines emanate from it to all other phases. An important deduction from this diagram is that TiSi_2 is stable on *conducting* TiN, and not on *insulating* Si_3N_4 [6].

Again TiN is the dominant phase in the Ti-N-O system. All the titanium oxides

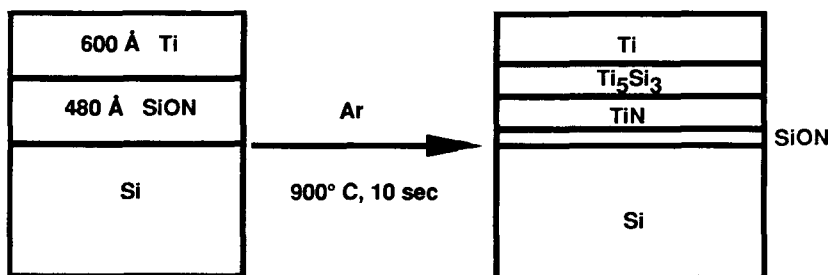
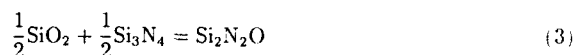


Figure 4: Schematic representation of the Ti/SiON reaction. After [7].

are stable in contact with TiN.

As a consequence of the Gibbs phase rule, tie lines must exist between $\text{Si}_2\text{N}_2\text{O}$ and Si, Si_3N_4 , SiO_2 . Even though the Gibbs free energy of $\text{Si}_2\text{N}_2\text{O}$ is not available, an upper limit of the same can be calculated from knowledge of that for SiO_2 and Si_3N_4 . The fact that $\text{Si}_2\text{N}_2\text{O}$ is a stable phase implies that the reaction



must have a negative free energy of reaction, i.e. $\Delta G < 0$. Thus it can be estimated that $\Delta G_{\text{Si}_2\text{N}_2\text{O}} \leq -203$ kcal/mole. This value has been used in the calculation of the Si-N-O phase diagram.

The quaternary phase diagram was calculated using the *same* Gibbs free energy values used in the calculation of the ternary diagrams. In addition to the ternary (exterior) tie-lines, quaternary (interior) tie-lines are now present from TiN to SiO_2 and $\text{Si}_2\text{N}_2\text{O}$. Clearly, TiN is a stable phase—e.g. with the titanium silicides and oxides, and with SiO_2 , Si_3N_4 and $\text{Si}_2\text{N}_2\text{O}$.

APPLICATIONS

As mentioned earlier, during salicide processing, TiN comes in contact with TiSi_2 , both of which come in contact with SiO_2 . A careful examination of the Ti-Si-N-O phase diagram reveals the existence of a tie plane connecting TiSi_2 , TiN and SiO_2 . Thus one can conclude that this metallization bilayer of TiN and TiSi_2 , in contact with SiO_2 is a stable one.

Consider now, the reaction of Ti on silicon oxynitride "SiON" studied by Morgan *et al.* [7]. The reaction is shown schematically in Figure 4. To predict the reaction products, the quaternary phase diagram can again be used. In Figure 5, SiON is represented in the Si-N-O ternary section, i.e. the base of the tetrahedron. Since there is no tie line between Ti and SiON, one can conclude that there ought to be a reaction between the two. Furthermore, since SiON is not a thermodynamically stable phase, it can be assumed that it breaks down, and that Si, N and O diffuse into the Ti; this is equivalent to saying that Si, N and O are added to Ti in proportionate amounts. This situation is shown schematically by the arrow in Figure 5. The initial reaction products, as predicted by the Ti-Si-N-O quaternary phase diagram, are then Ti_5Si_3 , TiN and TiO, since they form the very first tie plane that is intersected by an imaginary line joining Ti and SiON. This is

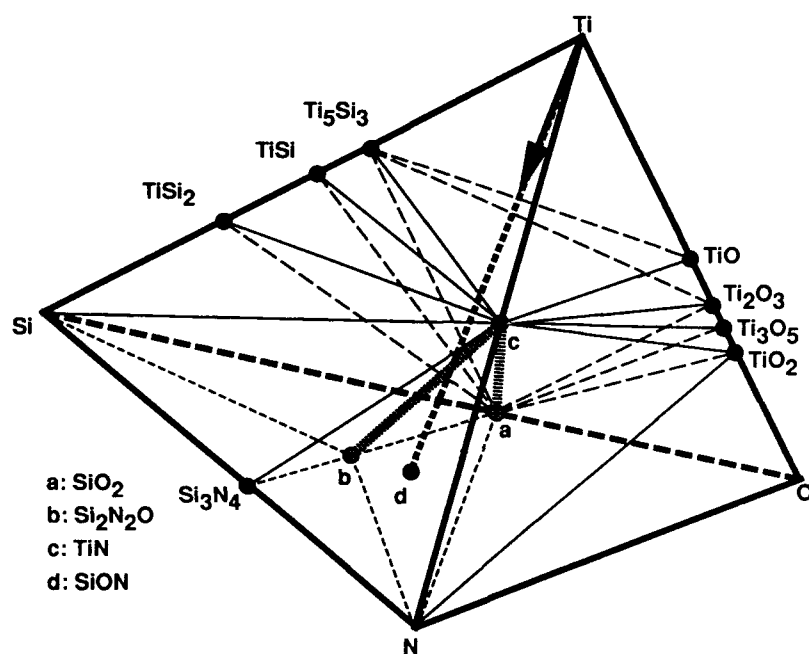


Figure 5. Interpretation of the Ti/SiON reaction. Initial reaction products are predicted to be Ti_5Si_3 , TiN and TiO , since this is the first tie-plane intersected by the arrowed line (*not an equilibrium tie-line*) from the titanium end.

in agreement with two of the reaction products (Figure 4) identified by Auger electron spectroscopy. It is quite possible that careful electron diffraction analysis could reveal the presence of titanium oxide.

CONCLUSIONS

Quaternary phase diagrams provide a fundamental framework for addressing the issue of phase equilibria in metallization layers used in integrated circuits. The calculated Ti-Si-N-O quaternary phase diagram predicts the stability of TiN/TiSi₂ metallization employed in a salicide technology. The reaction products as deduced by the phase diagram for Ti/SiON are in reasonable agreement with Auger electron spectroscopy results.

ACKNOWLEDGEMENTS

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KINETICS AND THERMODYNAMICS OF AMORPHOUS SILICIDE FORMATION IN NICKEL/AMORPHOUS-SILICON MULTILAYER THIN FILMS

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Abstract

Cross-sectional transmission and scanning transmission electron microscopy and thermodynamic and kinetic analysis have been used to characterize amorphous and crystalline nickel silicide formation in nickel/amorphous-silicon multilayer thin films. An amorphous-nickel-silicide layer was formed between the nickel and amorphous-silicon layers during deposition. Heating caused crystalline Ni_2Si to form at the nickel/amorphous-nickel-silicide interface. The composition of the amorphous-silicide was determined to be approximately 1 Ni atom to 1 Si atom. Thermodynamic analysis indicates that amorphous-nickel-silicide could be in equilibrium with nickel and amorphous-silicon if there were kinetic barriers to the formation of the crystalline silicides. Kinetic analysis indicates that the "nucleation surface energies" of the crystalline silicides, other than Ni_3Si , must be 1.6 to 3.0 times larger than that of amorphous-nickel-silicide.

Introduction

Metal silicides are usually formed by a reaction, induced by thermal annealing, between a thin film of a pure metal and a silicon wafer.¹ While *crystalline* silicides typically form during reactions of metals with single crystal silicon, various authors have recently reported the formation of metastable *amorphous*-silicide phases as well as crystalline silicide phases during metal/amorphous-silicon thin film reactions.^{2,3} In this paper, we report on the thermodynamic and kinetic analysis of amorphous and crystalline nickel silicide formation in nickel/amorphous-silicon multilayer thin film reactions.

Experimental

Samples for cross-sectional electron microscopy were prepared by first loading thermally oxidized (100) silicon wafers into an electron-beam evaporator. A nickel/amorphous-silicon multilayer film was then deposited by alternate electron beam evaporation of ten total layers of nickel and silicon. The atomic concentration ratio of nickel and silicon was 2 nickel atoms to 1 Si atom and the modulation period of the multilayer thin film was 100 nm.

After deposition, the wafers were removed from the evaporator and separated into two groups. One group was analyzed in the as-deposited condition and the other was heated at 20 K/min to 535 K and quenched at 320 K/min to room temperature. The temperature and heating rate were chosen to correspond to thermal changes observed in calorimetric data of these multilayer thin films.² Both sets of samples were then mechanically thinned in cross-section and ion milled at less than 4 kV on a liquid nitrogen cooled cold stage. Structural analysis was done by examining the nickel/amorphous-silicon multilayer thin films in cross-section with a JOEL 200 electron microscope operating at 200 keV. Composition analysis was done in cross-section with a Vacuum Generator HB5 scanning transmission electron microscope operating at 100 keV.

Results

Figure 1 shows a bright field cross-sectional micrograph of a portion of an as-deposited nickel/amorphous-silicon multilayer thin film with a modulation period of 100 nm. This figure shows that the nickel layers have a polycrystalline structure. The lighter colored layers are amorphous-silicon and have a typical amorphous appearance. Between the nickel and silicon layers there is a region of darker contrast which has no apparent crystalline structure. A

microdiffraction pattern taken from this layer shows that it is amorphous and we identify it as an amorphous-nickel-silicide. In the as-deposited film, this amorphous-nickel-silicide between the nickel and silicon layers has a thickness of approximately 4 nm.

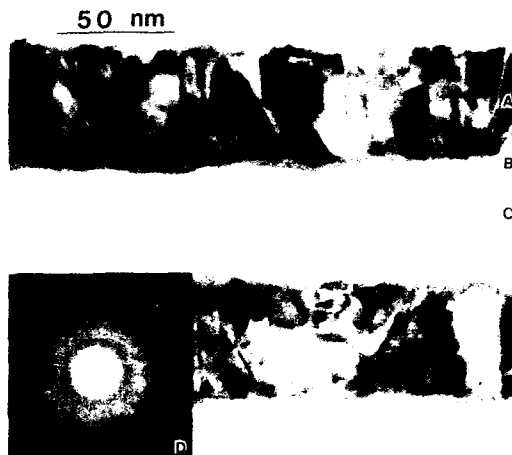


Figure 1: Bright field transmission electron microscope image of an as-deposited nickel/amorphous-silicon multilayer thin film: (a) polycrystalline nickel; (b) gray featureless layer with no crystalline contrast; (c) amorphous-silicon. The microdiffraction pattern (d) is taken from layer (b) and indicates that this layer is an amorphous-nickel-silicide.

Figure 2 shows the structure of the multilayer thin film of figure 1 which has been heated at 20 K/min to 535 K and then quenched at 320 K/min to room temperature. The amorphous-nickel-silicide is still present between the nickel and the amorphous-silicon layers, and it has grown to a thickness of about 20 nm. A polycrystalline nickel silicide has also formed and grown to a thickness of approximately 15 nm between the nickel and the amorphous-nickel-silicide layers. Thin film X-ray diffraction indicates that this layer is Ni_2Si .⁴

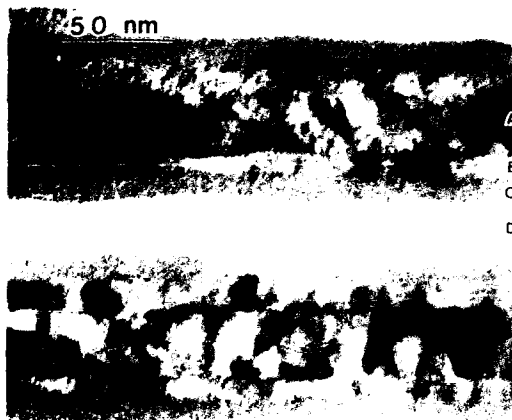


Figure 2: Bright field transmission electron microscope image of the multilayer thin film of figure 1 which has been heated at 20 K/min to 535 K and quenched to room temperature: (a) polycrystalline nickel; (b) Ni_2Si ; (c) amorphous-nickel-silicide; (d) amorphous-silicon.

The composition of the layers in the nickel/amorphous-silicon multilayer thin film of figure 2 was investigated using energy dispersive X-ray microanalysis in cross-sectional scanning

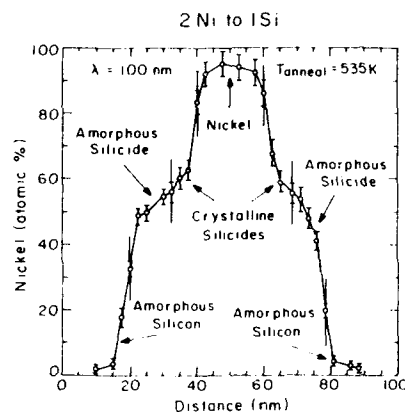


Figure 3: Nickel composition versus distance in a plane perpendicular to the plane of the layers for the multilayer film of figure 2. The position of the interfaces between different layers is marked by solid vertical lines.

transmission electron microscopy. The resulting data is shown in figure 3. In this figure, nickel concentration versus distance measured in a plane perpendicular to the plane of the layers is plotted across one modulation period of the multilayer thin film. This figure suggests that the composition of the amorphous-nickel-silicide under these annealing conditions is approximately 1 Ni atom to 1 Si atom.

Discussion

As demonstrated by figure 1, the first phase that forms from a reaction between layers of nickel and amorphous-silicon is an amorphous-nickel-silicide. This can be explained by considering the Gibbs free-energy versus composition diagram for the nickel/silicon system shown in figure 4a. In this figure, the free energies at 350 K of fcc nickel, covalently bonded amorphous-silicon, crystalline nickel silicides and the undercooled nickel-silicon liquid solution are plotted as a function of silicon concentration based on data reported by Mey⁵ and Donovan et al⁶. We have assumed in figure 4a that the free energy of amorphous-nickel-silicide is approximated by that of the undercooled metallic liquid.

In this figure, the common tangents between fcc nickel, the crystalline silicides and pure amorphous-silicon have been drawn in. The amorphous-nickel-silicide free energy curve lies above these common tangents, indicating that the amorphous-nickel-silicide is unstable with respect to the crystalline silicides (if they are all present, or if any one but Ni_3Si and NiSi_2 is present). This implies that an amorphous-nickel-silicide would not form at the nickel/amorphous-silicon interface if there were no kinetic barriers to the formation of the crystalline silicides. The instability of the amorphous-nickel-silicide also indicates that the simultaneous growth of amorphous-nickel-silicide and Ni_2Si will not occur at 350 K. However, for the annealing conditions of figure 2, this simultaneous growth can occur due to the fact that at 535 K, amorphous-nickel-silicide is thermodynamically stable with respect to Ni_2Si .

Because amorphous-nickel-silicide forms at the nickel/amorphous-silicon interface, there must be kinetic barriers that prevent the formation of the crystalline silicides. With this observation we can remove the crystalline silicides from the Gibbs free energy versus composition diagram of figure 4a. The resulting diagram is shown in figure 4b, with the common tangents now being drawn between fcc nickel, amorphous-silicon and amorphous-nickel-silicide. This construction indicates that the amorphous-nickel-silicide can form from and be in equilibrium with nickel and amorphous-silicon. Figure 4b also indicates that the composition of the amorphous-nickel-silicide should be between 35 to 55 atomic percent silicon. This agrees with the experimentally measured value of 50 atomic percent silicon presented in figure 3.

The kinetic barriers to the formation of the crystalline silicides can involve both nucleation¹ and growth, or growth alone.⁷ It has been shown recently that silicide formation at the

nickel/amorphous-nickel-silicide interface is controlled by nucleation barriers.⁸ Due to the similarities between the nickel/amorphous-nickel-silicide and the nickel/amorphous-silicon

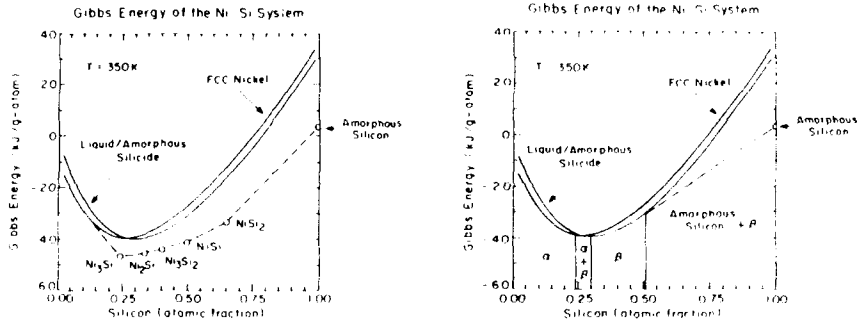


Figure 4a: Gibbs free energy versus composition diagram for the nickel/silicon system at a temperature of 350 K. The crystalline silicides are distinguished by "O". Dashed lines are the common tangents for fcc nickel, the crystalline silicides and amorphous-silicon.

Figure 4b: Same as figure 4a except that we have assumed that kinetic barriers prevent the formation of the crystalline silicides. α represents fcc nickel and β represents the amorphous-nickel-silicide. Common tangents are drawn for fcc nickel, amorphous-nickel-silicide and amorphous-silicon.

interfaces, one would also expect silicide formation at the nickel/amorphous-silicon interface to be controlled by nucleation barriers. These barriers are characterized by a critical free energy for formation given by,⁹

$$\Delta G^* = \frac{16\pi \times (\Delta\sigma)^3}{3 (\Delta G_v)^2} \quad (1)$$

where ΔG_v is the thermodynamic driving force and $\Delta\sigma$ is the "nucleation surface energy" for amorphous or crystalline nickel silicide formation at the nickel/amorphous-silicon interface. The "nucleation surface energy" for heterogeneous nucleation of lense shaped nuclei at the nickel/amorphous-silicon interface is given by,⁹

$$\Delta\sigma = \left(\sigma_{n-sl}^3 \left(\frac{2-3\cos\theta + (\cos\theta)^3}{4} \right) + \sigma_{s-sl}^3 \left(\frac{2-3\cos\theta' + (\cos\theta')^3}{4} \right) \right)^{\frac{1}{3}} \quad (2)$$

where σ_{n-sl} , σ_{s-sl} , θ and θ' are defined in figure 5.

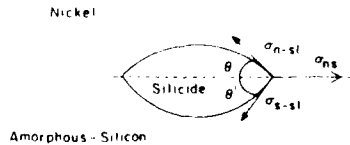


Figure 5: Ideal lense shaped silicide nucleus forming at the nickel/amorphous-silicon interface. σ_{n-sl} , σ_{s-sl} and σ_{n-s} are the nickel/silicide, amorphous-silicon/silicide and nickel/amorphous-silicon interface energies respectively. θ and θ' are the contact angles for the nickel/silicide and the amorphous-silicon/silicide interfaces respectively.

If we assume local thermodynamic equilibrium at the interface, the maximum driving force ΔG_v , can be expressed as:

$$\Delta G_v = G_{Ni_xSi_y} - (\overline{G}_{Ni} + X_{Si}(\overline{G}_{Si} - \overline{G}_{Ni})) \quad (3)$$

where $G_{Ni_xSi_y}$ is the free energy of the amorphous or crystalline silicide phase, \overline{G}_{Ni} and \overline{G}_{Si} are the chemical potential of nickel and silicon respectively and X_{Si} is the atomic fraction of silicon in Ni_xSi_y . The ΔG_v calculated in this way corresponds to the maximum driving force, based on the assumption that interdiffusion has lead to equilibrium compositions. However the $\Delta \sigma$ ratio calculated below represents a lower bound regardless of the amount of interdiffusion.¹⁰

For amorphous-nickel-silicide to form first at the nickel/amorphous-silicon interface, we must have

$$\Delta G^*_{Ni_xSi_w} > \Delta G^*_{am-NiSi} \quad (4)$$

Combining this equation with equation 1 and rearranging, we obtain,

$$\Delta \sigma_{Ni_xSi_w} > \left(\frac{\Delta G_{v, Ni_xSi_w}}{\Delta G_{v, am-NiSi}} \right)^{\frac{2}{3}} \Delta \sigma_{am-NiSi} \quad (5)$$

where Ni_xSi_w stands for the crystalline silicides and am-NiSi stands for amorphous-nickel-silicide. Combining equations 5 and 3 we can calculate a lower bound for nucleation surface energies of crystalline silicides compared to amorphous-nickel-silicide. The lower bound for nucleation surface energies along with thermodynamic driving forces for amorphous and crystalline silicide formation for a reaction temperature of 350 K are shown in table 1.

Table 1: Calculated lower bound for the nucleation surface energies of crystalline nickel silicides compared to amorphous-nickel-silicide for silicide formation at a nickel/amorphous-silicon interface. Also shown are thermodynamic driving forces for silicide formation at an equilibrium nickel/amorphous-silicon interface. ΔG_v for amorphous-nickel-silicide corresponds to the maximum $|\Delta G_v|$ for amorphous-nickel-silicide formation.

Phase	ΔG_v (kJ/g-atom)	$\left(\frac{\Delta G_{v, Ni_xSi_w}}{\Delta G_{v, am-NiSi}} \right)^{\frac{2}{3}}$
Ni ₃ Si	-1.8	0.7 <
amorphous-NiSi	-2.8	----
Ni ₂ Si	-6.0	1.6 <
Ni ₃ Si ₂	-9.2	2.2 <
NiSi	-12.5	2.7 <
NiSi ₂	-14.3	3.0 <

Table 1 demonstrates that, except for Ni₃Si, all the crystalline nickel silicides have higher driving forces for formation at an equilibrium nickel/amorphous-silicon interface than amorphous-nickel-silicide. Table 1 also indicates that the nucleation surface energy of a crystalline silicide needs to be from 1.6 to 3.0 times larger than the nucleation surface energy of amorphous-nickel-silicide in order for amorphous-nickel-silicide to form first at the nickel/amorphous-silicon interface.

The lower nucleation surface energy of amorphous nickel-silicide compared to that of crystalline nickel silicides can not be quantitatively explained. However, qualitatively, a low surface energy between amorphous-nickel-silicide and amorphous-silicon might be expected due to the amorphous nature of both structures. The nickel/silicide interface energies for both the

crystalline silicides and amorphous-nickel-silicide on the other hand, might be expected to be similar due to the dissimilarity between the nickel (fcc) and either silicide structure. Thus combining surface energy contributions at both the nickel/silicide and silicide/amorphous-silicon interfaces, it seems reasonable that amorphous-nickel-silicide would have the lowest nucleation surface energy of all the silicide phases.

Conclusion

We have shown for nickel/amorphous-silicon multilayer thin films that an amorphous-nickel-silicide is the first phase to form at the nickel/amorphous-silicon interface. Heating the multilayer thin film to 535 K, caused Ni_2Si to form at the nickel/amorphous-nickel-silicide interface. Cross-sectional scanning transmission electron X-ray dispersive analysis suggested that the composition ratio of the amorphous-nickel-silicide was approximately 1 Ni atom to 1 Si atom. Free energy diagrams were presented which demonstrated that amorphous-nickel-silicide is thermodynamically stable if kinetic barriers prevent the formation of the crystalline silicides. An analysis was presented which demonstrates that the nucleation surface energies of crystalline silicides, other than Ni_3Si , had to be 1.6 to 3.0 times larger than the nucleation surface energy of amorphous-nickel-silicide at 350 K, in order for amorphous-nickel-silicide to be the first silicide phase to form at the nickel/amorphous-silicon interface.

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A MODEL FOR INTERDIFFUSION AT METAL SEMICONDUCTOR INTERFACES: CONDITIONS FOR SPIKING

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ABSTRACT

We have derived a dynamical model for interdiffusion at aluminum-silicon interfaces which can explain the great variety of rates of interdiffusion observed for this system. The variables addressed by the model include the degree of covalent bonding which occurs at the chemical interface and the local atomic structure of that interface. Local solid solubility data and maximum rates of dissolution are derived analytically, and good agreement is observed between the model and both thermodynamic data for the bulk aluminum-silicon system and kinetic data for reaction rates at differently prepared interfaces. The influence of dopants and structural defects on the predictions of the model is in accord with experimental observations. The model points to some critical conditions for the preparation of thermally stable aluminum-silicon interfaces, which are potentially applicable to other metal-semiconductor systems.

INTRODUCTION

The preparation of thermally stable metal-semiconductor interfaces is key to device fabrication. While technical advances have reduced the magnitude of metal-semiconductor interface instability, a fundamental understanding of the phenomena responsible for interdiffusion at these interfaces is lacking. We propose a dynamical model for atomic movements which occur at aluminum-silicon interfaces as an example of a typical metal-semiconductor interface. This model incorporates an atomic-scale mechanism for the interface interdiffusion based on the motion of vacancies at the interface. Because this mechanism is microscopic, the configurational entropy of the system can be treated as the result of the random nature of a large number of atomic movements, and hence ignored in a treatment of each individual movement. As a result, kinetic data such as the rate of atomic motion across the interface can be extracted from the model.

ALUMINUM-SILICON REACTIONS

Aluminum is well known to react with silicon, often resulting in very non-uniform interfaces.¹ This reaction is of interest technologically because it commonly occurs during the contact sintering step of a fabrication, during which the silicon native oxide is reduced and an intimate contact is formed. In general, the reaction involves the dissolution of silicon into aluminum, followed by transport of the silicon away from the interface, often accompanied by precipitation of silicon crystallites in the aluminum film. This reaction has been attributed to bulk solid solubility criteria, to mechanical stress occurring at the interface, or to reactions with a nearby silicon oxide. However, the rate at which the dissolution occurs is found to be very sensitive to different methods of interface preparation. Fig. 1 shows a partial list of dissolution rates observed by different researchers.²⁻¹⁰ The highest dissolution rate is observed for aluminum films on undoped polycrystalline silicon, up to 5×10^{16} at/cm²s at 465°C, while the lowest are observed for epitaxial aluminum films on single crystal silicon, observed to be less than 5×10^{12} at/cm²s at 450°C. Among the many factors that are observed to affect the dissolution rates are silicon content of the aluminum, crystallinity of the silicon, doping in the silicon and dopant segregated to the interface, the presence of a silicon oxide and the quality and thickness of that oxide.

The rate limiting step for the dissolution process could be either the interfacial reaction of individual silicon atoms moving from the interface into the aluminum film, or the transport of silicon away from the interface into the aluminum. We point to our own work as an example of a case in which the interfacial reaction must be a rate-limiting reaction step.⁷ The work presented here focuses on a model for this interfacial step of the reaction. No such model has been proposed for interdiffusion in the aluminum/silicon system.

Figure 1. Estimates of Dissolution rates from the Literature.

Authors	Ref.	Rate (at/cm s)	T(°C)	Comments
Nakamura et al.	2	$> 6 \times 10^{15}$ $> 7 \times 10^{14}$	560 460	1.2 μm Al on 0.5 μm polySi, undoped
Naguib & Hobbs	3	1×10^{16}	450	2500 Å Al on 3000 Å polySi, undoped
Learn & Nowicki	4	5×10^{15} $< 1 \times 10^{14}$	500 500	1 μm Al on 0.5 μm polySi, undoped 1 μm Al on 0.5 μm polySi, P-doped
Herbots, et al.	5-7	up to 5×10^{16} down to 1×10^{13} 3×10^{14}	465 465 465	0.3 μm Al on 0.3 μm polySi, undoped 0.3 μm Al on 0.3 μm polySi, As-doped 0.3 μm Al on (100) Si, undoped, rate lower for doped samples
Ignat'ev, et al	8	$< 1 \times 10^{13}$	570	0.3-1 μm epi-Al on (100) Si
Yamada et al.	9	$< 5 \times 10^{12}$	450	0.36 μm epi-Al on (111) Si by ICBD: higher rate for (100) Si
Kobayashi, et al	10	$< 4 \times 10^{13}$	430	1 μm epi-Al on (111) Si by GTC-CVD

A MODEL FOR TREATING ALUMINUM-SILICON INTERDIFFUSION

Atomistic Mechanism

Our model is based on the dissolution of silicon into aluminum via a vacancy mechanism. That is, vacancies in the aluminum occasionally diffuse to the interface, exchanging places with a silicon atom at the silicon surface. We denote this type of jump as $\text{Si}\downarrow$. Subsequently, the site once occupied by the silicon atom is refilled with an aluminum atom ($\text{Al}\uparrow$). This sequence of events resembles a vacancy "bouncing off" the interface, and results in the dissolution of one silicon atom. The reverse jumps are also allowed to occur, that is, a vacancy exchanging places with an aluminum atom substituting for a silicon site at the interface ($\text{Al}\downarrow$), and being refilled with a silicon atom adjacent to the interface ($\text{Si}\uparrow$). These jumps are illustrated in Fig. 2. Our model ignores the possibility of vacancy diffusion in the silicon, because of the very high energies for vacancy formation and migration in silicon.¹¹

Assumptions

We would like to write expressions for the frequencies of these different vacancy jumps. In analogy to motion of vacancies in the bulk, these frequencies are functions of the concentration of vacancies, determined from a formation energy, and of an exponential of the activation energy for their motion. Before placing values on these energies, assumptions must be made about the nature of the interface. To begin, we assume that the motion of vacancies at the interface is governed by the activation energy for vacancy migration in aluminum, $E_{\text{Mig}}^{\text{Al}}$, with the exceptions noted below. This corresponds to an interface with metallic bonding character, as suggested experimentally and theoretically.^{12,13}

First, for the dissolution of one silicon atom caused by jump $\text{Si}\downarrow$, the bulk excess free energy of mixing per atom of silicon $\Delta G^{\text{xs},\text{Mix}}$ in aluminum must be added to the activation energy for jump $\text{Si}\downarrow$ only. This excess free energy is the enthalpy of mixing plus the non-configurational entropy of mixing multiplied by the temperature. We assume the reverse jump $\text{Si}\uparrow$ is not affected. Physically, if the dissolution reaction is complete after one atomic jump, as we speculate here, the interface takes on a very abrupt chemical transition, in agreement with Brillson, et al.¹⁴

Secondly, we assume that the jumps $\text{Si}\downarrow$ and $\text{Al}\uparrow$ are equally likely if equal numbers of silicon and aluminum atoms are in place to occupy vacancies at the interface. In other words, that the ratio of $\text{Si}\downarrow$ to $\text{Al}\uparrow$ jumps is simply the ratio of the concentration of silicon (in the aluminum near the interface) to that of aluminum. At low concentrations of silicon, this is X_{Si} , the atomic fraction of silicon in aluminum.

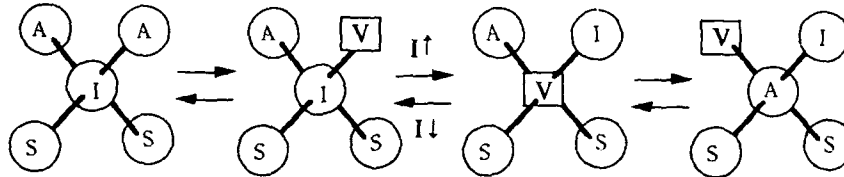


Figure 2. Atomistic Mechanism Proposed for Dissolution and Precipitation Occurring at a Silicon-Aluminum Interface. Forward arrows represent a sequence resulting in dissolution of a silicon atom if the interfacial atom *I* is a silicon atom, backward arrows represent a precipitation sequence.

The model predicts very high upper limits for precipitation rates on silicon surfaces. Using typical values, the rate can be above 1×10^{15} atoms/cm²s even for temperatures below 300°C. This is well above observations of post-anneal precipitation of thin layers of Al-doped silicon onto silicon surfaces, and allows for other observations of silicon precipitation from aluminum silicon films.^{17,18}

Lastly, we assume the concentration of vacancies near the interface is an exponential function of an activation energy which is the sum of the energy of vacancy formation in bulk aluminum, $E_{F,Bulk}^V$ and a factor ΔE^F . This factor is the difference in free energy between vacancies near the interface and vacancies in the bulk. For example, an interface with some component of covalent bonding might have an appreciable ΔE^F , due to extra enthalpy of breaking those bonds in moving vacancy from the bulk to the interface.

Frequencies of jump sequences

Now we can write expressions for the individual jump frequencies

$$J_{Si\uparrow} = f_{Si\uparrow} \omega_D [Si]_{Int} X_V \exp(-(\Delta G^{xs,Mix} + E_{Mig} + \Delta E^F)/kT) \quad (1)$$

$$J_{Al\uparrow} = f_{Al\uparrow} \omega_D [Al]_{Int} X_V \exp(- (E_{Mig} + \Delta E^F)/kT) \quad (2)$$

$$J_{Al\downarrow} = f_{Al\downarrow} \omega_D [V]_{Int} X_{Al} \exp(- (E_{Mig})/kT) \quad (3)$$

$$J_{Si\downarrow} = f_{Si\downarrow} \omega_D [V]_{Int} X_{Si} \exp(- (E_{Mig})/kT) \quad (4)$$

where *f* is a correlation factor which is different for each sort of jump, X_V is the fraction of vacancies in bulk aluminum, $[V]_{Int}$ is the number of vacancies available for \downarrow jumps in #/cm², $[Al]_{Int}$ and $[Si]_{Int}$ are the concentrations of aluminum and silicon atoms at interfacial sites in #/cm², X_{Al} and X_{Si} are atom fractions in the aluminum, and ω_D is the attempt frequency. The correlation factor enters the expressions because after a $Si\uparrow$ jump takes place, there is a larger fraction X_{Si} of silicon near interface vacancies, which in turn leads to a higher rate of $Si\downarrow$ jumps. Physically, this corresponds to a vacancy jumping back and forth resulting in no net motion. To first order, this factor can be evaluated for low X_{Si} as $(1-1/NN_x)$ for $Si\uparrow$ jumps where NN_x is the number of sites into which the vacancy can subsequently move: i.e., if there are three such sites, then one of three is occupied by a silicon atom and 33% of the jumps are cancelled ($f=.67$), if each jump is equally probable, as we assumed above. The factor can be evaluated as unity for the remaining jumps.

These equations can be simplified by considering sequences of jumps. At low values of X_{Si} , and appreciable values of $\Delta G^{xs,Mix}$, it becomes much easier to evaluate the frequency of a $Si\uparrow$ jump followed by a $Al\downarrow$ jump, etc. This eliminates the dependencies on $[V]_{Int}$ as well as separating out the frequency of back and forth jumps which cause no atomic motion. Assuming that each \uparrow jump is associated with a \downarrow jump removes another dependency. Thus, the frequency $J_{Si\uparrow-Al\downarrow}$, that of the concatenation of those two jumps, is

$$J_{Si\uparrow-Al\downarrow} = f_{Si\uparrow} \omega_D [Si]_{Int} \exp(-(\Delta G^{xs,Mix} + E_{Mig} + E_{F,Bulk}^V + \Delta E^F)/kT) \quad (5)$$

and

$$J_{Al\uparrow-Si\downarrow} = f_{Al\uparrow} \omega_D X_{Si} [Al]_{Int} \exp(- (E_{Mig} + E_{F,Bulk}^V + \Delta E^F)/kT) \quad (6)$$

As a check of the applicability of these expressions, we can use these formulae to calculate a solid solubility of silicon in aluminum. At equilibrium solubility, the flux of silicon out of the interface equals the flux in, so these frequencies must be identical. Setting the two equal, we find

$$X_{Si} = \left[(f_{SiT}/f_{AlT}) ([Si]_{Int}/[Al]_{Int}) \right] \exp(-(\Delta G^{xs,Mix})/kT) \quad (7)$$

This is the thermodynamic equation for solid solubility, as shown by Freedman and Nowick¹⁵, multiplied by the factor in brackets, which will be interface dependent. Thus, the model predicts the expected trends for thermodynamic solid solubility, modified by a factor which accounts for non-equilibrium interfaces.

Kinetics of the Model

In the previous section, the equilibrium criterion was met by setting the flux away from the silicon equal to the flux to the silicon. By examining these individual fluxes, we can estimate upper and lower bounds for dissolution and precipitation rates. For example, in the equation for J_{SiT-Al} we predict an upper limit of 1×10^{17} at/cm²s with the values $NN_x=4$, $\omega_D=10^{13}$ /s, $\Delta E^F=0$, $\Delta G^{xs,Mix} = .44\text{eV} + 1.7kT$ from Freedman and Nowick¹⁵, $E^F_{Bulk} = 0.62$ eV and $E^{Mig} = 0.66$ eV from Lundy and Murdoch¹⁶, $[Si]_{Int}=1.35 \times 10^{15}$ at/cm², the surface atomic density of Si (100), and $T=450^\circ\text{C}$.

A minimum upper bound dissolution rate might be estimated in two ways. First, the dissolution might be retarded by a high value of ΔE^F . Secondly, the correlation factor f_{SiT} might be constrained by the geometry of the interface to be very low. Following the first path, we need to evaluate the extra energy of a vacancy at the interface, or in other words, the strength of the aluminum-silicon bond at the interface. This is a rather elusive value, but it is not unreasonable to suggest that it might be as high as one quarter of the vacancy energy in silicon, 2.0 eV. This would lead to ΔE^F equal to 0.5 eV. Using the same values above for the other quantities, this gives a maximum dissolution rate of 3×10^{13} at/cm²s at 450°C .

Following the second path, we find that the fewer the number of sites with which an interface vacancy can exchange, the greater the influence of the correlation factor. In an extreme case, if there is but a single aluminum site adjacent to silicon surface sites, as in the case of (111) epitaxial aluminum on (111) silicon, then the correlation factor f_{SiT} is equal to zero and the dissolution rate also becomes zero (see Fig. 3 for an illustration). In this case there are no aluminum atoms available to fill a surface site vacated by a silicon atom, thus there can be no dissolution by the mechanism we propose.

These upper and lower limits account for the variations in dissolution rates summarized in Table 1. For example, the low reactivity of all of the epitaxial films is explained by a decrease in f_{SiT} , resulting in low dissolution rates. The results of Ignat'ev et al. are confusing, because their films are not grown on (111) silicon, the interface for which f_{SiT} can approach zero. However, the exact nature of their interface is not investigated. The results of Herbots et al., Nakamura et al., Naguib & Hobbs and Learn & Nowicki however, can be explained by a variation in ΔE^F . Here the variations in dissolution rates are less than a factor of 1000. In these cases, because interfaces between polysilicon and aluminum comprise a mix of different silicon and aluminum grain orientations, the interfacial structure will not be ordered enough that the correlation factor f_{SiT} plays a significant role in modifying the rate of dissolution.

The model predicts very high upper limits for precipitation rates on silicon surfaces. Using typical values, the rate can be above 1×10^{15} atoms/cm²s even for temperatures below 300°C . This is well above observations of post-anneal precipitation of thin layers of Al-doped silicon onto silicon surfaces, and allows for other observations of silicon precipitation from aluminum silicon films.^{17,18}

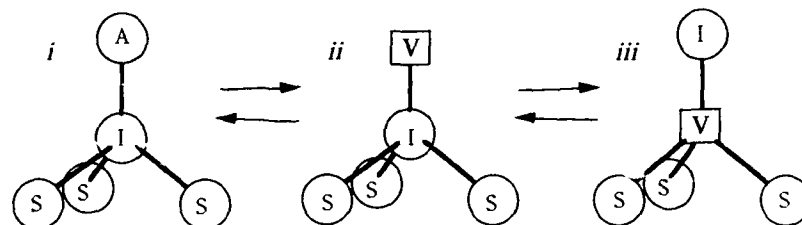


Figure 3. *Proposed Sequence of Vacancy Jumps at a Si(111)/Al(111) Epitaxial Interface. Once the vacancy has reached position iii, it can only exchange places with the atom originally in the interface, because of the high energy of moving a vacancy into the silicon structure. Thus the interface stays intact.*

Correlation of the Dissolution Rate with Transport Rate

We mentioned above that the rates of interface dissolution and bulk transport could both be rate limiting in the aluminum silicon reaction. The diffusion rate for silicon in thin film aluminum has been measured by McCaldin and Sankur to be in the range of 10^{-8} cm²/s at 450°C, which is about 100 times the diffusivity in bulk aluminum.¹⁹ For transport across a 3000 Å layer of metal, this would correspond to a flux of 1×10^{16} atoms/cm²s for a concentration gradient of 0.0005 at%. The conclusion we draw from this is that silicon transport in aluminum will not be a rate limiting mechanism unless the concentration gradients in the system are very low: i.e. when the system is very near equilibrium.

DISCUSSION

There are two major implications of the model for the fabrication of thermally stable interfaces. The first is that a greater degree of covalent bonding at the interface makes the interface more stable by repelling vacancies from it. Covalent bonding is weakened in the silicon structure at defects, such as grain boundaries or dislocations: thus, it is at the intersection of these defects with the surface where silicon films are the most prone to dissolution. We have suggested in earlier work that this effect can be reversed somewhat by the presence of dopant atoms at these defective sites.⁷ The effect of such dopants is to substitute for silicon atoms in the cores of these defects at sites of 3- or 5-fold coordination, bonding covalently to the atoms which surround them. In terms of the model, this increase in covalent bonding makes the interface more stable by decreasing the concentration of vacancies adjacent to these sites by increasing their formation energy, thus decreasing the dissolution rate. Thus, thermal stability of interfaces may be increased by promoting higher energy bonding at the interface itself. The term defect might also be extended to include surface ledges and kinks, which could also serve as preferential dissolution sites, and could also associate with dopant atoms. This type of interface stabilization is predicted to decrease the maximum dissolution rate by a factor of 3000 at 450°C.

Secondly, the model demonstrates the possibility of making interfaces extremely stable by exploiting the anisotropy of the vacancy jump frequencies in different directions, as represented in the correlation factor f_{Si} . This is especially promising for low coordination number structures for interfaces lying in low bond density planes. This type of interface stabilization is predicted to decrease the maximum dissolution rate until a different mechanism (e.g. divacancy) causes the dissolution.

We have neglected to discuss the factors $[Si]_{int}$ and $[Al]_{int}$ so far. Comparatively, the two factors should be roughly the same, as the number of sites from which a silicon atom can dissolve ought to be very similar to the number of sites onto which a silicon atom can precipitate. However, the relative values of these expressions is irrelevant in calculating maximum dissolution rates. In this case, the maximum value for these surface site densities is simply the surface atomic density. A more detailed look at these expressions is beyond the scope of this work.

This model ignores a number of phenomena which have been suggested to influence the aluminum silicon reaction: the presence of an oxide on the silicon surface, the effects of stress at the interface and the thermal expansion mismatch of the two materials, grain size of the aluminum, which might influence transport properties and the generation of vacancies, and vacancy-silicon

association, and lastly, it ignores silicon surface curvature, which, via the Gibbs-Thompson effect, would alter the thermodynamic values for free energy of mixing. The accuracy of the model in spite of its ignoring these effects is an indication that these phenomena are not directly responsible for affecting the reaction rate.

This sort of model ought to be equally applicable to any metal-semiconductor system in which there is an appreciable free energy of mixing, and for which the activation energy for vacancy migration in the metal is well below that in the silicon: for example the system of titanium / palladium / silver metallizations on silicon, as suggested by Weizer and Fatemi.²⁰ Also, the vacancy model for diffusion is especially applicable for close-packed metal structures.

CONCLUSION

We have examined in detail one aspect of aluminum silicon interdiffusion reactions. A model has been generated to calculate upper limits for dissolution rates controlled by the interfacial atomic transport caused by vacancy motion. Calculations are in good agreement with a number of experiments, and show promise for explaining the great disparity in observed dissolution rates. Other rate-limiting mechanism cannot be ruled out, however. The model suggests two phenomena that increase the interfacial stability: an increase in covalent bonding at the interface caused by increased ordering which lowers the number of vacancies available near the interface, and an increase in the influence of a correlation factor for vacancies interacting with the interface which is encountered for epitaxial aluminum on (111) silicon.

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ELECTRON-RADIATION-INDUCED EPITAXIAL GROWTH OF CoSi_2 ON $\text{Si}(111)$

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ABSTRACT

We report electron-radiation-induced epitaxial growth of CoSi_2 on $\text{Si}(111)$ from an amorphous Co/Si 1:2 mixture with epitaxial CoSi_2 nuclei. Under the electron beam of a Philips EM430 electron microscope, the epitaxial nuclei grow parallel to the surface with a growth rate orders of magnitude higher than that for thermally activated growth. The substrate temperature during irradiation and the electron energy dependence were studied. Electron-radiation-induced growth shows very weak temperature dependence in the temperatures between 100°K and 300°K and the activation energy is 0.03 eV. The growth rate increases significantly as the electron energy increased to 200 KeV which is about the threshold energy for displacing Si atoms.

INTRODUCTION

Modification of the microstructure of thin films by energy beams has been extensively studied. Electron beams and lasers have been used for rapid surface heating.[1] Ion beams at energies of 10 to 10^3 KeV have been widely applied to thin film processing such as surface heating, ion-implantation and ion mixing. Recently, ion beams have been used to enhance a number of thermally activated processes including grain growth of polycrystalline Si and Ge thin films, [2,3] diffusion of Au in amorphous Si,[4] and epitaxial growth of amorphous Si on crystalline Si.[5-7] Electrons, being charged particles, interact with the solid strongly. Generation of point defects by high-energy electrons in various semiconductors has been reported.[8-10] Electron radiation damage in metals and electron induced amorphization of alloys have been studied.[11] However, due to its small mass, the electron is not as effective in displacing atoms as ions. The effect of electron irradiation on the microstructure of thin films has not been extensively studied. In this paper, we report the electron-radiation-induced growth (ERIG) of epitaxial CoSi_2 on $\text{Si}(111)$ from an amorphous Co/Si 1:2 mixture. The ERIG is compared with the results on a thermal annealing study reported previously.[12]

EXPERIMENTAL PROCEDURE

An amorphous Co/Si mixture was prepared in a RIBER EVA 32 Si molecular beam epitaxy system with a base pressure of 3×10^{-11} Torr. A 10-nm-thick amorphous film was deposited by coevaporation of Co and Si in a 1:2 stoichiometric ratio at near room temperature from separated Co and Si sources which are controlled by a Sentinel III deposition controller. The microstructure was analysed by plan-view and cross-sectional transmis-

sion electron microscopy. The specimens for plan-view TEM were prepared by chemical thinning from the back side of the Si substrates with the surface protected by wax. Cross-sectional TEM specimens were prepared by mechanical polishing followed by 5 Kev Ar ion milling. The samples were always kept below 50°C during sample preparation procedures. TEM analysis was performed in a Philips EM430 electron microscope operating at energies between 100 KV and 300 KV. The electron irradiation was also carried out in the same microscope after the sample was made into a thin TEM specimen. The total beam current on the sample was on the order of nA. The temperature dependence of the growth was studied in the temperature range from 100°K to 300°K using a liquid nitrogen cold stage. In the area analyzed, the substrate was about 100 nm thick and the deposited layer was 10 nm. Since the substrate was an order of magnitude thicker than the CoSi₂ film, the substrate can be regarded as an infinite bulk for the deposited film.

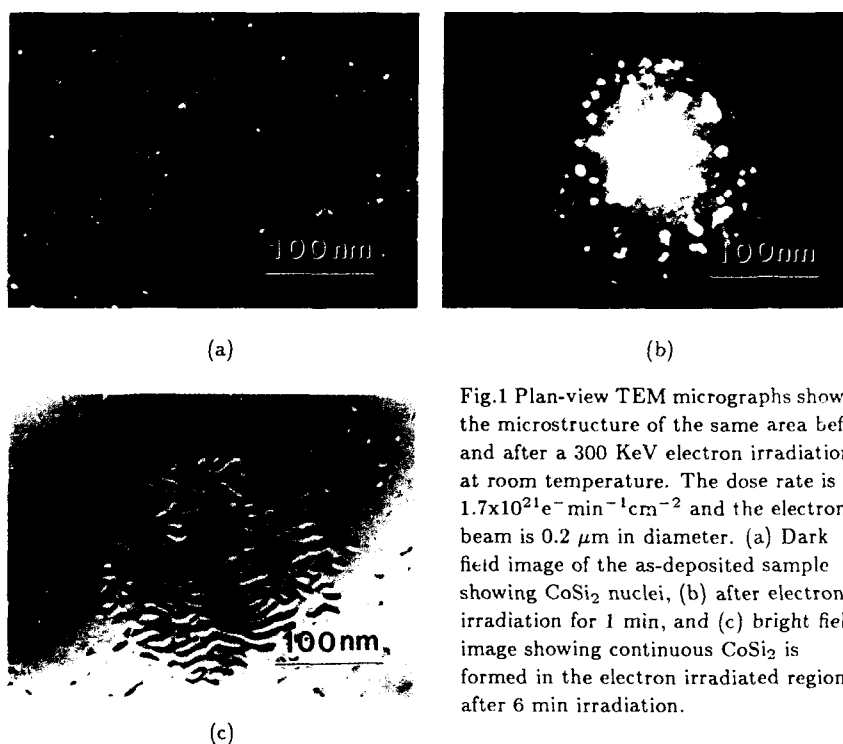


Fig.1 Plan-view TEM micrographs showing the microstructure of the same area before and after a 300 KeV electron irradiation at room temperature. The dose rate is $1.7 \times 10^{21} \text{ e}^- \text{ min}^{-1} \text{ cm}^{-2}$ and the electron beam is 0.2 μm in diameter. (a) Dark field image of the as-deposited sample showing CoSi₂ nuclei, (b) after electron irradiation for 1 min, and (c) bright field image showing continuous CoSi₂ is formed in the electron irradiated region after 6 min irradiation.

RESULTS AND DISCUSSION

Fig.1 (a) shows the microstructure of an as-deposited film. The film is mostly amorphous with crystalline CoSi₂ nuclei embedded in it. All the crystalline CoSi₂ regions are epitaxial and rotated 180° with respect to the Si substrate. Crystalline CoSi₂ nuclei are

about 7 nm in size and 20 nm apart. Cross-sectional TEM analysis shows that the crystalline CoSi_2 nuclei extend from the Si surface to the top of the as-deposited layer. Under the 300 KeV electrons bombardment, epitaxial CoSi_2 nuclei grow parallel to the surface, see Fig.1 (b). The growth is isotropic with a constant growth rate of $13\text{\AA}/\text{min}$, which is equivalent to a 160°C thermal annealing. In about six minutes, a continuous epitaxial CoSi_2 film is formed in the electron illuminated area while the CoSi_2 nuclei outside the irradiated area remain unchanged, as shown in Fig.1 (c). The dose rate on the $4 \times 10^{-2} \mu\text{m}^2$ irradiated area is $1.7 \times 10^{21} \text{e}^- \text{min}^{-1} \text{cm}^{-2}$. The distance between CoSi_2 nuclei varies from 5 nm to 50 nm, and the growth rate of each nucleus seems to be unaffected by the distance to neighboring nuclei. This indicates that the effective range for the electron-interface interaction is less than 5nm. Assuming only the electrons within 5nm from the amorphous/crystalline interface are effective in activating the atoms, one atom is removed from the amorphous phase to appear in the crystalline phase for every 10^5 electrons incident on the sample.

Due to the small cross section for 300 KeV electrons, most of the electrons go through the 10 nm deposited layer and the 100 nm substrate without losing energy. A small amount of the electrons lose energy through the interaction with atomic nuclei or atomic electrons. The energy deposition rate for KeV electrons decreases with increasing electron energy.[13] However, the experimental results shows opposite growth rate-energy dependence. Fig.2 shows the dependence of ERIG on the electron energy between 100 and 300 KeV. In this energy range the growth rate increases drastically with increasing electron energy. Electrons with energies higher than 0.1 MeV can transfer enough energy to displace atoms. The threshold energy for atomic displacement by the electrons depends on the mass and the displacement energy of the atoms. For elemental Si, assuming the displacement energy is 15 eV, the calculated threshold electron energy is about 200 eV.[13] For Si atoms in the amorphous Co/Si mixture, the threshold energy is expected to be lower since the Co-Si bonding energy is lower than the Si-Si covalent bonding energy. The probability for displacing atoms increases rapidly when the electron energy increases to near the threshold energy. The result in Fig.2 indicates that the atomic displacement caused by high energy electrons is essential for ERIG. For ion-beam-induced epitaxial growth, the energies that have been used are far beyond the energy necessary for displacing atoms, and experimental results show that the growth rate decreases with increasing ion energy.[6]

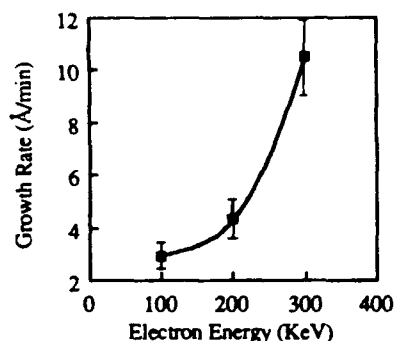


Fig.2 Rate of electron radiation induced epitaxial growth as a function of electron energy. The measurements are made at room temperature with a dose rate of $1.7 \times 10^{21} \text{e}^- \text{min}^{-1} \text{cm}^{-2}$.

The temperature dependence of the ERIG was studied for temperatures between 100°K and 300°K . The logarithm of the growth rate is plotted against the inverse of

the temperature in Fig.3. For comparison, the results for thermally activated growth are also shown in the diagram. ERIG shows a weak temperature dependence in this temperature range. The growth rate for the ERIG is orders of magnitude higher than that for thermally-activated growth extrapolated from high temperature data. The activation energy for ERIG obtained from Fig.3 is 0.03 eV, which is significantly lower than the 0.8 eV for thermally-activated growth. This reduction in activation energy is also observed in ion-beam-induced processes. For example, the activation energies for epitaxial growth of amorphous Si on Si substrate are 2.7 eV and 0.24 eV for thermal annealing and ion-induced growth, respectively. The activation energy observed in this study (0.03eV) is smaller than the activation energies for most thermal processes. This weak temperature dependence suggests a direct interface activation mechanism. The characteristics of EIG are summarized in Table 1. For comparison, the corresponding results for ion-induced epitaxial growth of Si [5] are also shown in the table.

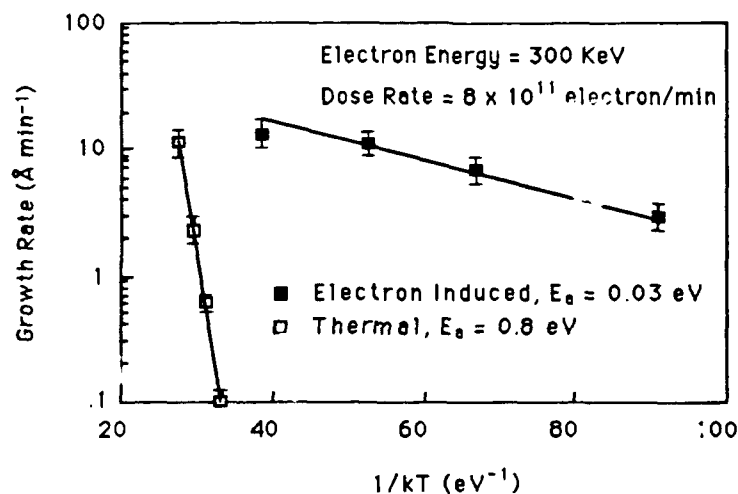


Fig.3 Electron-radiation-induced epitaxial growth of CoSi_2 as a function of temperature. The electron energy and dose rate are 300 KeV and $2 \times 10^{21} \text{e}^- \text{min}^{-1} \text{cm}^{-2}$, respectively. The irradiated area is about $4 \times 10^{-2} \mu\text{m}^2$. For comparison, the data for thermally activated growth is also shown in the diagram. The activation energy obtained from the plot is 0.8 eV for thermal annealing and 0.03 eV for electron-induced growth.

CONCLUSIONS

We report the electron-beam-induced epitaxial growth of CoSi_2 on $\text{Si}(111)$. The effect of electron energy and substrate temperature during irradiation are studied. Electron-beam-induced growth shows weak temperature dependence with an activation energy of 0.03eV at temperatures between 100 and 300°K. The growth rate increases drastically as the electron energy is increased to about 200 KeV. The mechanism for the EIG is not clear at this point. The energy dependence indicates that displacing atoms by electrons is essential for the growth and the weak temperature dependence suggests a direct interface

activation mechanism.

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Table I: Summary of the characteristics of electron-radiation-induced epitaxy. For comparison, the corresponding results for ion-beam-induced epitaxy are also listed.

	ELECTRON	ION [5]
Experimental conditions		
Energy	0.1-0.3 MeV	0.6-3 MeV
Dose Rate($\text{cm}^{-2}\text{min}^{-1}$)	10^{21}	10^{14}
Irradiated area	$0.1 \mu\text{m}^2$	cm^2
Temperature dependence	$E_a=0.03 \text{ eV}$	$E_a=0.2 \text{ eV}$
Energy dependence	Growth rate increases with increasing electron energy	Growth rate decreases with increasing ion energy
Microstructure	Same as thermally induced growth	Same as thermally induced growth
Number of particles /transferred atom	10^5 electron/atom	10^{-1} ion/atom

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**MOIRÉ PATTERN STUDIES OF THIN LAYERS DEPOSITED ON (001)Si SUBSTRATES :
CASES OF TiSi_2 and GaAs.**

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ABSTRACT

Moiré pattern images have been used to investigate the crystalline quality of thin films deposited on (100)Si substrates. Observations performed on TiSi_2 show a three-dimensional growth process and two different epitaxial modes. In the case of GaAs epilayers, it is shown that the residual strains are not uniformly distributed in the layer. Residual strain and threading dislocations are related to imperfections of the misfit dislocation network.

INTRODUCTION

The aim of this contribution is to discuss some results obtained by the moiré fringe technique on thin films deposited on (001)Si substrates. According to Hirsch et al. /1/, one of the most useful applications of this technique concerns the heteroepitaxial growth of oriented deposits on crystalline substrates.

The crystal growth performed by Molecular Beam Epitaxy or Solid Phase Epitaxy can be, in the case of large lattice mismatches, separated into two stages : firstly a three-dimensional growth appears at an early stage of the deposition. The islands grow independently and coalesce. When the coverage is complete a two-dimensional growth can develop. The growth behaviour certainly plays a very important role in the creation of defects. Two different problems of heterostructure are discussed: -i) the epitaxial modes of TiSi_2 on (001)Si for very thin films. -ii) the relationship between the epilayer defects and the misfit dislocation network in the GaAs/Si system.

EXPERIMENTAL TECHNIQUE

Moiré fringe technique

Moiré patterns are observed in electron microscope images when overlap occurs between two crystals with almost exactly equal lattice parameters. Under these circumstances moiré patterns form if a beam diffracted by both crystals is allowed to recombine to form the final image. In the case of parallel moiré patterns, the fringe periodicity D is given by

$$D = d_1 d_2 / (d_1 - d_2)$$

where d_1 and d_2 are the interplanar distances of each grain involved in this interference effect. The moiré fringes are, in this case, parallel to the reflecting planes /1/.

Moiré pattern images appear to offer a very convenient method of observing lattice imperfections in the deposited layers. They are formed by superposing a perfect and imperfect crystal and they represent a magnified image of the imperfect crystal. The images reveal the way in which

imperfections disturb the periodicity of the crystal. Then, if we assume that the silicon substrate is unaffected by the deposited layer, a variation of the moiré fringe direction indicates a local change in the orientation of the layer. A small rotation of one set of the planes can modify completely the orientation of the moiré fringes (90° for rotation moiré) /1,2/. Hence one can observe small misorientations or local strain with this method. In addition, this technique is convenient for studying the defect density in the range of 1 per 5nm.

Conditions of observation

Moiré fringes are observed when the substrate and the deposited layer overlap. A condition for obtaining clear information is that the investigated layer is monocrystalline in the growth direction. The silicon substrate is chemically etched from the rear side in order to give specimens thin enough to be observed in plane view at 200 kV.

The use of more than one diffracted beam is an advantage when beams diffracted by more than one set of crystal planes are included. This allows a two-dimensional moiré image of a crystal to be formed. In this way, all periodicities perpendicular to the electron beam are revealed on one image. In our case experimental conditions are defined as follows : the incident beam is nearly parallel to $\langle 001 \rangle \text{Si}$. More precisely, the reflexions (220), (220) and (400) are in Bragg position. Double diffraction effects occur. The bright field and the (400) dark field images show simultaneously the two perpendicular moiré fringes related to the (220)Si planes.

EPITAXIAL MODES OF TiSi_2/Si

TiSi_2 , which has the lowest resistivity among the refractory metal silicides, is of great interest. For this reason TiSi_2/Si interfaces have been extensively studied /3 to 11/. However an agreement between the different results is difficult to achieve due to the strong reactivity of Ti with contaminants which can severely alter compound formation and growth. Moreover, most studies have been focused on the formation of thick TiSi_2 films and the different resulting interfaces remain incompletely characterized from the chemical and crystallographic points of view. At least, one interesting result concerning this silicide is the existence of two different phases : the low temperature metastable phase known as the C49 structure and the high temperature C54 structure which presents the low resistivity properties.

TiSi_2 can be formed either by annealing of a titanium film deposited at room temperature or by deposition of titanium on a directly heated silicon substrate /5/. In this work, a 4nm thickness of Ti has been deposited on a $\langle 001 \rangle \text{Si}$ substrate at a temperature of 400°C under UHV conditions with a pressure in the 10^{-10} torr range /8/. At this temperature, titanium and silicon react directly to give both crystalline and amorphous titanium silicide /9,10/.

Fig. 1 shows a typical view of the sample with the e-beam nearly parallel to $\langle 001 \rangle \text{Si}$. The deposited layer is not continuous. The silicon is partially covered by silicide grains imaged by moiré patterns. They are characterized by an average size of few tens of nm. This result shows a three-dimensional growth process of the silicide. Three-dimensional growth has also been observed in situ at the end of the deposition by Auger Electron Spectroscopy and Electron Energy Loss Spectroscopy, which give at the same time both silicon and silicide signals /8/. The main result given by TEM concerns the nature of the epitaxial growth mode of the silicide on silicon. Two modes have been identified by different moiré patterns :



Figure 1 : TiSi_2 grains on (001)Si. Note the three different types of moiré fringes A, B, C.

Double moiré fringe pattern

The grains labelled A on fig. 1 are imaged by a double moiré fringe pattern. Their shape is sometimes rectangular. Each system of fringes is parallel to the (110) planes of the silicon. Double moiré patterns are uniform for the majority of grains.

Fig. 2a shows the diffraction patterns of both silicide and silicon. TiSi_2 diffraction spots are aligned with the (220)Si reflexions. The interplanar distances measured from the diffraction pattern are equal to 0.18 nm. These values correspond to both $d(200) = 0.1773$ nm and $d(002) = 0.1775$ nm of the orthorhombic structure C49 with the crystalline parameters found by Van Hontum and Raaijmakers /11/.

The interfringe D, measured on fig. 1, is equal to 2.5 nm for both moiré systems. This value is in good agreement from the value calculated with the data of the C49 structure /11/. D is found equal to 2.46 nm for (200) TiSi_2 plane and to 2.5 nm for the (002) TiSi_2 plane.

These observations show that these grains of silicide are growing by epitaxy along $\langle 001 \rangle \text{Si} // \langle 010 \rangle \text{TiSi}_2$, defined by (220)Si // (200) TiSi_2 and (220)Si // (002) TiSi_2 .

Simple moiré fringe pattern

A large number of grains, labelled B and C on fig. 1, present only one system of fringes. The B and C moiré fringes are perpendicular. They are due to the interference between the (200) TiSi_2 or (002) TiSi_2 and both (220)Si and (220)Si. The fringe periodicity D is equal to 2.5 nm. The relative orientation of such grains is deduced from the diffraction pattern. Fig. 2b shows the diffraction pattern with the electron beam parallel to $\langle 001 \rangle$ in silicon. The silicide spots are indexed as (131) and (062) as shown on fig. 2b /4/. The (062) TiSi_2 and (220)Si are simultaneously excited. The misorientation is thus characterized by (220)Si // (200) TiSi_2 and (220)Si // (031) TiSi_2 . The silicide is growing with the $\langle 001 \rangle \text{Si} // \langle 013 \rangle \text{TiSi}_2$.

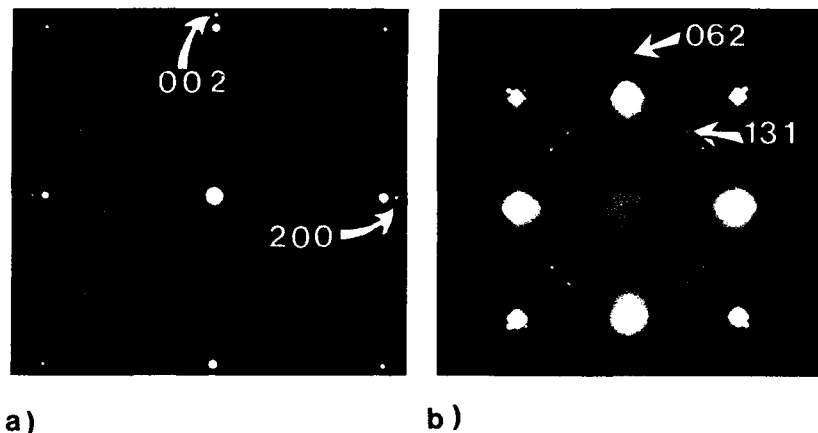


Figure 2 : Superimposed diffraction patterns of both the $\langle 001 \rangle$ silicon and TiSi_2 grains : the small spots are related to TiSi_2 . a) $\langle 001 \rangle \text{Si} // \langle 010 \rangle \text{TiSi}_2$, b) $\langle 001 \rangle \text{Si} // \langle 013 \rangle \text{TiSi}_2$.

This epitaxial mode could be explained on the basis of the lattice match concept and the geometrical CSL/DSC model as discussed by Nipoti and Armigliato and Catana et al. /3b, 6/.

The different moiré patterns observed on the same image show that the TiSi_2 is growing according to at least two different epitaxial modes. Variants are also observed as required by the symmetry consideration. A complex polycrystalline structure will certainly be obtained with a titanium layer thick enough to provide uniform silicide films.

DEFECTS IN GaAs/Si HETEROSTRUCTURE.

The heteroepitaxy of GaAs thin films on silicon substrates (GaAs/Si) has attracted considerable interest in recent years /12/. However, the density of structural defects such as dislocations, stacking faults and microtwins in GaAs/Si heteroepitaxy is still too high for some applications /12/. We would like to show that one origin of these defects propagating into the epilayer is related to the interface imperfection. For this purpose the investigated specimen is a 60 nm GaAs layer deposited on a 4° off $(100)\text{Si}$ surface. The first 10 nm has been grown by MEE (Migration Enhanced Epitaxy) at 300°C and the next 50 nm by MBE also at 300°C . In order to improve the crystalline quality of the GaAs film, the sample has been heated in situ at 640°C for 75 min. /13/.

Fig. 3 shows a plane view of this GaAs/Si interface. Note the double system of moiré fringes observed on the bright field image of fig. 3a. The direction of the fringes is parallel to the $(220)\text{Si}$ planes. The calculated moiré fringe spacing assuming bulk GaAs and Si lattice constants is 5 nm for the (220) reflection; this agrees well with the observed value.

Interfacial dislocations

Fig. 3b is a (400) weak beam image of the same area of fig. 3a. No stacking fault and microtwins are observed. We believe they disappeared during the heat treatment. The two families of perpendicular misfit

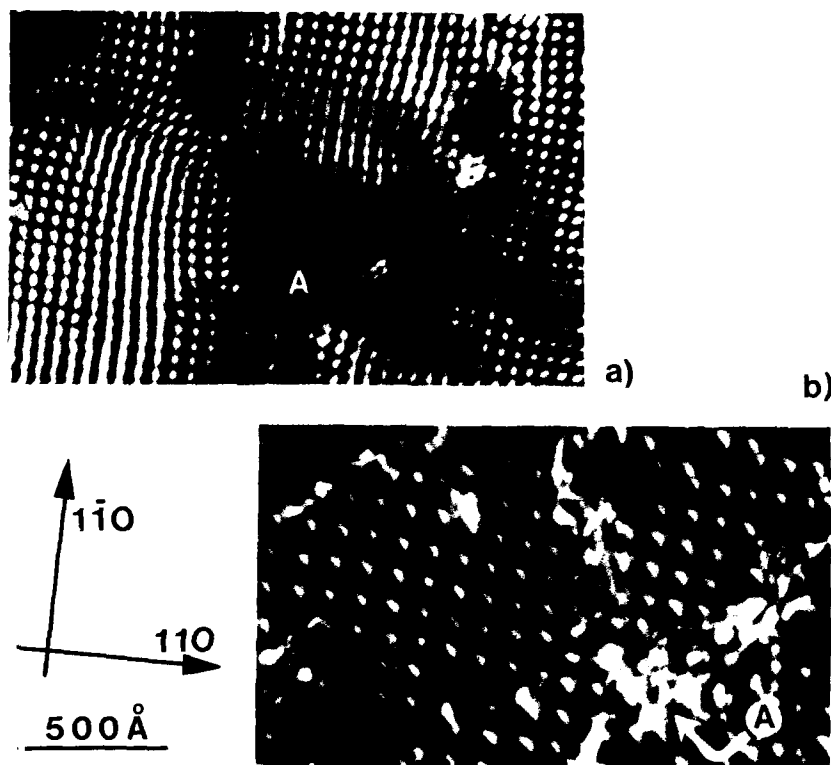


Figure 3 : Plane view of the GaAs/Si specimen a) double moiré fringes pattern. b) the (400) weak beam image shows misfit dislocations mainly characterized as Lomer dislocations. Note the limited size of the dislocation sub-networks.

dislocations are seen. These dislocations have a limited length. They have a spacing equal to 10 nm. By comparison of this value and the moiré spacing of 5 nm, the dislocations are characterized as Lomer type with a Burgers vector $1/2\langle 110 \rangle$, as found also by Ishida /14/. In addition, they are organized in small sub-networks of less than ten dislocations in each direction. Each sub-network, mainly free of defects, is probably associated with the island growth process.

It is interesting to note that the size of homogeneous moiré zones is 2 or 3 time larger than the size of misfit dislocation sub-network. Then the coalescence effect between grains can give an interaction between misfit dislocations sub-networks without emission of defects in the epilayer.

Defects in the epilayer

The moiré fringes are deformed and disappeared locally. The non uniformity of moiré fringes is related to the residual stresses and threading dislocations. A typical imperfection, arrowed A, is shown on fig. 3a. There is a direct correspondance between A on fig. 3a and the high concentration of defects observed in A on fig. 3b. It is interesting to note

that these defects are located at a boundary of the misfit dislocation sub-networks.

The defects are formed because of the different lattice constants and thermal expansion coefficients in the substrate and the epilayers. As a result of the mismatches, defects in the epilayer are formed initially during the growth process. The misfit dislocation network, necessary for the stability of the heterostructure, is not perfect as shown on fig. 3b : the dislocation length is limited to few tens of nm. The interaction between misfit dislocations from different sub-networks can generate defects merging into the epilayer. Many defects are also created during the postgrowth cooling by propagation into the epilayer. The misfit parameter, varying by 5% when the temperature decreases from 500°C to room temperature, induces stresses in the epilayer. The interface dislocations in excess are emitted to relax, at least partially, the thermal stresses. They can be blocked by defects in the interface such as boundary dislocation sub-networks. In this case, these dislocations become parallel to the growth direction and contribute then to the high defect density in the epilayer.

In conclusion, we think that the high density of defects observed in the GaAs/Si heterostructure is directly related to the imperfections in the arrangement of the misfit dislocations. In particular, this density can be a direct function of the size of homogeneous misfit dislocation sub-networks.

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PART III

The Mechanism of
Schottky Barrier Formation

NEW ELECTRONIC PROPERTIES OF METAL / III-V COMPOUND SEMICONDUCTOR INTERFACES

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ABSTRACT

Recent studies of interface states and band bending at metal / III-V compound semiconductor interfaces reveal that these junctions are much more controllable and predictable than commonly believed. Soft x-ray photoemission spectroscopy studies demonstrate a wide range of band bending for metals on many III-V compounds, including GaAs. Cathodoluminescence spectroscopy measurements show that discrete states form at the microscopic junction which can have a dominant effect on the band bending properties. Internal photoemission measurements confirm the bulk barrier heights inferred by photoemission methods. After separating out surface chemical and bulk crystal quality effects, one finds simple, predictive barrier height variations which follow classical Schottky behavior.

INTRODUCTION

The electronic properties of metals on III-V compound semiconductors exemplify the behavior of solid-state interfaces which have intrigued researchers and frustrated technologists for decades. Like many metal-semiconductor contacts, these interfaces have, until recently, exhibited only a weak barrier height dependence on the properties of the metal, contrary to the large differences in charge exchange expected between metal and semiconductor space charge region expected with differences in metal work function [1]. This insensitivity derives from the presence of trapped charge at the intimate metal-semiconductor interface, which screens the potential difference between the two materials [2]. Such trapped charge can arise from a variety of factors, including intrinsic surface states, metal wave function tunneling into the semiconductor, the presence of foreign species such as contaminants or semiconductor defects, and new dielectric phases and/or directed bonding due to chemical reaction at the microscopic junction. These factors have been the subject of many intensive studies by surface and interface-sensitive techniques over the last two decades [3-5]. Many of these efforts have shown the

importance of extrinsic phenomena, the chemical and structural interaction of metal and semiconductor, in forming interface electronic properties.

In this paper, we review recent studies of interface states and band bending at metal / III-V compound semiconductor interfaces prepared with particular attention to surface chemical and bulk crystal quality effects. We find that these junctions are much more controllable and predictable than commonly believed, especially if chemical reactions are minimized and bulk crystal quality is optimized. Soft x-ray photoemission spectroscopy studies demonstrate a wide range of band bending for metals on many III-V compounds, including GaAs. Cathodoluminescence spectroscopy measurements show that discrete states form at the microscopic junction which can have a dominant effect on the band bending properties. Internal photoemission measurements confirm the bulk barrier heights inferred by photoemission methods. After separating out surface chemical and bulk crystal quality effects, one finds simple, predictive barrier height variations which follow classical Schottky behavior.

Because of its representative III-V compound electronic properties, both scientific and technological, this paper focusses primarily on the recent interface studies of GaAs. The first section presents the band bending properties of metals on GaAs under ultrahigh vacuum (UHV) conditions for both bulk and thin film crystals, followed by sections on interface and/or native deep levels, low temperature metallization, and the implications of these findings for models of interface electronic behavior.

ROOM TEMPERATURE METALLIZATION OF GaAs

Soft x-ray photoemission spectroscopy (SXPS) is an effective method of measuring changes in band bending during the initial stages of Schottky barrier formation. Several years ago, it was found that metals on clean, ordered surfaces of the ternary III-V alloy $\text{In}_x\text{Ga}_{1-x}\text{As}$ ($0 \leq x \leq 1$) exhibited a much wider range of Fermi level (E_F) stabilization than had previously been reported [6]. These differences highlighted the importance of interface contamination and its effect on subsequent metal-semiconductor interdiffusion and reaction. Subsequently, studies of metals on UHV-cleaved GaP surfaces revealed E_F stabilization energies which spanned a wide energy range and agreed in detail with predictions of a simple Schottky charge exchange model [7]. Deviations from this ideal behavior again emphasized the importance of interface chemistry. Metals on clean, ordered surfaces of GaAs (100) prepared by molecular beam epitaxy (MBE) also displayed a wide E_F stabilization range and the effects of extrinsic phenomena [8,9]. Figure 1 illustrates the large variation

in E_F movement within the band gap as a function of metal overlayer coverage for both melt-grown (110) UHV-cleaved (Fig. 1a) and MBE-grown (100) (Fig. 1b) surfaces. These room temperature measurements exhibit several striking differences. First, the MBE-grown GaAs (110) surface exhibits a much wider range of barrier formation. Second, the E_F stabilization energies for n-type and p-type GaAs (100) appear to coincide, unlike the melt-grown case. Third, the E_F movement differs from metal to metal on the (110) surface and evolves over several monolayers, consistent with metallization features observed via SXPS, and in contrast to the (110) melt-grown case. Coupled with the III-V interface

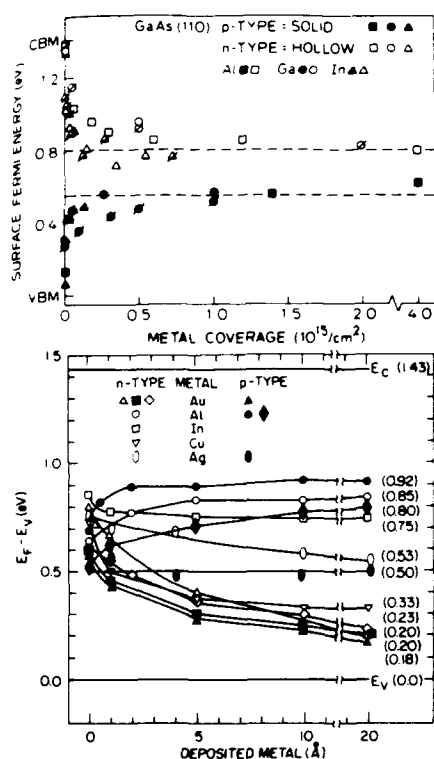


Fig. 1. Comparison of SXPS-measured E_F movements as a function of metal coverage for melt-grown (top) and MBE-grown (bottom) GaAs. Unlike the melt-grown case, MBE-grown GaAs movements exhibit a wide range of energies, nearly identical n- and p-type energies for the same metal, and an evolution at room temperature over several monolayers or more [9].

work already mentioned, these results demonstrate that the barrier height insensitivity commonly attributed to III-V materials is in fact not a representative feature of such contacts.

A self-consistent electrostatic analysis of the E_F stabilization energies [10] shown in Figs. 1a and 1b suggests a corresponding difference in the presence of deep levels at their interfaces. For the melt-grown case, the common E_F stabilization energies require a high ($\leq 10^{14} \text{ cm}^{-2}$) density of mid-gap states for all metals. For the clean, ordered, MBE-grown GaAs (100) surface, Fig. 2 illustrates the n-type barrier height (ϕ_B) dependence of different metals as a function of metal work function (ϕ_M). For semiconductor electron affinity X_{SC} , deviations from the Schottky line determined by

$$\phi_B = \phi_M - X_{SC} \quad (1)$$

can be attributed to states localized at the interface with discrete energies in the band gap. The SXPS data is sufficient to provide a unique fit to two states, located 0.2 and 0.8 eV above the valence band edge, as pictured in the inset [11,12]. Furthermore, only a low density ($3 \times 10^{13} \text{ cm}^{-2}$) of 0.2 eV acceptor states are required to account for the behavior of medium and high work function metals, whereas a high (mid- 10^{14} cm^{-2}) and metal-dependent density of 0.8 eV acceptor states are needed to match the behavior of low work function metals. The presence of such discrete states, as well as their detailed energy levels and metal dependence have in fact been confirmed experimentally, as will now be discussed.

INTERFACE AND NATIVE DEEP LEVELS

In order to detect the changes in electronic structure which occur near metal-semiconductor interfaces as they are formed, we have developed a low energy variant of the cathodoluminescence spectroscopy (CLS) technique [13]. This CLS technique provides information on new interface states, new compound dielectric compound formation, and changes in band bending as a function of metallization. Many of these changes are observed to occur at coverages beyond a few monolayers, where conventional surface science techniques are no longer effective. For example, CLS measurements of metals on UHV cleaved InP reveal that new states appear whose energies and densities evolve with coverage over nanometer thicknesses, which depend on the particular metal, and whose energies can account for the different E_F stabilization energies [14].

CLS studies of metals on GaAs show major differences between MBE- and melt-grown single crystals. Figure 3 displays CLS spectra for As capped,

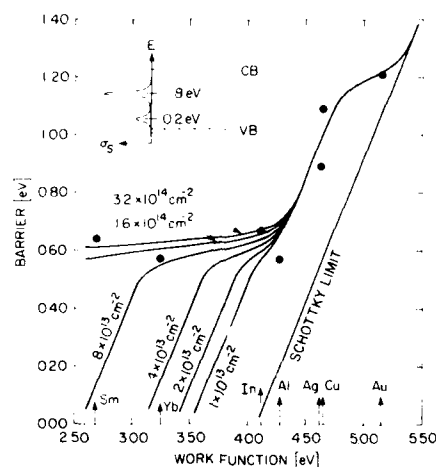


Fig. 2. Barrier heights measured by SXPS versus metal work function at room temperature. A self-consistent electrostatic analysis accounts for the entire range of behavior using two discrete energy levels located 0.2 and 0.8 eV above the valence band edge. An order-of-magnitude higher and variable density of states is needed to account for the low work function metals. CLS profiles evidence for these discrete states, their metal-dependence, and these specific energies [11,12].

thermally-cleaned, and Au-covered GaAs (100) surfaces grown by MBE. Desorption of As reduces the mid-gap emission substantially, leaving only a relatively small emission from bulk states within the band gap for the clean surface. Deposition of Au on this surface causes new emissions to appear at 0.8 and 1.25 eV [15]. The 0.8 eV level corresponds closely to the emission due to the As overlayer and suggests that the Au-GaAs interaction produces an As accumulation at the interface. (Excess As outdiffusion from GaAs into Au is observable by SXPS). The 0.8 and 1.25 eV peaks also correspond to the most likely observable transitions involving recombination to or from states 0.8 and 0.2 eV above the valence band edge [11,12], as predicted by the self-consistent electrostatic analysis.

Deposition of Al on the clean GaAs (100) surface also produces states at 0.8 and 0.2 eV, but with different relative intensities [16]. Here, the 0.8 eV state shows a decrease relative to the 1.25 eV level, due perhaps to the strong bonding

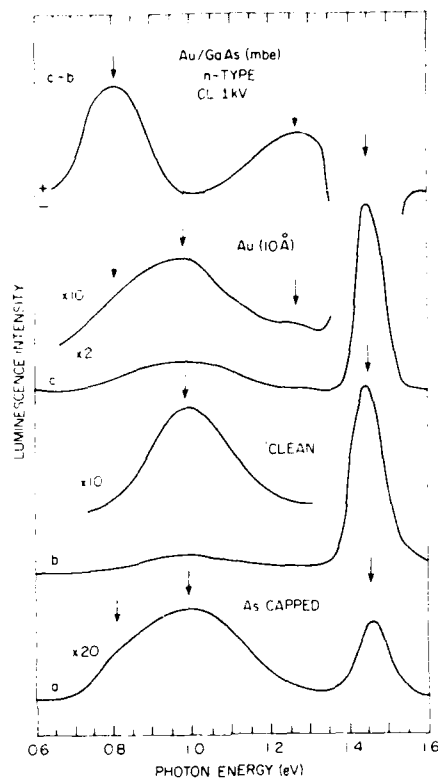


Fig. 3. CLS data for As-covered, thermally-cleaned, and Au-deposited GaAs (100) surfaces. The spectral features indicate an As-related interface state at 0.8 eV, a bulk-related state at 1.1-1.2 eV, and metal-related states at 0.8 eV and 1.25 eV. Transitions with these energies involving states near the valence band are in good agreement with the self-consistent analysis of Fig. 2 [16].

of Al with As and the epitaxial relationship of AlAs with GaAs. Indeed, annealing the Al overlayer on GaAs produces a further decrease in the 0.8 eV level. The process-dependent nature of this state is consistent with the family of density curves required to account for the low work function metals in Fig. 2.

Au and Al on melt-grown GaAs (110) surfaces produces very different behavior. Even before metal deposition, the clean GaAs (110) surface exhibits

significant mid-gap emission due to deep bulk states, most likely native defects. This is consistent with the orders-of-magnitude higher deep level defect densities of melt- versus MBE-grown GaAs [17], especially for the mid gap EL2 level [18]. Figure 4 illustrates the new CLS features for Au on melt-grown (110) GaAs [16]. In addition to the bulk-related features, an intense peak appears to dominate the spectra at energies of 0.6 to 0.7 eV, beyond the low-energy cutoff of our CLS detector. Comparison of Figs. 3 and 4 shows the orders-of-magnitude difference in mid-gap emission between the MBE-grown (100) and melt-grown (110) surfaces. Similar differences are evident for the two Al-GaAs surfaces (not shown).

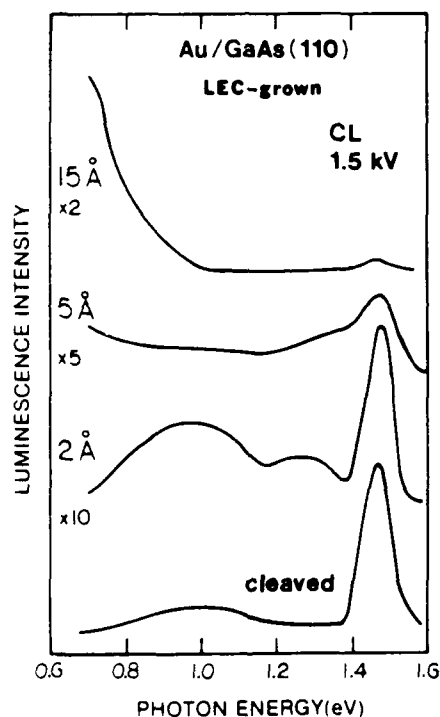


Fig. 4. CLS data for UHV-cleaved and Au-deposited melt-grown GaAs (110) surface. Besides the bulk-related features of the clean surface and the new metal-induced features above 0.8 eV, Au deposition produces a large emission feature near mid-gap which peaks below the CLS detector cutoff [15].

Bulk photoluminescence spectra of melt- versus MBE-grown GaAs suggest that differences in crystal growth can contribute to the observed differences in interface state features [16]. These bulk spectra (not shown) reveal 2-3 orders-of-magnitude higher deep level emission from the melt-versus MBE-grown GaAs. Furthermore, the deep level emission for the bulk melt-grown GaAs resides near mid-gap, where E_F stabilization is commonly reported. On the other hand, the relatively weak deep level emission for MBE-grown GaAs appears at 1.1-1.2 eV, away from mid-gap (and consistent with the bulk feature in Fig. 3).

Overall, the melt- and MBE-grown GaAs single crystals exhibit several striking differences. The MBE-grown GaAs exhibits orders-of-magnitude lower emission from bulk deep levels, orders-of-magnitude lower emission from interface states on the clean surface, and orders-of-magnitude lower emission from states with metal deposition. Concomitantly, the MBE-grown GaAs exhibits a range of E_F stabilization with different metals which extends over 0.7 eV at room temperature, compared with the 0.2-0.3 eV range measured for melt-grown GaAs.

Studies of metals on other compound semiconductors provide strong evidence for the influence of bulk deep levels on E_F stabilization and "pinning". For example, CdTe single crystals which exhibit major differences in bulk photoluminescence show corresponding differences in E_F stabilization [19-21]. Comparison of two CdTe specimens, one with relatively little bulk deep level emission and the other with a deep level near mid-gap, shows a barrier height difference of 0.2-0.3 eV for the same Au overlayer [21]. The CdTe with little mid-gap emission exhibits an n-type Au barrier consistent with the work function of Au. The CdTe with mid-gap emission exhibits an n-type Au barrier corresponding to Fermi level "pinning" at the mid-gap emission energy.

We have also shown that diffusion barriers at metal-CdTe interfaces can alter the outdiffusion of anion and cation, producing significant differences in near-interface cathodoluminescence and photoluminescence [22]. Using Yb interlayers between Au and UHV-cleaved CdTe (110) surfaces, one can substantially eliminate Te outdiffusion and reduce the amount of new mid-gap emission observed. Correspondingly, such Yb interlayers produce a major increase in n-type barrier height. Such experiments emphasize the importance of bulk deep levels on E_F stabilization, as well as the role of interface chemistry in modifying new deep level production near the interface.

LOW TEMPERATURE METALLIZATION

Several research groups have investigated the E_F movement for metals on GaAs deposited at liquid nitrogen temperatures (77-100K), where chemical interactions and metal clustering are inhibited [23]. Their studies have shown detailed E_F movements at sub-metallic coverages (less than a few monolayers) which can be explained with metal-dependent adsorbate-atom charge states. For these metals on melt-grown GaAs, the Fermi level moves to a common energy position near mid-gap for most metals above a critical thickness. For MBE-grown GaAs, Fig. 5 shows a different E_F dependence on metal at low temperature [24]. While the Fermi levels measured by SXPS for different metals appear to remain relatively unchanged with initial coverage, metallization beyond a critical coverage of several Å produces an abrupt movement to new energies. This critical thickness and the abrupt change is consistent with other studies, but the range of E_F stabilization is not. Here one observes a range of band bending which extends over 1 eV. Thus, all low temperature work indicates a final E_F stabilization occurring with metallic coverage, but the low temperature MBE-grown GaAs measurements demonstrate that such behavior is not linked with a canonical E_F "pinning" [25] position.

The low temperature barrier heights corresponding to the E_F positions shown in Fig. 5 provide strong support for a simple, Schottky dependence on work function. Barrier heights versus work function appear in Fig. 6 for the low temperature data [24]. The simple Schottky relation [26] of Eq. 1 appears as the diagonal straight line which intersects the zero barrier height axis at the electron affinity of GaAs. With the exception of Yb, for which a strong chemical reaction is evident even at 100 K, most metals follow a Schottky relation closely. Internal photoemission of the contact barriers measured thus far (Au, Al, and Cu) show good agreement with the SXPS measurements. Furthermore, Fig. 6 illustrates how these barrier heights move away from the Schottky line with room temperature annealing (Fig. 2 data points). This observation underscores the importance of controlling interface chemical reactions in achieving systematic and predictable barrier heights with different metals.

IMPLICATIONS FOR SCHOTTKY BARRIER MODELS

The data in Fig. 6 emphasizes the classical nature of metal-semiconductor for systems in which chemical interactions are minimized. The wide range of band bending and the broad, detailed agreement between measured and predicted barrier heights, with no adjustable parameters, argues strongly against models which assume a large localized dipole at the interface [25]. Such models were developed in large part to account for the narrow E_F "pinning"

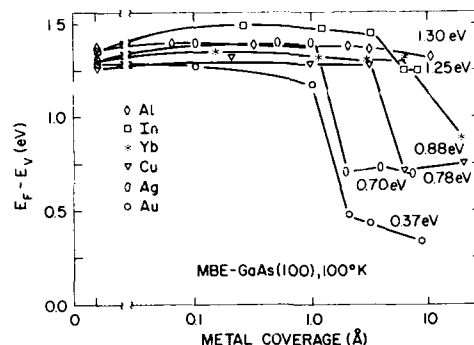


Fig. 5. E_F movements within the GaAs band gap as a function of metal coverage at low temperature on the clean (100) MBE-grown surface. All metals exhibit a plateau effect below a critical "metallic" thickness and an abrupt movement to a final stabilization energy at higher coverages. The range of E_F stabilization energies is much wider than is reported for melt-grown GaAs (110) surfaces [12].

typically reported over the past few decades. However, unless one incorporates large perturbations from a canonical starting position into such models, it is difficult for them to account for the MBE-grown, low temperature GaAs (100) data.

The trend of research in studying rectification at metal-semiconductor interfaces over the past several decades has been toward increasing levels of refinement. Early refining methods in the late 1940's provided single crystals whose interface properties could be distinguished from the bulk. In the 1960's, high vacuum chambers became available to prepare metal-semiconductor interfaces relatively free from contamination. By the mid-1970's, surface science techniques had begun to reveal the importance of surface preparation in minimizing extrinsic charge state phenomena and by the early 1980's had demonstrated the influence of chemical interaction between the constituents in forming macroscopic barriers. The recent measurements of MBE-grown III-V compounds, as well as high-quality GaP and II-VI compound semiconductors, reveals the added importance of bulk crystal quality and possibly surface

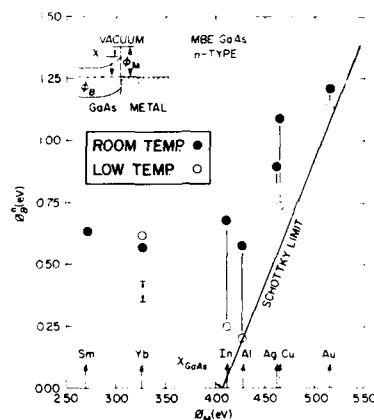


Fig. 6. Barrier heights plotted versus metal work function for MBE-grown GaAs (100) surfaces. Insert shows the comparison of parameters for the simple Schottky model. At low temperature, the SXPS measured data from Fig. 5 exhibits good agreement with the diagonal Schottky line, with deviations from the Schottky limit increasing with room temperature annealing (Fig. 2 data). The broad, detailed agreement with Schottky predictions (for all but the reactive Yb point) emphasizes the near-ideality achieved for clean metal-semiconductor interfaces for which chemical interactions have been inhibited [12].

processing in achieving near-ideal contact formation. Thus we have come full circle to the importance of material quality and, fifty years after Schottky's original proposal, we now have strong evidence for the validity of this model.

CONCLUSIONS

We have reviewed a complementary set of SXPS, CLS, bulk photoluminescence, and internal photoemission spectroscopy measurements for metals on GaAs surfaces. These studies show that a wide range of band bending is possible, contrary to conventional expectations. For all interfaces studied, we observe discrete interface states with energies which can account for F_r stabilization. For some compound semiconductor systems, we can observe the influence of bulk deep levels on E_F "pinning". For metals on high-quality, clean,

ordered GaAs (100) surfaces at low temperature, the decrease in interface reactivity leads to an increase in E_f stabilization range and a good agreement between measured barrier heights and those expected from a simple Schottky model of charge transfer.

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ELECTRICAL STUDY OF METAL/GaAs INTERFACES*

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We have carried out a systematic study of the electrical properties of Schottky barriers formed on atomically-clean and contaminated n-type and p-type GaAs surfaces[1-11]. Diodes were fabricated by in-situ deposition on clean GaAs (110) surfaces prepared by cleavage in ultrahigh vacuum and on contaminated surfaces prepared by cleavage and exposure to the atmosphere[1-4]. The consistent and reproducible barrier height determinations from the electrical measurements of unannealed and annealed diodes, when combined with results of transmission electron microscopy (TEM)[5,6] and surface sensitive studies on identically prepared samples[7,8], are found to be a particularly critical test of models of Schottky barrier formation. A strong correlation between annealing-induced changes in the Schottky barrier height and the stoichiometry of the near-interfacial GaAs is found.

In an open system, Au reacts exclusively with Ga, forming an alloy of Au and Ga. For the case of the UHV-cleaved surfaces, TEM micrographs[5,6] and surface analysis by laser ionization (SALI)[9] results have shown that a higher concentration of Ga in the Au overlayer and a significant excess of As released by the reaction and trapped near the interface has been detected. For this system, a 120 meV decrease in the Schottky barrier height on n-type material is found after annealing[2]. In contrast, in the Ti and Al systems the selective reaction between the metal and the As, with the subsequent release of Ga at the interface, is expected. For both systems, the Schottky barrier height on n-type material is found to increase by over 80 meV after annealing[3,4]. In the case of Ag deposited on atomically clean n-GaAs, no chemical reaction has been observed and no significant change in the Schottky barrier is found[2]. For diodes formed on air-exposed surfaces, significantly different chemistry can occur due to the contamination. However, in the cases where the effects of chemical reactions between the metal, semiconductor and the interfacial contamination layer is taken into account, the same correlation is found between the interfacial chemistry and the changes in Schottky barrier height upon annealing[10].

The correlation between the release of As (Ga) by the chemical reaction at the interface and a decrease (increase) in the Schottky barrier height is strong evidence for the importance of stoichiometric-related defects such as the As_{Ga} antisite in Fermi level pinning. Further support of the importance of this defect in Fermi level pinning comes from the fact that (a) the anion antisite has been shown experimentally to have two energy levels which coincide with the 0.25 eV range in Fermi level pinning positions found for metals on GaAs, (b) theoretical predictions of the anion antisite energy are consistent with the interface Fermi level pinning position for metals deposited on GaAs, InP , $Al_xGa_{1-x}As$ and $In_xGa_{1-x}As$, (c) the anion antisites have a small energy of formation and (d) are surprisingly stable at high annealing temperatures once formed.

Replacing a group III with a group V atom, the As_{Ga} is a double donor. To account for the pinning positions for metals deposited on n-type and p-type GaAs surfaces, a spectator acceptor defect (e.g. the Ga_{As}) which is believed to typically be found in smaller concentration, has been proposed[3,7,8,11]. With this model, an understanding of the changes in barrier height which occur upon annealing is straightforward. For metals which selectively react with Ga and release As

at the interface, an increase in the As_{Ga} donor concentration would be expected. The movement of the interface Fermi level toward the conduction band caused by the increased number of donors is consistent with the decrease in the Schottky barrier height on n-type material. In contrast, for metals which selectively react with As and subsequently release Ga at the interface, a decrease in the As_{Ga} donor concentration and increase in the acceptor concentration would be expected. The movement of the Fermi level toward the valence band due to the decreased number of donors and/or increase in the number of acceptors is consistent with the increase in the Schottky barrier height on n-type material.

To add further justification of this model, we will address several key issues. First, we must identify the source of the excess-As at the interface. As has been recently reported, commercial bulk-grown LEC GaAs is As-rich. The excess-As which is found in these crystals is believed to exist in part in very mobile As interstitials[12]. Because the diodes in this study were formed on bulk-grown LEC GaAs, the excess-As at the interface may come from the excess-As in the bulk and/or any As released by the reaction at the interface. Further evidence that excess-As occurs and is in a mobile form at room temperature comes from a study which reported that large As clusters can be found on the surface of bulk-grown GaAs crystals after cleavage[13].

The attraction of non-stoichiometric defects by the local strain fields at the interface may be responsible for the formation of the excess-As at the metal/semiconductor junctions in our study; similar to a proposed mechanism of the large concentration of excess As (and in particular the EL2 defect) which has also been found around single dislocations[14].

Our discussion of metal/semiconductor junctions has not covered cases in which stoichiometry-related defects such as As_{Ga} do not seem to play a role. Examples for such cases are early stages of metal deposition at cryogenic temperatures[15], metal contacts deposited in-situ on MBE grown III-V material [Brillson et. al., these proceedings], or contacts produced by cluster deposition [Weaver et. al., these proceedings]. The pinning position reported in these cases are generally outside the range of 0.5 to 0.7 above the valence band maximum which is given by the energy levels of As_{Ga} . The ability to produce Schottky contacts under conditions in which stoichiometric conditions are maintained at the interface is important. Nevertheless, we have shown strong experimental evidence that Schottky contacts deposited on commercial bulk GaAs, which is grown As-rich, with methods such as thermal evaporation or sputtering, which release considerable by sublimation and/or reaction, are indeed dominated by defects such as As_{Ga} . This class of Schottky contacts includes most notably contacts prepared in commercial GaAs device technology, which all show Fermi level pinning in the range of 0.5 to 0.7 above the valence band maximum.

* This article is an extended abstract which summarizes references 1-11.

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**METAL-SEMICONDUCTOR INTERFACES WITH NOVEL
STRUCTURAL AND ELECTRICAL PROPERTIES: METAL CLUSTER DEPOSITION**

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Studies of Schottky barrier formation at metal-semiconductor interfaces have been complicated by the difficulty of producing an abrupt, "ideal" interface. The commonly used methods of producing metal-semiconductor interfaces result in complex interfacial morphology and chemistry including substrate disruption, atomic interdiffusion, alloy or compound formation, and substrate surface structural changes. The complicated nature of such interfaces makes it difficult from a fundamental point of view to identify the mechanisms dominating Schottky barrier formation for the various stages of development.

A number of models have been proposed to explain Schottky barrier formation at interfaces grown by atom-by-atom deposition techniques. They include models based on adsorption-induced defect formation,¹ interface chemistry,² effective work function,³ metal-induced gap states,⁴ and bulk semiconductor crystal quality.⁵ Recently, a number of studies of Schottky barrier formation at low temperature (60-200 K) were performed in an attempt to inhibit certain interfacial interactions and thereby isolate the effects of other interactions on Schottky barrier formation.⁶⁻⁹ These studies established that metal clustering and atomic interdiffusion are inhibited at low temperature, but several of the investigations^{8,9} demonstrated temperature independent adatom-induced disruption of the substrate with little simplification of the interface morphology and chemistry. The primary difference between interfaces formed at 60 K and 300 K was found to involve the distribution of the liberated substrate atoms in the evolving interface. This redistribution was usually kinetically limited so that the disrupted substrate atoms were trapped near the interface at 60 K, but were able to outdiffuse toward the vacuum interface at 300 K. These studies also revealed temperature- and bulk-concentration-dependent Schottky barrier evolution which has led to significant rethinking of surface phenomena and band bending.¹⁰⁻¹³

In an effort to create more "ideal" boundary regions, we have developed a method of producing abrupt, defect-free interfaces.⁹ Our approach has been to buffer the substrate from the

impinging atom flux and thereby avoid complications at the surface due to adatom impact and coalescence. To achieve this, we first covered the clean substrate with a thin layer of Xe. Metal atoms were then condensed onto this Xe buffer layer at 60 K, and the buffer layer was desorbed by warming the sample. This resulted in the deposition of rather large, preformed metallic clusters on atomically clean surfaces. Preliminary electron microscopy and lattice imaging studies of clusters formed by depositing 7 Å of Au on GaAs(110) showed distributed metal islands on atomically flat surfaces with characteristic dimensions of ~100 Å along the surface and ~50 Å thick.¹⁵

Photoemission studies of Al, Ag, Au, Ga, Ti, and Co clusters grown on GaAs(110) show unique Fermi level positions ~0.3 and 1.0 eV below the conduction band minimum for n- and p-type substrates, resp., with energies that are nearly metal- and coverage-independent. Remarkably, we find no evidence for metal-induced gap states or conventional midgap adatom-induced defect levels despite the fact that the clusters are metallic in character. Detailed analysis of the substrate core level spectra shows that cluster deposition produces a defect-free boundary for GaAs(110). Results for cluster deposition on InP(110) show greatly reduced disruption compared to atom-by-atom deposition. In contrast, conventional metal atom deposition produces diverse and metal-dependent interfacial interactions. We believe that the differences in E_F position produced by cluster and atom deposition are related to the loss of surface relaxation under the clusters and around their perimeter and the consequent presence of intrinsic GaAs surface states in the gap. This is supported by recent scanning tunneling spectroscopy measurements that show states in the gap near the perimeter of clusters.

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EFFECT OF Si AND Ge INTERFACE LAYERS ON THE SCHOTTKY BARRIER HEIGHT OF METAL CONTACTS TO GaAs

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ABSTRACT

A new approach for extending the range of the Schottky barrier height ϕ_B of metal contacts to (100) GaAs is described. Very thin (~ 10 - 30\AA) heavily n-type and p-type Si or Ge interlayers are found to directly alter the GaAs interface Fermi energy E_F . X-ray photoemission spectroscopy is used to determine E_F during contact formation and the corresponding ϕ_B for thick contacts is measured by electrical methods. In an appropriate structure the ϕ_B range for contacts to n-type GaAs is ~ 0.25 to 1.0 eV. For p-type GaAs ϕ_B has been increased to as much as 0.9 eV. This method of ϕ_B control can be used for both Schottky barrier contact and nonalloyed ohmic contact applications. The results are interpreted in terms of a simple heterojunction model.

INTRODUCTION

Conventional metal contacts to GaAs generally have a Schottky barrier height ϕ_B of 0.7 - 0.9 eV for n-type material and 0.5 - 0.6 eV for p-type material. Within these narrow ranges, the barrier height does not appear to depend on the metal work function or details of the various metal/GaAs interface chemical reactions. In many GaAs device applications an increase or decrease in barrier height beyond the limits of ordinary contacts is desirable. For example, the resistance of tunnel ohmic contacts is greatly reduced if the contact barrier is lowered while an increase in gate Schottky barrier height can benefit field effect transistor performance.

In this paper we review our recent work in which the barrier height range for metal contacts to both n-type and p-type GaAs is significantly widened by inclusion of a very thin (~ 10 - 30\AA), heavily doped Si or Ge interface layer to influence the interface Fermi energy E_F [1-5]. Only a relatively brief description and discussion of the experimental procedures and results are given; for a more complete account the publications given in the references should be consulted. The E_F movement within the GaAs band gap at the various contact interfaces is discussed in terms of a heterojunction model where GaAs interface states are compensated by the dopants associated with the semiconductor interlayer.

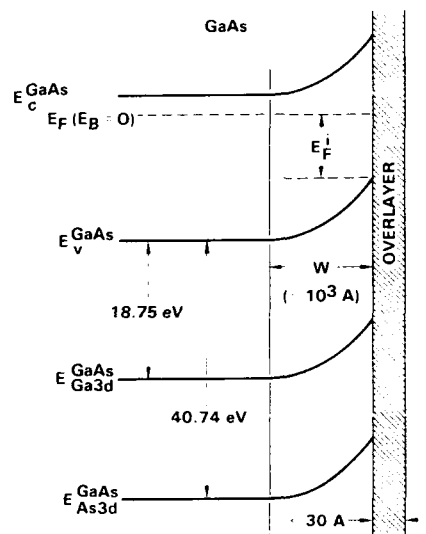
EXPERIMENTAL TECHNIQUES

X-ray photoemission spectroscopy (XPS) was used to obtain E_F^i and interface composition during initial contact formation which involves deposition of thin overlayers onto clean GaAs surfaces. The contact interfaces were prepared under ultrahigh vacuum (UHV) conditions within the XPS system. Figure 1 is a schematic band diagram of an overlayer/GaAs (n-type) interface with accompanying band bending that extends into the GaAs bulk. If the overlayer thickness is comparable to the effective XPS photoelectron escape depth for our system ($\sim 16\text{\AA}$), the Ga 3d and As 3d core level peaks from the GaAs at the interface can be monitored (the photoelectron escape depth is much smaller than the band bending distance).

The value of E_F^i is obtained from the relation $E_F^i = E_{\text{Ga}3d} - 18.75$ eV, or from $E_F^i = E_{\text{As}3d} - 40.74$ eV, where 18.75 ± 0.03 and 40.74 ± 0.03 eV are the respective Ga 3d and As 3d core level to valence band maximum binding energy differences in GaAs [6]. For overlayers that involve a metal, the Schottky barrier height is $\phi_B = 1.43 - E_F^i$ eV for n-type GaAs and $\phi_B = E_F^i$ for p-type. The thick contacts were formed on the same interfaces characterized by XPS by depositing $> 2000\text{\AA}$ of additional metal in UHV; the ϕ_B was measured by conventional current-voltage (I-V) and capacitance-voltage (C-V) methods.

Fig. 1

Schematic band diagram of overlayer/GaAs interface that illustrates the use of XPS to measure E_F^I by using the Ga 3d and As 3d core levels in GaAs.



For a given sample, the electrical measurements were performed on an array of circular 2.54×10^{-2} cm diameter contacts defined by photolithography and etching. The GaAs material is $\sim 5 \times 10^{16}$ cm $^{-3}$ bulk grown (100) n-type and p-type. Prior to contact formation, the GaAs was etched in 4:1:1 H $_2$ SO $_4$:H $_2$ O $_2$:H $_2$ O solution; the resulting native oxide was removed by momentary heating in UHV to the minimum temperature necessary ($\sim 575^\circ\text{C}$). Si and Ge interlayers were doped heavily n-type by evaporation in an overpressure of As $_4$ or P $_2$ [designated Si(As), Si(P), Ge(As), and Ge(P)]. Heavily p-type Si was obtained by Ga incorporation [Si(Ga)] or B incorporation [Si(B)]. Heavily p-type Ge results from evaporation in a vacuum [Ge(vac)].

RESULTS

Contacts to n-type GaAs with Ge Interlayers

Figure 2 compares representative Ga 3d core level spectra for several samples with thin Ge(vac), Ge(As), and Ge(P) overlayers (peak heights are normalized). The vertical reference line marks the center of the Ga 3d peak (a) of a clean surface. Spectra (b) and (c) are for thin layers of Ge(vac) deposited at 325 and 250 $^\circ\text{C}$, respectively; a shift to lower binding energy occurs (referring to Fig. 1, a core level shift to lower binding energy represents a decrease in E_F^I and a corresponding increase in n-type GaAs band bending). Spectrum (d) is for the sample of spectrum (c) after an additional deposit of 23 Å of Ge(As). A large shift to higher binding energy (increased E_F^I) is evident. A similar large shift to higher binding energy is obtained for Ge(P) deposition onto a clean surface, spectrum (e).

A summary of XPS E_F^I measurements is given pictorially in Fig. 3 for a number of n-type GaAs samples with ~ 10 Å Ge overlayers, grouped into sets (a)-(d) according to the Ge deposition conditions. The average E_F^I value for set (a), which involves Ge(vac) overlayers, is ~ 0.6 eV. Also shown is the result of exposure of a Ge(vac) overlayer sample to an As $_4$ overpressure after the Ge(vac) deposition; no significant change in the below mid-gap E_F^I is observed. In marked contrast to set (a), deposition of Ge(As) overlayers, as shown in set (b), produces an average E_F^I of ~ 1.1 eV, with maximum

Fig. 2

XPS Ga 3d core-level spectra for several n-type GaAs (100) samples with thin Ge overlayers. The overlayer composition and deposition temperatures are noted. Spectrum (d) is for the sample of spectrum (c) with the addition of a Ge(As) layer.

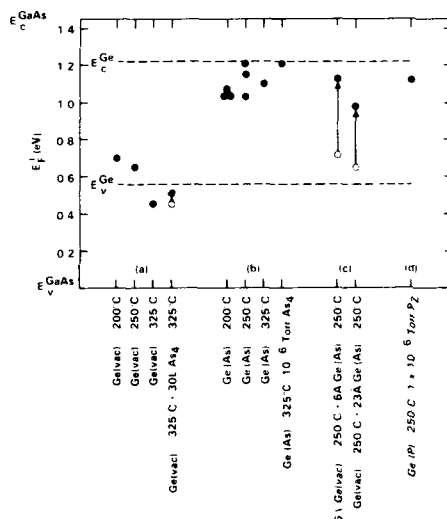
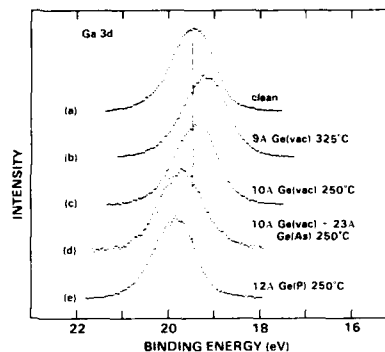


Fig. 3

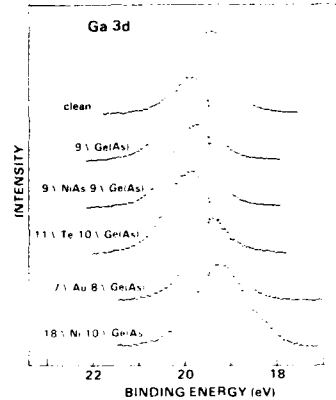
Summary of E_F^i measurements that involve Ge overlayers on n-type GaAs (100). Overlayer characteristics are given at bottom of figure. Unless noted, overlayer thickness is $\sim 10 \text{ \AA}$ and depositions intended to incorporate As or P were made in 10^{-7} Torr background pressure of As_4 or P_2 : (a) deposition in vacuum; (b) deposition in As_4 ; (c) initial deposition in vacuum followed by deposition in As_4 , and (d) deposition in P_2 .

values of 1.2 eV. Set (c) demonstrates that an initial low E_F^i state of the Ge(vac) overlayer is changed to a high E_F^i state upon an additional deposition of a Ge(As) overlayer. This result indicates that the high E_F^i values are because of As incorporation in the Ge overlayer rather than possible As accumulation at the Ge/GaAs interface. The 1.12 eV E_F^i of set (d) for the Ge(P) overlayer shows that the low band bending state is not unique to Ge(As) overlayers but is caused by the incorporation of a n-type dopant into the Ge.

The large E_F^i values in Fig. 3 suggest that low 0.2-0.4 eV barrier contacts that include a Ge(As) or Ge(P) interlayer can be achieved if the low band bending condition at the thin Ge/GaAs interface is retained when additional contact material is deposited. The Ga 3d core level spectra in Fig. 4 show examples of such depositions. The third (from top) peak is for NiAs [7], a conductive nonmetal, deposited onto the high E_F^i Ge(As) interface represented by the second peak; there is essentially no change in E_F^i . Similarly, no E_F^i shift occurs, fourth spectrum, upon deposition of Te (also a conductive nonmetal) onto a another high E_F^i Ge(As) overlayer. In comparison, the effect of Au or Ni deposition onto a high E_F^i Ge(As) overlayer is quite different, as seen in the lower two spectra.

Fig. 4

XPS Ga 3d core-level spectra for various thin overlayer structures on initially clean n-type GaAs (100) surfaces. Upper three spectra are for successive depositions on the same sample.



With both metals, E_F^i decreased by ~ 0.4 eV; that is, the low barrier condition was removed (the appearance of the low binding energy shoulder in the bottom peak is owing to a Ni-GaAs interface chemical reaction).

Based on the XPS results, the contact structures shown in Fig. 5 were fabricated to investigate how a thick low barrier contact can be made via use of a heavily n-type Ge interlayer. In each structure an initial Ge overlayer is followed by the indicated room temperature depositions. Contacts without the Ge interlayer, designated ideal, have Au, Ni, or NiAs deposited directly onto clean GaAs. Table I lists the I-V measured barrier height ϕ_B for several representative contacts with these structures. The XPS and I-V results are in accord. The Au-NiAs-Ge(Ar) and Au-Te-Ge(Ar) contacts that have a ~ 1.0 - 1.2 eV E_F^i because of the Ge(Ar) interlayer also have a low ~ 0.25 - 0.4 eV ϕ_B . In contrast, without the intervening NiAs or Te layer the Au-Ge(Ar) and Ni-Ge(Ar) contacts that had a high E_F^i prior to metal deposition have a high ϕ_B of ~ 0.6 - 0.8 eV. By using the data in Table I, ϕ_B values can be compared to those for ideal Au and Ni contacts and contacts where a Ge(vac) interlayer was used. Thus, a high E_F^i value obtained with a Ge(Ar) layer can be preserved by a NiAs or Te layer that prevents the thick contact metal from interacting with the Ge(Ar)-GaAs interface.

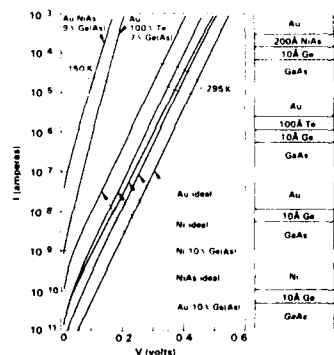


Fig. 5

Representative I-V data for a selection of contacts to n-type GaAs that have a variety of structures (contact area = 5×10^{-4} cm²). Multilayered contact structures are shown schematically on right.

Table I. Schottky Barrier Height for Contacts to n-type GaAs (100) Which Contain a Thin Ge Interlayer

Contract Structure	ϕ_B^{IV} (eV)
Au-NiAs-9Å Ge(As)	0.31
Au-NiAs-11Å Ge(As)	0.35
Au-NiAs-9Å Ge(As)	0.39
Au-100Å Te-10Å Ge(As)	0.23
Au-100Å Te-9Å Ge(As)	0.39
Au-100Å Te-7Å Ge(As)	0.36
Au-10Å Ge(As)	0.76
Au-8Å Ge(As)	0.61
Au-9Å Ge(As)	0.64
Ni-10Å Ge(As)	0.81
Au-100Å Te-9Å Ge(vac)	0.65
Au-9Å Ge(vac)	0.71
Au-100Å Te	0.79
NiAs-ideal	0.80
Ni-ideal	0.84
Au-ideal	0.89

The contact resistance ρ_c for a tunnel ohmic contact to n-type GaAs is $\rho_c \propto \exp(\phi_B/kT) / N_D$, where N_D is the donor concentration ($> 5 \times 10^{18} \text{ cm}^{-3}$) and $a = 5 \times 10^{10} \text{ cm}^{-3} \text{ eV}^{-1}$ [8]. The contact structures with low ϕ_B thus indicate that low ρ_c nonalloyed contacts to n-type GaAs can be designed by using thin, heavily n-type, Ge interlayers if interface composition is properly controlled. Although the present results used thick Au as the contact metal, it is expected that a number of other metals would also be suitable for low barrier contacts when used in a similar multilayer structure.

Contacts to n-type GaAs with Si Interlayers

Figure 6 shows As 3d core level spectra (normalized peak heights) that demonstrate the wide range in E_F that can be obtained from deposition of Si(Ga), Si(B), and Si(P) overlayers onto clean n-type GaAs surfaces (upper two peaks are for the same sample). The vertical line through the clean surface peak at 41.52 eV binding energy corresponds to $E_F = 0.78 \text{ eV}$ (the average clean surface E_F for a large number of samples is 0.79 eV). The difference in As 3d binding energy between the Si(P) and the Si(Ga) overlayers represents a E_F difference of 0.75 eV. Figure 7 gives the values of E_F for ~10-30Å Si overlayers with either Ga, B, As, or P incorporation deposited onto clean GaAs n-type surfaces at substrate temperatures between 200-350°C. The maximum range in E_F for the Si-GaAs interfaces in Fig. 7 is given by the 0.90 eV difference between a 0.33 eV value for a Si(Ga) overlayer and the 1.23 eV value for a Si(As) overlayer.

Retention of the low E_F values at the Si(Ga)-GaAs and Si(B)-GaAs interfaces after deposition of a metal would suggest the possibility of Schottky barrier contacts with ϕ_B of 1 eV. In Fig. 8 the top three As 3d peaks are for successive depositions of Si(Ga) and Au overlayers onto a clean GaAs surface; essentially no change in peak binding energy, and thus E_F , has occurred after the Au deposition ($E_F = 0.32 \text{ eV}$). Similarly, the bottom peak at 41.12 eV for a Ti overlayer has a low E_F of 0.38 eV. Table II lists the ϕ_B measured for thin metal overlayers of Au-Si(Ga), Ti-Si(Ga), and Au-Si(P) contacts (the Cr ϕ_B was not measured because of As 3d and Cr 3p peak overlap). Thus, deposition of a metal does not increase the low E_F values established at the Si(Ga)-GaAs interfaces. There is, however, a slight ~0.1 eV decrease in E_F for the Au-Si(P) contact. The XPS measurements thus predict a large ~1 eV ϕ_B for thick contacts to Si(Ga)-GaAs and a small ~0.4 eV ϕ_B for contacts to Si(P)-GaAs.

Fig. 6

XPS As 3d core-level spectra for thin p-type and thin n-type Si overlayers deposited on clean n-type GaAs (100) surfaces.

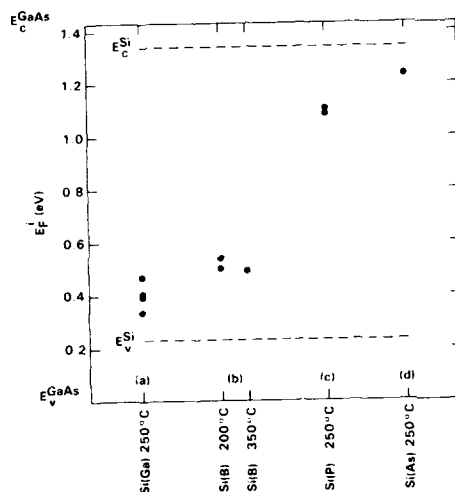
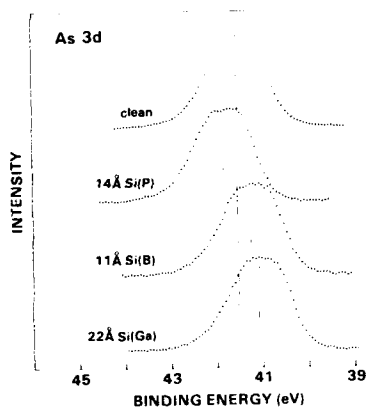


Fig. 7

Summary of E_F measurements that involve Si overlayers on n-type GaAs (100). Overlayer thickness range is from 11 to 28 Å. Si deposition temperatures are noted.

Fig. 8

XPS As 3d core-level spectra for various thin overlayers deposited on clean n-type GaAs (100) surfaces.

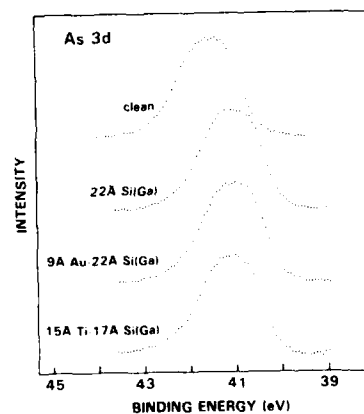


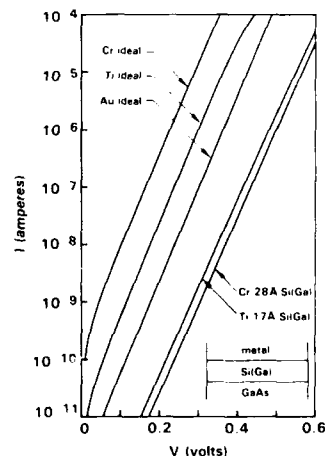
Table II. Schottky Barrier Height for Contacts to n-type GaAs (100) Which Contain a Thin Si Interlayer

Contact Structure	XPS ϕ_B (eV)	IV ϕ_B (eV)	CV ϕ_B (eV)
Au-22Å Si(Ga)	1.11	1.01	1.01
Cr-28Å Si(Ga)	-	0.99	1.10
Ti-17Å Si(Ga)	1.05	0.98	1.14
Ti-26Å Si(Ga)	1.01	0.97	1.06
Cr-24Å Si(B)	-	0.92	0.97
Au-14Å Si(P)	0.43	0.53	0.46
Au-25Å Si(P)	0.42	0.49	0.42
Au-ideal		0.89	
Cr-ideal		0.76	
Ti-ideal		0.83	

Figures 9 and 10 show a selection of I-V data for a variety of thick Schottky barrier contacts that include structures shown in the insets. The Au, Cr, and Ti contacts with a Si(Ga) or Si(B) interlayer have a barrier height significantly larger than that of the corresponding ideal metal contact. Consistent with the high E_F for the Si(P)-GaAs interface (Fig. 7) the Au-Si(P) contact has a low barrier height. Table II lists the ϕ_B measured by I-V and C-V methods for metal contacts to n-type GaAs that include a Si interlayer and for comparison the ϕ_B for ideal contacts with the same metals. The electrical measurements of ϕ_B are thus consistent with the XPS measurements. A large 1 eV ϕ_B is measured for the metal-Si(p-type)-GaAs contacts, independent of the contact metal, and a small 0.5 eV is measured for the metal-Si(n-type)-GaAs contact.

Fig. 9

Representative I-V data for Cr-Si(Ga) and Ti-Si(Ga) contacts to n-type GaAs (100) compared to the corresponding ideal contacts (contact area = $5 \times 10^{-4} \text{ cm}^2$).



Contacts to p-type GaAs with Si and Ge Interlayers

The Ga 3d core level data in Fig. 11 demonstrate the range in E_F that can also be obtained with Si and Ge overlayers on p-type GaAs (normalized peak heights). The figure inset illustrates the XPS E_F measurement for p-type material, where the interface band bending is downward in contrast to n-type material. An increase in Ga 3d binding energy thus corresponds to an increase in band bending. The vertical line in Fig. 11 is through

Fig. 10

Representative I-V data for Au-Si(Ga), Cr-Si(B), and Au-Si(P) contacts to n-type GaAs (100) (contact area = $5 \times 10^{-4} \text{ cm}^2$).

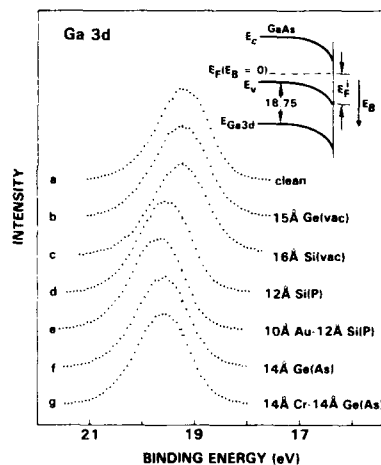
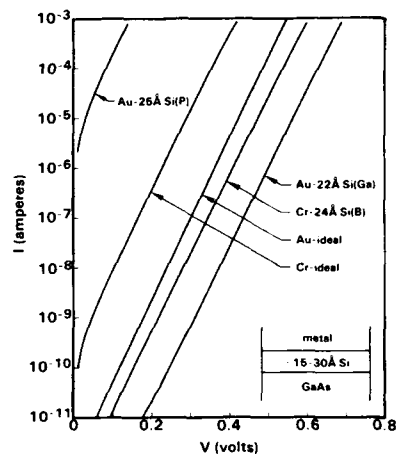


Fig. 11

XPS core-level spectra for various thin overlayers on clean p-type GaAs (100) surfaces. Inset shows the relationship between the Ga 3d binding energy and E_F .

the center of the clean surface peak (a) and corresponds to an E_F^1 of 0.49 eV (the average p-type clean surface value for a large number of samples is 0.54 eV).

Peak (b) in Fig. 11 is for Ge(vac) deposited onto the clean surface represented in spectrum (a), and peak (c) is for Si(vac) deposited onto another sample. For both peaks essentially no shift from the clean surface E_F occurs. There is, however, a distinct movement to higher binding energy for both a Si(P) overlayer, peak (d), where $E_F = 0.82$ eV, and a Ge(As) overlayer, peak (f), where $E_F = 0.87$ eV. Figure 12 gives the values of E_F obtained for a number of p-type GaAs samples upon which were deposited - 15Å overlayers of the indicated Si and Ge overlayers. Comparison of sets (a) and (b) indicates that Si(As), Si(P), Ge(As), and Ge(P) have similar E_F values of 0.77 to 0.90 eV, with an average value of 0.83 eV.

The effect of depositing a metal (Au, Cr, Mn, Ni, and Al) onto the large E_F^1 Si(n-type) and Ge(n-type) overlayers is somewhat complex. Spectrum (e), $E_F = 0.96$ eV, in Fig. 11 is with 10Å Au deposited on the sample of peak (d); and spectrum (g), $E_F = 0.86$ eV, is with 14Å Cr on the sample of peak (f). Thus, E_F (ϕ_B) either slightly increased (Au) or was essentially unchanged (Cr) with these metals. Table III lists ϕ_B for various contact structures. The thin Au, Cr, and Mn contacts with a n-type Si or Ge interlayer have

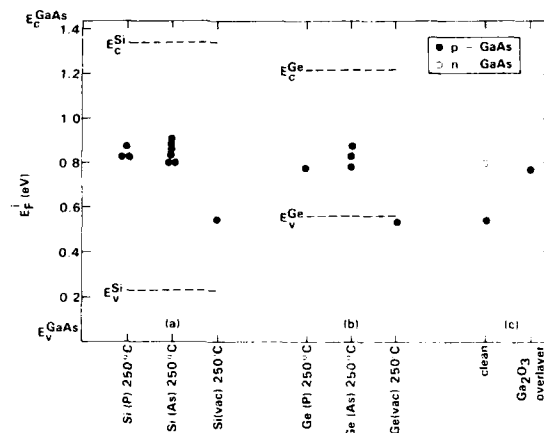


Fig. 12 Summary of several E_F^i measurements that involve various overlayers on p-type GaAs (100) surfaces (one measurement on a n-type surface is shown for comparison): (a) Si overlayers; (b) Ge overlayers; (c) clean surface and a Ga_2O_3 overlayer. Si and Ge deposition temperatures are noted.

Table III. Schottky Barrier Height of Metal Contacts to p-type GaAs (100) Which Contain a Thin Si or Ge Interlayer

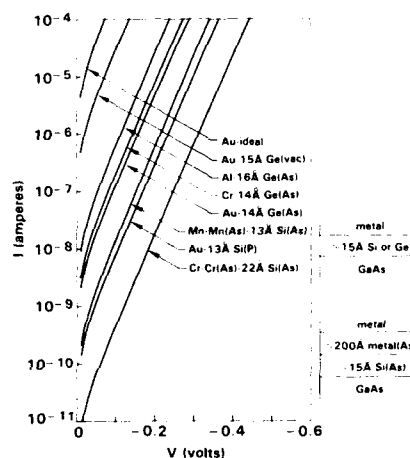
Contact Structure	XPS ϕ_B (eV)	IV ϕ_B (eV)	CV ϕ_B (eV)
Au-12Å Si(P)	0.96	0.88	1.01
Au-13Å Si(P)	0.93	0.81	0.94
Au-10Å Si(As)	0.81	0.73	0.84
Au-13Å Ge(P)	0.88	0.74	0.88
Au-14Å Ge(As)	0.83	0.73	0.86
Au-16Å Si(vac)	0.44	0.37	-
Au-15Å Ge(vac)	0.56	0.59	0.72
Cr-10Å Si(P)	0.83	0.68	0.83
Cr-14Å Ge(As)	0.86	0.72	0.89
Cr-Cr(As)-22Å Si(As)	0.93	0.88	1.04
Mn-12Å Si(As)	0.77	0.73	0.81
Mn-Mn(As)-13Å Si(As)	0.95	0.80	0.90
Ni-11Å Si(As)	0.61	0.59	0.66
Ni-Ni(As)-9Å Si(As)	0.67	0.62	0.68
Al-16Å Ge(As)	0.67	0.69	0.84
Au-ideal		0.53	
Cr-ideal		0.56	
Mn-ideal		0.56	
Ni-ideal		0.62	
Al-ideal		0.61	

XPS ϕ_B values of 0.77-0.96 eV. The Au-Si(vac) and Au-Ge(vac) contact values are significantly lower, 0.44 eV and 0.56 eV, respectively. For Mn, Ni, Al, and Cr a decrease in E_F occurs which is substantial with Al and Ni, moderate with Mn, and minor with Cr. When the initial Cr, Mn, or Ni deposition was made in an $\sim 1 \times 10^{-7}$ Torr As_4 background pressure [these metal interlayers are designated metal(As)] the E_F decrease could be prevented for Cr and Mn but not for Ni [Al(As) was not tried because AlAs is non-metallic]. The XPS measurements thus show that thin contacts to p-type GaAs which include thin Si and Ge interlayers can have ϕ_B values between 0.44 and 0.96 eV.

Representative I-V data for several of the thick interlayer contacts are plotted in Fig. 13 [data for the Au-12Å Si(P) contact overlap the Cr-Cr(As)-22Å Si(As) data]; also shown for comparison are data from a Au-ideal contact. The thick contact structures are also given in Fig. 13. Table III lists the ϕ_B values obtained from I-V and C-V data.

Fig. 13

Representative forward bias I-V data for a selection of metal contacts to p-type GaAs (100) that have a variety of interface structures (contact area = 5×10^{-4} cm²). Multi-layered contacts are shown schematically on right.



The XPS, I-V, and C-V results are in good agreement. Inclusion of a $\sim 200\text{\AA}$ metal(As) layer between the metal and the Si(As) significantly increased ϕ_B for Cr and Mn contacts, apparently by suppressing a metal/Si(As) reaction. The ϕ_B of Ni, Ni-Ni(As), and Al interlayer contacts is not significantly increased compared to the corresponding ideal contact, evidently because of a metal/interface reaction. Thus, large 0.7-0.9 eV ϕ_B Au, Cr, and Mn contacts to p-type GaAs can be achieved by inclusion of a thin, heavily n-type Si or Ge interlayer. A number of other metals should also have a similar large ϕ_B when used with the appropriate interlayer contact structure.

DISCUSSION AND HETEROJUNCTION MODEL

The XPS measurements of E_F^I during the formation of the Si and Ge interlayer contacts have demonstrated that the observed large ϕ_B variations in the electrical measurements are directly the result of corresponding E_F variations. That is, for n-type GaAs a large ϕ_B is caused by a small E_F and a small ϕ_B is caused by a large E_F . Analogously, with p-type GaAs a large ϕ_B is caused by a large E_F . This means of controlling ϕ_B is thus different in principle from methods [9] in which a variable effective ϕ_B is obtained by tailoring the impurity profile, and hence the potential, in the GaAs depletion region adjacent to a metal-GaAs interface where ϕ_B itself remains constant.

Referring to Fig. 3, the dashed lines indicate the alignment [9] of the Ge conduction band minimum and valence band maximum at a crystalline Ge/GaAs heterojunction interface. The various E_F values that we and others [11-15] have observed for Ge over-

layers on n-type GaAs lie approximately within the confines of the Ge band gap. Similarly, in Fig. 7 the Si/GaAs heterojunction band lineup is indicated [16]; the range of E_F variation for Si overlayers does not exceed the magnitude of the Si band gap. It thus appears that the location of the Ge and Si conduction and valence bands may be providing a bound on the magnitude of the E_F movement within the GaAs band gap that can be induced by the Ge and Si overlayers. We have shown that the essential condition for the large observed E_F variation at Ge/GaAs and Si/GaAs interfaces is that the semiconductor overlayer be heavily either n-type or p-type. For both Ge and Si neither a precise growth temperature nor a particular dopant is crucial. The large lattice mismatch between Si and GaAs and the generally nonepitaxial nature of the Si layers also demonstrate that the degree of interface heterojunction perfection is relatively unimportant. The mechanism for Fermi energy movement thus appears to be most directly related to the presence of a large concentration of an impurity in the semiconductor overlayer that is a n-type or p-type dopant for the overlayer (rather than a dopant for GaAs).

It is often assumed that the fairly narrow range of E_F observed at most GaAs interfaces, especially those involving metals, is associated with a large concentration of acceptor and donor states spatially located in the GaAs within a few angstroms of the interface with energies near the GaAs mid gap. With nonmetal/GaAs interfaces, such as the vacuum/thermally cleaned surface, for example, the E_F for n-type GaAs is often ~ 0.25 eV greater than for p-type; this suggests that the acceptor interface states lie above the donor interface states in energy. For the present discussion we assume the existence of interface states without specifying the origin, nature, and precise energy distribution of these states.

The thin heavily doped Ge and Si overlayers on GaAs result in a large concentration of donor or acceptor states located in energy near the band edges of the overlayer and located spatially near the GaAs interface states. We suggest that the semiconductor overlayer provides a source of charge that can compensate (fill or empty) the GaAs interface states to thus move E_F toward the energy of the overlayer impurity level. Consider, for example, the Ge(n-type)/GaAs(n-type) interface where there is a large concentration of donors located ~ 0.2 eV from the GaAs conduction band owing to the heterojunction band lineup (Fig. 3). Electrons are thus available to fill unoccupied mid gap GaAs acceptor states; if all such states become occupied E_F will move to approximately the energy of the Ge conduction band minimum because the Ge, in the ideal case, is degenerately doped and remains undepleted. Similarly, for the Ge(p-type)/GaAs(n-type) interface there is a large concentration of acceptors available ~ 0.56 eV from the GaAs valence band to empty occupied mid gap GaAs donor states to thus place E_F near the Ge valence band maximum. As seen in Fig. 3, the heterojunction model we describe is in reasonable accord with the Ge/GaAs(n-type) data.

Referring to Fig. 7, this simple model is also in reasonable, although not complete, agreement with the Si/GaAs(n-type) data. The maximum range of E_F approaches, but is less than, the magnitude of the crystalline Si band gap. Among the plausible reasons for a departure from the model are: the effective band gap of the deposited Si, which is not fully crystalline, may be smaller than that of crystalline Si; the heavy dopant incorporation may have led to band gap narrowing; or there may have been insufficient dopant incorporation into the Si to fully compensate the GaAs interface states. It is possible, therefore, that refinement of the Si deposition conditions, particularly with respect to dopant incorporation, may lead to a further increase in the E_F range possible at Si/GaAs(n-type) interfaces).

The heterojunction model is in qualitative agreement with the essential features of the E_F data for Ge and Si overlayers on n-type GaAs. For the n-type Ge and Si overlayers on p-type GaAs, on the other hand, the E_F values are rather less than the predicted values near the Si and Ge conduction band minima (Fig. 12). Referring to the data of set (c) in Fig. 12, the E_F for the thermally cleaned surface of n-type GaAs (100) is ~ 0.8 eV. A substantial variation in E_F for Ga₂O₃ covered p-type and n-type GaAs surfaces has been measured [17], the maximum value of which for p-type GaAs is also ~ 0.8 eV. These two observations suggest the presence of a significant concentration of acceptor levels around 0.8 eV, which is also about the average value of E_F for the n-type Ge and Si overlayers. Furthermore, for n-type GaAs the band bending approaches a flat-band condition after deposition of the n-type Ge and Si overlayers while for p-type GaAs the band bending increases. Thus, more electrons must be supplied by the overlayer to both fully compensate interface acceptors and to support band bending on p-type compared to n-type GaAs. The lower p-type E_F values may therefore be due to

incomplete compensation of interface acceptors. Thus, refinement of the Ge and Si deposition conditions may lead to a larger concentration of electrically active donors than has been presently achieved and make possible a further increase of E_F values (hence larger ϕ_B Schottky barrier contacts to p-type GaAs).

Lastly, we note that in addition to GaAs, other III-V compound semiconductors (for example, InP) also tend to exhibit a restricted range of ϕ_B for metal contacts. If the mechanism that limits the range in ϕ_B for other III-V semiconductors is similar to that for GaAs, the heterojunction model suggests that heavily n-type and p-type Si and Ge interlayers included in appropriate contact structures will also increase the ϕ_B range for metal contacts to these semiconductors.

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DEFECT REACTIONS AT METAL-SEMICONDUCTOR AND SEMICONDUCTOR-SEMICONDUCTOR INTERFACES

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ABSTRACT

A recently proposed, new approach to the problem of native defect formation in compound semiconductors is presented. The approach is based on the concept of amphoteric native defects. It is shown that the defect formation energy as well as structure and properties of simple native defects depend on the location of the Fermi level with respect to an internal energy reference: the Fermi level stabilization energy. The known location of the stabilization energy determines the electronic part of the defect formation energy and allows for a quantitative description of a variety of phenomena including: the formation of defects at metal-semiconductor interfaces, doping induced superlattice intermixing and limitations of free carrier concentrations in semiconductors.

I. INTRODUCTION

It has long been recognized that identification of the physical processes which control the formation and the abundances of native (intrinsic) defects is essential for understanding of the structural and electronic properties of semiconductors [1]. This problem has become especially important in compound semiconductors in which, in principle, a large variety of different native defects can exist. In these materials the native defects were implicated to play a crucial role in a variety of phenomena in bulk crystals as well as at the metal-semiconductor (M-S) and semiconductor-semiconductor (S-S) interfaces. Thus, it has been proposed that a number of effects observed in semiconductors, such as saturation of electrical activity of impurities [2], formation of Schottky barriers [3] and doping-induced superlattice intermixing [4] are direct consequences of the presence of native defects. However, the well-known difficulties with the identification of native defects in compound semiconductors have left these proposals in a speculative stage.

It will be shown in this paper that recent developments in experimental defect studies, as well as higher accuracy of theoretical methods to calculate defect energies, provide the basis for identification of the defects which play a pivotal role in the determination of structural and electronic properties of semiconductors. It will be argued that many of the properties of semiconductors can be understood within a single unifying concept of amphoteric native defects (AND) [5]. The most important factor controlling defect incorporation and defect abundances is the location of the Fermi level measured with respect to the internal energy reference, the Fermi level stabilization energy [6]. Therefore, structural properties as well as electronic identity (donor or acceptor) of the defects depend on the type of doping, doping concentration and temperature. We will demonstrate how this novel approach to the problem of defects can be applied to quantitatively understand the formation of the Schottky barriers, superlattice intermixing and limitations of free carrier concentrations in semiconductors.

II. DEFECT INDUCED STABILIZATION OF FERMİ ENERGY

It has been demonstrated in numerous photoemission experiments that the deposition of a metal on cleaved (110) surfaces of weakly ionic III-V semiconductors results in stabilization of the Fermi energy [7]. The position of the stabilized Fermi level is only very weakly dependent on the metal, and agrees very well with the position of the Fermi level at the interface determined from the Schottky barrier heights measured for thick metal coverages [7,8]. These experimental results indicate that deposition of metal stabilizes (or pins) the Fermi level at the interface. There were several attempts to understand this phenomenon in terms of screening [9], formation of new phases [10,11], or formation of localized states at the M-S interface. [3,12-16] The nature of

possible localized states and the mechanisms of their formation have been hotly debated issues. Thus it has been proposed that the presence of a high density electron gas in the metal in intimate contact with a semiconductor induces localized states in the semiconductor band gap [13-16]. These so-called metal induced gap states (MIGS) stabilize the Fermi energy at the neutrality point E_B , which is determined by the semiconductor band structure [16].

Another very actively pursued concept uses the assumption that the stabilization or pinning of the Fermi energy is caused by native defects created in the semiconductor in the immediate vicinity of the surface [3]. The attractiveness of this proposal lies in the fact that it could, in principle, explain the pinning of the Fermi energy caused by oxidation, surface damage, or deposition of submonolayers of metals, i.e., the cases to which the MIGS concept is not applicable. The problem of the defect model, however, was that at the time when the model was proposed the properties of native defects in compound semiconductors were very poorly understood. Therefore one could only speculate on the identity of the native defects responsible for the Fermi level pinning [3]. Lack of a solid proof of the existence of native defects with properties required to explain the Fermi level behavior was considered to be a strong argument against the defect model [17].

In the defect model of Schottky barriers one assumes that electrically active native deep donor and/or acceptor-like defects stabilize the Fermi energy. If these defects can be associated with intrinsic properties of the semiconductors rather than with the metal-semiconductor interface one can expect that they should be observable in other experiments in which native defects are intentionally introduced into the semiconductor.

The experimental situation in which electronic properties of a semiconductor are determined by native defects is realized in semiconductors heavily irradiated with high energy particles. In such a case the primary damage takes the form of simple native defects: vacancies and interstitials. Since such defects can be electrically active they can also affect the position of the Fermi energy. It has been demonstrated in recent experiments that the introduction of a high concentration of native defects leads to stabilization of the Fermi energy [18-20]. Figs. 1(a) and 2(a) show the dependence of the Fermi energy on the electron irradiation dose in GaAs [18] and InP [20]. It is seen that independently of the type of conductivity of the original material the native defects produced by high energy electrons lead to the same stable position of the Fermi energy at $E_{FS} \approx E_v + 0.7$ eV and $E_{FS} \approx E_v + 1.0$ eV for GaAs and InP, respectively. There is a striking similarity between the Fermi level stabilization induced by irradiation and by the deposition of a metal on GaAs [21] (Fig. 1b) and InP [22] (Fig. 2b). The stabilization energy caused by the metal deposition is in excellent agreement with the ultimate position of the Fermi energy in heavily irradiated samples.

For both GaAs and InP, E_{FS} is located in the band gap. It means that the native defects compensate intentionally introduced donor or acceptor impurities leading to high resistivity materials. This is not generally true since as is shown in Fig. 3, in InAs [23], irradiation produces low resistivity n-type material. From measurements of electron concentration in neutron irradiated InAs one finds that E_{FS} is located in the conduction band at $E_v + 0.45$ eV. The condition $E_F = E_{FS}$ corresponds to the electron concentration of $n \approx 3 \times 10^{18} \text{ cm}^{-3}$. The location of E_{FS} in neutron irradiated InAs agrees quite well with the Fermi level position determined from the Schottky barrier height measured on p-type

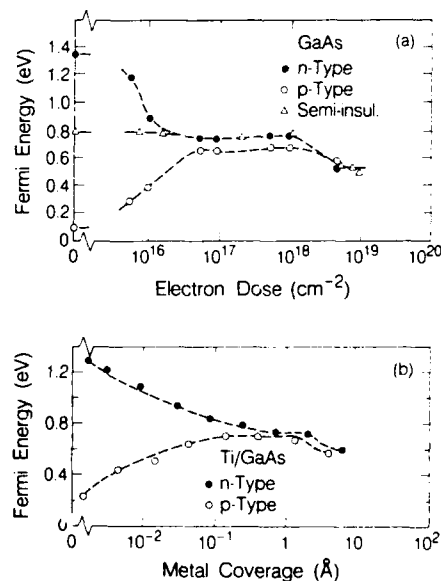


Fig. 1. The Fermi level dependence on electron irradiation dose in bulk GaAs (a) (Ref. [18]) and on metal thickness at metal-GaAs interface (b) (Ref. [21]).

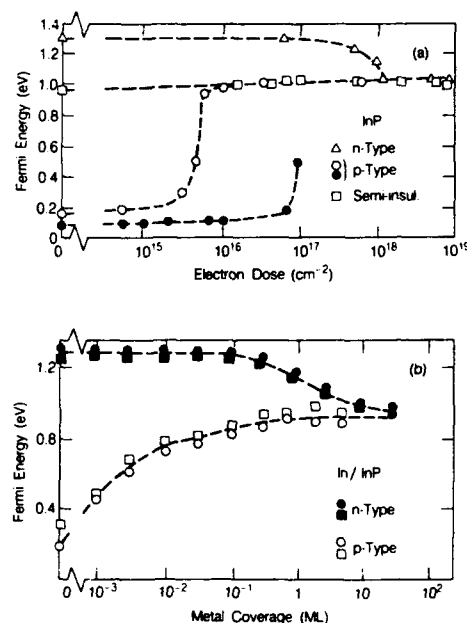


Fig. 2. The same as Fig. 1 but for InP. (Refs. [20] and [22]).

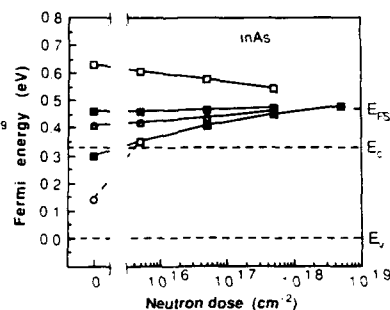


Fig. 3. Fermi level position in neutron irradiated InAs (after Ref. [43]). E_{FS} represents the Fermi level position determined from the Schottky barrier height in p-type InAs.

InAs [24]. The fact that E_{FS} is located in the conduction band indicates that the electronic states of the native defects are associated with a higher lying conduction band rather than with the low density of states conduction band minimum at Γ point. The donor-like nature of the native defects introduced in p-type or in low electron concentration ($n < 3 \times 10^{18} \text{ cm}^{-3}$) n-type InAs has been confirmed by ion implantation experiments which have shown that the implantation of acceptors (Mg) leads to n-type conductivity in this material [25].

The effects of irradiation have been much less extensively studied in other III-V semiconductors. On the basis of existing data compiled in Fig. 4 one finds, however, that in all the semiconductors for which experimental results are available there is a good agreement between the value of E_{FS} observed in heavily irradiated semiconductors and the Fermi energy position determined from the Schottky barrier heights at M-S interfaces [6,26]. One can conclude from the above experimental data that the same class of native defects is responsible for the defect induced Fermi level stabilization at metal semiconductor interfaces and in irradiated semiconductors.

The position of the neutrality point energy E_B [16] which has been postulated as the Fermi level pinning energy in the MIGS model of M-S interfaces is also shown in Fig. 4. Reasonably good agreement between the experimental values of E_{FS} and E_B is found. This is not surprising since it can be shown that E_B corresponds to an average energy of neutral vacancies [27,28]. Therefore, this energy is intimately related to the properties of native defects in semiconductors.

III. AMPHOTERIC NATIVE DEFECTS

In general, a quantitative description of defect abundances in semiconductors requires a full knowledge of the energetics of native defects. Recently a theoretical calculation of total energies of simple native defects in GaAs has been reported [29,30]. Based on this calculation it

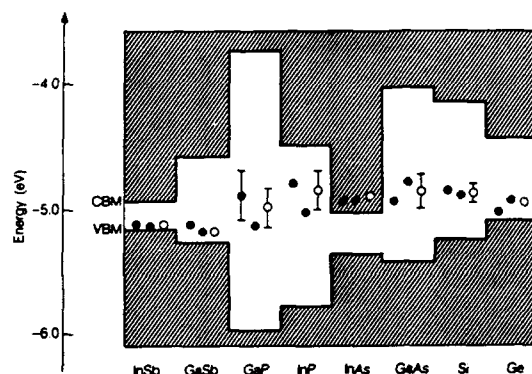


Fig. 4. Position of the Fermi level stabilization energy (Ref. [26]) deduced from the Fermi energy position in heavily irradiated semiconductors (●) and from the Schottky barrier heights of metal-semiconductor interfaces (○). The positions of the neutrality point energy E_B is also given (+).

has been shown that the abundances of simple nonstoichiometric defects are controlled by the following defect reactions [26]



and



The transformation from acceptor-like defects on the left hand side of 1(a) and 1(b) to the donor-like defects on the right hand side is accomplished by a single jump of an arsenic or gallium atom between the nearest neighbor sites. Since the donors and acceptors can support multiple charges their formation energy strongly depends on the location of the Fermi energy [29,31]. This is illustrated in Fig. 5 where total energies of the defects as functions of the Fermi level are shown. It is seen that in p-type GaAs donors $\text{As}_{\text{Ga}} + \text{V}_{\text{As}}$ and V_{As} have lower formation energies and are stable defects. On the other hand, in n-type material acceptor-like defects V_{Ga} and $\text{Ga}_{\text{As}} + \text{V}_{\text{Ga}}$ are stable. Therefore, when simple native defects are intentionally introduced into n- or p-type GaAs, acceptor or donor-like defects are formed. These defects compensate the electrical activity of the impurities and the Fermi energy shifts towards the mid-gap until it reaches the energy at which formation energies for donor- and acceptor-like defects are equal. At this point, further introduction of defects will not affect the Fermi level position. One finds from Fig. 5 that the stable Fermi level is located at $E_v + 0.6$ eV and $E_v + 0.8$ eV for the reactions (1a) and (1b), respectively. The theoretical values of E_{FS} are in good agreement with the experimental Fermi level stabilization energies determined from the Fermi level position in heavily irradiated GaAs and also determined from the Fermi level pinning at the metal-GaAs interface.

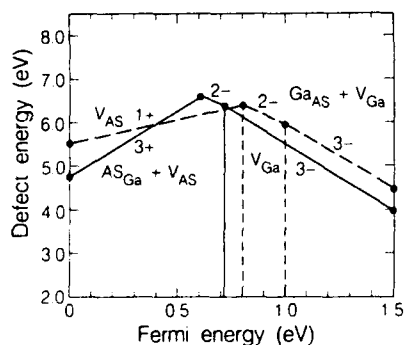


Fig. 5. Defect formation energies for V_{Ga} , V_{As} and related $\text{As}_{\text{Ga}} + \text{V}_{\text{As}}$, $\text{Ga}_{\text{As}} + \text{V}_{\text{Ga}}$ defects. The numbers at the graphs represent net charge transfer from the Fermi sea to the defects. The stabilization energy corresponds to zero net charge transfer.

In our discussion of defect reactions in GaAs we have neglected arsenic and gallium interstitials. This is a good approximation for the present considerations since interstitials are fast diffusing species and do not exist as isolated defects at room or higher temperatures. However, the interstitials have to be included at low temperatures when their diffusion is suppressed [26]. It has to be emphasized that incorporation of the interstitials does not significantly affect the value of E_F obtained for the reactions (1a) and (1b) [6].

IV. DEFECT FORMATION AT METAL-SEMICONDUCTOR INTERFACE; SUBMONO-LAYER COVERAGE

In order to consider the formation of defects during metal deposition on a semiconductor surface one has to identify a source of energy which is required for the defect generation. A perfectly cleaved (110) surface of a group III-V semiconductor undergoes a relaxation which removes the dangling-bond-like localized states from the energy gap. In such a system the Fermi energy at the surface is determined by bulk doping. There are several sources of additional energy released during metal deposition on a relaxed (110) surface:

- a) Energy of condensing metal atoms.
- b) Energy of exothermal chemical reactions between the deposited metal and host semiconductor atoms.
- c) Energy released during formation of metal clusters [32].
- d) Energy of the surface back-relaxation (un-relaxation) [33,34].

The energy of condensing metal atoms is small and cannot lead to the formation of defects by itself, however, it can initiate the other processes which can provide much more energy. In general, all the other three processes (b - d) can contribute to the formation of defects. However, here in our model calculations we will limit ourselves to the case when the energy for the defect formation is provided by surface back-relaxation. It has been shown in recent calculations that a substantial energy of about $E_0 = 0.35$ eV/surface atom is released in the process of back-relaxation of cleaved (110) GaAs surface [33,34].

To model the process of defect formation we assume that the number of back-relaxing surface atoms is given by the Poisson distribution,

$$p(N) = e^{-\langle N \rangle} \left(\langle N \rangle^N / N! \right) \quad (2)$$

where $\langle N \rangle$ is the mean value of the distribution. The probability of creating a defect with formation energy $E_{def}(E_F)$ is given by

$$G(E_F) = P[N \geq N_0] = \int_{N_0}^{\infty} p(N) dN \quad (3)$$

where $N_0(E_F) = E_{def}(E_F)/E_0$. The change of the defect concentration is related to the change in the concentration of metal atoms via the equation

$$dN_{def} = G(E_F) dN_{at} \quad (4)$$

Using standard electrostatic considerations one obtains

$$dN_{at} = \left(\epsilon N_i / 4\pi |Q| \left| E_{Fb} - E_F \right| \right)^{1/2} dE_F / G(E_F) \quad (5)$$

where Q is the charge transferred from the defects to the Fermi gas.

Equation 5 has been solved for the defect reaction (1a) corresponding to the case of the As rich interface [35]. The results are presented in Fig. 6. A most important feature of the Fermi level behavior is a slow pinning extending over more than two orders of magnitude of the metal

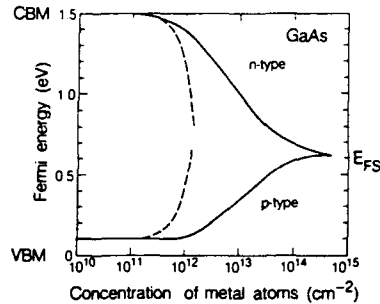


Fig. 6. Room temperature Fermi level pinning in n- and p-type GaAs obtained from the model calculations for $\langle N \rangle = 10$. The broken curves represent the pinning for defects with Fermi level independent defect formation energy.

coverage. This slow pinning is a direct consequence of the strongly Fermi level dependent defect formation energy. Such experimental behavior of the Fermi level is always observed for metal deposited at room temperature. Thus, as is seen in Fig. 1(b), in the case of Ti deposited on GaAs the full pinning of the Fermi energy extends over almost three orders of magnitude of metal coverage. This result can be contrasted with the Fermi level pinning predicted for the case of the defects with constant formation energy. As is seen in Fig. 6 for $G(E_F) = \text{const}$, a very fast pinning is found. Such dependence of the Fermi level pinning on the metal layer thickness is clearly inconsistent with the experimental data.

V. DOPING INDUCED SUPERLATTICE INTERMIXING

All the considerations of the preceding sections have been limited to the cases where the defects are intentionally introduced at low (room) temperature. Such defects form supersaturated systems and are not in equilibrium with the crystal lattice. It is well known that native defects play a crucial role in many phenomena observed at elevated temperatures during crystal preparation and/or processing. A phenomenon which has lately attracted considerable attention is so-called doping-induced superlattice intermixing [4]. It has been found that annealing leads to a very rapid destruction of GaAs/AlAs superlattices doped with donor impurities [4]. The effectiveness of the intermixing strongly depends on the dopant level [36]. Also, it has been found that co-doping with acceptors suppresses the intermixing [37]. All these facts were interpreted as an indication that the concentration of the defects facilitating the interdiffusion of Ga and Al atoms depends on the Fermi energy [4,38,39]. A more complex situation has been found in the case of acceptor impurities where it has been demonstrated that doping with Be to very high levels of $4 \times 10^{19} \text{ cm}^{-3}$ does not lead to any significant intermixing [37]. On the other hand, very fast intermixing is promoted by diffusion of Zn into a GaAs/AlGaAs superlattice [40]. Here we will show how the process of donor induced intermixing of a GaAs/AlAs superlattice can be understood in terms of the properties of amphoteric native defects.

The diffusion coefficient for intermixing at the GaAs/Al_xGa_{1-x}As heterointerface is given by,

$$D(x, T) = D_0(T) \exp(A(T) \cdot x) \quad (6)$$

where

$$A(T) = (E_{\text{Ga}} - E_{\text{Al}}) / kT \quad (7)$$

$$D_0(T) = C \exp(-E_{\text{Ga}} / kT) \quad (8)$$

E_{Ga} and E_{Al} is the formation energy of Ga and Al vacancies, respectively. One finds from these equations that the diffusion coefficient is proportional to the vacancy concentration

$$D_0(T) \sim [V_{\text{Ga}}] \quad (9)$$

As has been discussed in previous sections, the formation energy of V_{Ga} depends on the Fermi level. For n-type doping ($E_F > E_{\text{FS}}$) one has

$$[V_{Ga}] = C' \exp \left(\frac{-E_{Ga}^0 - 3(E_F - E_{FS})}{kT} \right) \quad (10)$$

or

$$[V_{Ga}] = C'' \exp \left(\frac{3E_F}{kT} \right) \quad (11)$$

where E_{Ga}^0 is the formation energy of V_{Ga} for $E_F = E_{FS}$. The Fermi level is determined by free carrier concentration

$$n = N_c F_{1/2} \left(\frac{E_F - E_c}{kT} \right) \quad (12)$$

where $F_{1/2}$ is the Fermi-Dirac integral. Since V_{Ga} are triply ionized acceptors they compensate intentionally introduced donors and

$$n = N_D^+ - 3[V_{Ga}] \quad (13)$$

where N_D^+ is the total concentration of shallow donors.
From eqs. (11), (12) and (13) one obtains

$$[V_{Ga}] = C'' \left(\frac{N_D^+ - 3[V_{Ga}]}{N_c} \right)^3 \quad (14)$$

Typical experiments on superlattice intermixing are performed in the temperature range $\sim 700^\circ\text{C}$ to 900°C . Therefore, to solve eq.(14) one has to know the temperature dependence of the position of conduction band-edge measured with respect to E_{FS} . There are two contributions to the temperature dependence of the band edges: the lattice dilation and electron-phonon interaction. The dilation contribution to the temperature shift of $(E_c - E_{FS})$ is

$$\frac{\partial (E_c - E_{FS})}{\partial T} = 3 \frac{\Delta a}{a} \cdot a_c \quad (15)$$

where $\Delta a/a$ is the relative temperature dependent change of the lattice parameter, and a_c is the conduction band deformation potential. Using the value $\Delta a/a = 6 \times 10^{-6} \text{ K}^{-1}$ and recently determined value of $a_c = 9.3 \text{ eV}$ for the deformation potential [41], one obtains $\partial(E_c - E_{FS})/\partial T = 1.7 \times 10^{-4} \text{ eV/K}$. Here we neglect the electron-phonon interaction contribution to the band-edge shift since it depends on the effective mass and is small for the conduction band. Eq. (14) is solved numerically. The results of the calculations are shown in Fig.7. It is seen that the diffusion coefficient increases very rapidly at low donor concentrations $D \sim N_D^3$. A much slower dependence $D \sim N_D$ is found for the doping levels exceeding $\sim 3 \times 10^{18} \text{ cm}^{-3}$. These results are in very good agreement with experimentally observed trends on the Si-doped GaAs/AlGaAs superlattice intermixing. A rapid decrease of the diffusion coefficient for $N_D < 3 \times 10^{18} \text{ cm}^{-3}$ was interpreted as a threshold for Si-induced intermixing.[42] The threshold concentration corresponds to $E_F - E_{FS} \approx 0.7 \text{ eV}$ at 1000 K. This location of the Fermi energy leads to the reduction of the V_{Ga} formation energy by 2.1 eV.

According to our present considerations the efficiency of intermixing is determined by the separation of the Fermi energy from E_{FS} . This indicates that the effectiveness of the doping induced superlattice intermixing will be reduced in systems with the conduction band edge lying closer to E_{FS} . An example of such a system is the lattice matched $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.47}\text{Al}_{0.52}\text{As}$ superlattice. In InAs E_{FS} is located in the conduction band, therefore the primary effect of

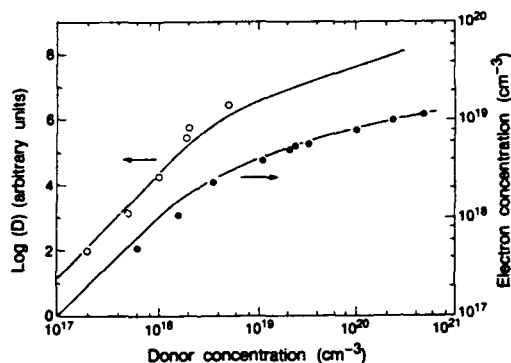


Fig. 7. Diffusion coefficient, D , in n -type GaAs/AlAs and electron concentration in GaAs as functions of donor concentrations. Experimental data from Si-doped GaAs/AlAs superlattice intermixing (o) [36] and from Hall measurements of electron concentration in Se doped GaAs (•) [46] is also shown.

addition of $\sim 50\%$ of In to GaAs and AlAs is to reduce $E_c - E_{FS}$. In GaAs at ~ 1000 K, $E_c - E_{FS} = 0.7$ eV, whereas it is only ~ 0.4 eV in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$. In InGaAs the value of $E_F - E_{FS} = 0.7$ eV is achieved for electron concentrations of about $2 \times 10^{19} \text{ cm}^{-3}$, which is much higher than the threshold concentration of $3 \times 10^{18} \text{ cm}^{-3}$ found in GaAs. Recently, Si-doping-induced intermixing of In GaAs/InAlAs superlattice has been studied [43]. It has been observed that the donor doping to the level $7 \times 10^{18} \text{ cm}^{-3}$ does not produce any intermixing. Much higher doping of $1.3 \times 10^{19} \text{ cm}^{-3}$ is required to substantially intermix the superlattice. This value of the critical doping agrees quite well with our theoretical estimate, providing additional support for the proposed mechanism of superlattice intermixing.

In its simplest form the present mechanism of the doping induced intermixing does not depend on the nature of donors. Intermixing efficiency depends only on the location of the Fermi level which in turn is determined by the carrier concentration. The most recent study of a Te-induced intermixing of GaAs/AlAs superlattice has shown that the interdiffusion is a linear function of Te concentration for the doping level in the range $2 \times 10^{17} \text{ cm}^{-3}$ to $5 \times 10^{18} \text{ cm}^{-3}$. This is a much slower dependence than that reported for the case of Si doping. Assuming that all Te atoms are electrically active this result indicates that a different, more efficient interdiffusion process is operational in this case. However, if for some reason the electron concentration in the MOCVD grown superlattice is a sublinear function of the Te doping level, then it could explain the slower dependence of the interdiffusion on the Te atom concentration. Only direct measurements of the electron concentration in Te doped samples could resolve this issue.

It should be noted that the present model does not predict any intermixing of the GaAs/AlAs superlattice by p-type doping. For $E_F < E_{FS}$ the stable defects are V_{As} and $As_{Ga} + V_{As}$. These defects do not lead to interdiffusion of Ga and Al. This conclusion is in agreement with experiments which indicate that there is no universal intermixing of GaAs/AlAs interfaces by p-type doping. A very efficient intermixing caused by Zn in-diffusion finds an explanation consistent with the substitutional-interstitial mechanism of acceptor diffusion in GaAs [40,45]. The explanation of superlattice intermixing in terms of the Fermi level dependent defect formation has been proposed before [38,39]. However, without the concept of the Fermi level stabilization energy the authors of this proposal were not able to account for the difference between n - and p -type doping or between superlattices based on different materials.

VI. LIMITATIONS OF MAXIMUM FREE CARRIER CONCENTRATIONS IN SEMICONDUCTORS

Many of the applications of compound semiconductors require preparation of low resistivity and high free carrier concentration materials. It is well recognized that in some cases one cannot achieve a high carrier concentration by either doping, implantation, or diffusion. Thus, in bulk grown GaAs the highest electron concentration which can be achieved by the doping does not exceed $\sim 10^{19} \text{ cm}^{-3}$ [46]. The highest electron concentration obtained by donor implantation is in the range 3 to $5 \times 10^{18} \text{ cm}^{-3}$ [47,48].

The situation is much different for p-type dopants in GaAs. In this case a very high concentration of holes, exceeding 10^{20} cm^{-3} , can be obtained [49]. Also, there is a one to one correspondence between the acceptor concentration and the concentration of holes, indicating that all acceptor atoms are electrically active and that the concentration of compensating donors is low. A semiconductor which shows a behavior similar to GaAs is GaSb. Again, in this case one finds that the maximum reported hole concentration is much higher [50] than the maximum electron concentration [51].

In striking contrast to GaAs and GaSb, one can obtain n-type InP with high electron concentrations approaching 10^{20} cm^{-3} [52]. Whereas doping of this material with acceptors is very inefficient and the highest reported hole concentrations lie in the range 3 to $5 \times 10^{18} \text{ cm}^{-3}$ [53]. The low carrier saturation concentrations in n-type GaAs and GaSb and in p-type InP are not dependent on the chemical identity of the donors or acceptors and are not associated with the solubility limits of the impurities which can be one to two orders of magnitude higher than the maximum carrier concentrations.

All these findings indicate that the electrical activity of shallow impurities is compensated by native defects, acceptors in GaAs and GaSb, and donors in InP. In order to quantitatively describe the compensation process we consider n-type GaAs. In this case the Fermi energy is above E_{FS} and the formation energy of V_{Ga} is reduced. The concentration of free electrons is given by eq. (13) with $[V_{Ga}]$ determined by the solution of eq. (14). The calculated free carrier concentration is shown in Fig. 7. The value of the parameter $C'' = 3 \times 10^{18} \text{ cm}^{-3}$ has been used in the calculations. It is seen that for low doping levels, $N_d < 3 \times 10^{18} \text{ cm}^{-3}$, the concentration of the compensating V_{Ga} acceptors is low and $n = N_D^+$. For $N_d > 3 \times 10^{18} \text{ cm}^{-3}$, a much weaker dependence of the electron concentration on N_D is found, $n \propto (N_D)^{1/3}$. This characteristic $1/3$ power dependence is related to the fact that the compensating V_{Ga} are triply charged acceptors. As is seen in Fig. 7 the results of the calculations are in a good agreement with experimental data on Se doped GaAs [46]. It should be noted that very similar $n(N_D)$ dependencies were observed for other donors in GaAs [54]. We find from Fig. 7 that a critical concentration of electrons at which the effects of the compensation are becoming significant is $\sim 3 \times 10^{18} \text{ cm}^{-3}$. This corresponds to the value of $|E_F - E_{FS}| = 0.7 \text{ eV}$ for $T = 1000 \text{ K}$. In p-type GaAs the same condition $|E_{FS} - E_F| = 0.7 \text{ eV}$ is satisfied for the hole concentration of $p \approx 9 \times 10^{20} \text{ cm}^{-3}$. This indicates that in p-type GaAs the limit for the free hole concentration set by the native defect compensation is very high. This is in agreement with the experiments which consistently show a high activation efficiency for acceptors in GaAs.

We infer from the above considerations that the donor-induced GaAs/AlAs superlattice intermixing is intimately related to the problem of saturation of free electron concentration in GaAs. Also, we find that the most important parameter controlling generation of compensating native defects is the separation of the Fermi energy from E_{FS} . From known locations of E_{FS} we can predict the trends in doping activation efficiency for different III-V semiconductors. In InP $E_{FS} \approx E_V + 1.0 \text{ eV}$ is located close to the conduction band. Therefore one expects that it should be easier to activate donors in this material than in GaAs. On the other hand, even moderate hole concentrations will result in a large value of the energy difference ($E_{FS} - E_F$) leading to the formation of native defects and compensation of intentionally introduced acceptors. This is exactly what is observed experimentally where it has been found that it is much easier to obtain heavily doped n-type InP while the maximum hole concentration is limited to \sim mid 10^{18} cm^{-3} [53].

By virtue of the same qualitative argument one can expect that in GaSb, in which E_{FS} is located at $\sim E_V + 0.1 \text{ eV}$, i.e. very close to the valence band, doping with donors will be much less efficient than doping with acceptors. Systematic studies of donor doping in GaSb have shown that for $n > 10^{18} \text{ cm}^{-3}$ the electron concentration very weakly depends on the donor concentration ($n \propto N_D^{1/3}$) [51]. This is the same dependence as that found for n-type dopants in GaAs. Therefore, we conclude that the native acceptor defects compensating the electrical activity of donors in heavily doped n-type GaSb occur in a triply ionized charge state. The highest electron concentration reported in GaSb does not exceed $3 \times 10^{18} \text{ cm}^{-3}$ [51]. On the other hand, doping with acceptors can provide material with the hole concentrations in excess of 10^{20} cm^{-3} [50].

Although the case of GaSb is, in many respects, similar to GaAs there is one important aspect which makes GaSb a unique material. It is well known that undoped, as-grown GaSb

shows p-type conductivity with the hole concentration of the order of 10^{17} cm^{-3} . It has been proposed, based on thermodynamical analysis of the defect formation, that $\text{GaSb} + \text{V}_{\text{Ga}}$ native acceptors are responsible for this high hole concentration [55]. It is interesting to note that this finding is in full agreement with the conclusions one can draw from the AND model. In Sb-deficient GaSb the amphoteric defect reaction corresponding to the reaction (1b) is,



Since, in GaSb E_{FS} is closer to the valence band than in GaAs, therefore, in intrinsic material the condition $E_{\text{F}} \gg E_{\text{FS}}$ is always satisfied and the $\text{GaSb} + \text{V}_{\text{Ga}}$ acceptor is the stable defect.

VII. CONCLUSIONS

We have presented a new approach to the understanding of native defects in semiconductors. The approach is based on the concept of amphoteric native defects. It has been shown that the relative abundance, as well as structural and electronic properties of simple native defects, are controlled by the location of the Fermi level. The strongly Fermi level dependent electronic contribution to the total defect formation energy is proportional to the energy separation between the Fermi level and an internal energy reference: Fermi level stabilization energy. The location of the Fermi level stabilization energy with respect to the conduction and valence band edges is the single most important parameter controlling defect abundances at the metal-semiconductor and semiconductor-semiconductor interfaces, as well as in bulk semiconductor crystals. We have employed the amphoteric native defect model to show that apparently unrelated phenomena such as Schottky barrier formation, doping induced superlattice intermixing, and limitations of free carrier concentrations in semiconductors can have a simple common explanation.

The concept of amphoteric native defects finds application going beyond the effects discussed in this paper. It has been demonstrated recently that the very extensively studied and practically very important effect of doping-induced suppression of dislocation formation finds an explanation within the same basic concept [56,57]. Further, experimental and theoretical studies of defects in different semiconductors will be necessary to test the universality and applicability of this concept to other phenomena in semiconductors.

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PART IV

Ohmic Contacts/
Insulator-Semiconductor
Heterostructures

DEVELOPMENT OF THERMALLY STABLE INDIUM-BASED OHMIC CONTACTS TO n-TYPE GaAs

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ABSTRACT

Development of low resistance ohmic contacts to n-type GaAs which withstand high temperature cycles without degrading their electrical properties is crucial for fabrication of high performance GaAs integrated circuits. Prior to our work, indium-based ohmic contact materials were not attractive for actual devices, because the contacts provided resistances higher than those of the widely used AuNiGe contacts, were thermally unstable after contact formation, and had rough surface morphology. Recently, based on analysis of the interfacial microstructure of these contacts, several thermally stable, low resistance In-based ohmic contacts to n-type GaAs have been developed in our laboratories using a standard evaporation and lift-off technique and annealing by a rapid thermal annealing method. The present paper points out the reasons for the poor electrical properties and thermal stability of the "traditional" In-based ohmic contacts, and reviews the recent progress.

INTRODUCTION

GaAs is a very attractive material for use in optoelectronic devices, and also for digital integrated circuits to operate at speeds beyond the capability of Si devices. In addition, compared with Si devices, the GaAs devices operate at lower power, are more radiation tolerant, and the device fabrication process is simpler. Currently making the transition from laboratory to manufacturing is the MESFET (metal-semiconductor field-effect transistor). In order for GaAs to be economically competitive with Si, the fabrication process for GaAs devices should be compatible with that of Si devices as much as possible. With increasing circuit complexity, device reliability (or stability) becomes an important issue in addition to device performance. A few years ago, development of reliable metallization systems for GaAs devices was far behind that of Si devices. The stability of Schottky contacts had been significantly improved by replacing so-called "soft" (low melting point) metals by refractory metals [1-3]. However, the development of thermally stable ohmic contact materials had not seen similar progress.

To reduce contact resistance at the metal/semiconductor interface, there are two approaches: one is heavily doping GaAs with donors, and the other is reducing the barrier height at the metal/GaAs interface [4]. Most of the contacts used commercially in GaAs MESFETs have been developed using the former approach, and the AuNiGe metal system has been universally used for over 20 years [5]. There are several reasons for the wide use of this metallurgy. It provides sufficiently low contact resistance, and is compatible with conventional deposition and lift-off patterning techniques developed for Si circuitry. Excellent device performance has been demonstrated using these contacts [6]. In spite of these good properties, rough surfaces, deteriorated contact edge profiles, and thermal instability have been observed after ohmic contact formation [7,8]. These properties are marginally acceptable for the current technology, but definitely not for the future technology, which must be scaled to smaller dimensions.

In contrast to this approach, indium-based ohmic contacts generally do not require incorporation of a dopant from the deposited metals. The typical contact materials, prepared by an evaporation and lift-off technique which is compatible with the current MESFET process, are In [9-16], Ag-In [17,18], Ag-In-Ge [17,19-30], Au-In [10,31-35], Au-In-Ge [28,36-41], Al-In [42], Sn-In [43], Pt-In [44], and Pd-In [45]. The resistances of these contacts are higher than those obtained routinely in AuNiGe ohmic contacts and surface morphology and thermal stability after contact formation are poor. Therefore, none of these In-based ohmic contacts are used in the manufacturing MESFET devices.

Recently, significant improvement of the In-based ohmic contacts have been made in our laboratories [46-50]. MESFET devices made using one of these recent ohmic contacts showed excellent device performance [51], and thermal stability and surface morphology were superior to devices with AuNiGe ohmic contacts.

The purpose of the present paper is to describe the reasons for the poor electrical properties and thermal instability of the "traditional" In-based ohmic contacts, and to review progress of the "recent" ohmic contacts. First, the microstructure at the In/GaAs interfaces is correlated with the electrical properties of the contacts. Then, the fabrication processes which influenced the interfacial microstructure are described. Finally, the "recent" ohmic contacts developed by selecting the process parameters which provided low resistance and excellent thermal stability are described along with the results of the MESFET devices made with these contacts.

EXPERIMENTAL PROCEDURES

Formation of ohmic contact materials

The contact resistances (R_c) were measured by the transmission line method (TLM) [52]. The channels were doped by SiF^+ at 100 KeV with a 3.5×10^{13} dose and activated by annealing at 800°C for 10 min with a Si_3N_4 cap layer. After decapping this layer using a CF_4/O_2 plasma and forming the photoresist lift-off stencil, the wafers were chemically cleaned by soaking in a buffered HCl solution (50% HCL) for 5 min, prior to metal deposition. The vacuum system was pumped down to $\sim 8 \times 10^{-6}$ Pa before metal deposition. The substrate holder was cooled by circulating liquid nitrogen for In/W deposition [53]. Other contact materials were prepared at room temperature, where Ni, Mo, Ge, and W were evaporated by electron beam, and In was deposited by RF induction heating. (A slash (/) indicates the sequential deposition.) Samples were then covered by 50 nm thick PECVD Si_3N_4 layers deposited at around 300°C . Ohmic contacts were formed by heating in a furnace (FA) or by a short heat pulse generated by CW lamps (here called RTA) in an Ar/H_2 atmosphere.

The thermal stability experiment was carried out by annealing the samples isothermally at 400°C in a furnace with an Ar/H_2 atmosphere. Cross-sectional TEM was mainly used to observe interfacial microstructure. Specimens were prepared by mechanical polishing and ion milling at liquid nitrogen temperature. A JEOL-200CX TEM was operated at 200KeV to obtain lattice images and a Philips 400T TEM/STEM, operated at 120KeV, was used to perform microanalysis at the interface by x-ray energy dispersive spectroscopy.

MESFET fabrication

The fabrication process for self-aligned refractory MESFETs has been described previously [6]. The present process steps are similar. The n^+ channels were formed by implanting SiF^+ ions at 85 KeV with a dose of $2.5 \times 10^{13}/\text{cm}^2$, annealed at 850°C for 20 min with a SiO_2N_x (index reflection coefficient $n=1.75$) cap layer, and decapped using a CF_4/O_2 plasma. A blanket film of $\text{WSi}_{0.1}$ gate metal with thickness of 200 nm was then deposited by dc magnetron sputtering. Reactive ion etching in a CF_4/O_2 mixture was employed to define the FET gate with lengths down to about 1.0 μm . The SiF^+ ions were again implanted at 100 KeV with a dose of $6 \times 10^{13}/\text{cm}^2$. The $\text{WSi}_{0.1}$ gate serves as a mask for the n^+ implant in the FET source and drain regions. The source/drain implant was activated by a Si_3N_4 cap annealing technique at 800°C for 10 min. Next a photoresist lift-off stencil for ohmic contacts was applied. For NiInW ohmic contact formation, the deposition sequence and annealing temperature are the same as described in the previous section.

For the thermal stability experiment, the devices were coated by a Si_3N_4 layer except for via-holes for electrical measurements and annealed at temperatures between 400 and 500°C in a furnace with an Ar/H_2 atmosphere [51].

EXPERIMENTAL RESULTS AND DISCUSSION

In/GaAs interaction

In order to improve the electrical properties and thermal stability of In-based ohmic contacts to GaAs, the In and GaAs interaction at high temperatures must be understood. As a first step, ternary InGaAs phase diagrams were calculated [53,54] using an equation given by Antypas [55], where the activity coefficient in the liquid phase was calculated using Darken's quadratic equation [56] and the solid solution in equilibrium with the ternary liquid was assumed to be regular. An example of the phase diagrams calculated at 700°C is shown in Fig. 1. The dashed lines indicate tie-lines which connect two phases at thermal equilibrium at 700°C. At this temperature the solid $\text{In}_x\text{Ga}_{1-x}\text{As}$ phase and the liquid $\text{In}(\text{Ga,As})$ phase (indicated by points "a" and "b", respectively) coexist when the "effective" average composition is at the point "c" which is within the two phase region.

The microstructures of In deposited on GaAs were observed by TEM by Ding et al [57] and Kim et al [53]. As an example, the cross-sectional microstructure of the In deposited onto a GaAs substrate at room temperature and annealed at high temperature is illustrated schematically in Fig. 2. When In was deposited on the GaAs substrate at room temperature, In usually formed islands and no reaction with the GaAs was observed. Upon annealing the In/GaAs at temperature above the melting point of In, In started to react with the GaAs and In-rich $\text{In}(\text{Ga,As})$ phases and $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases were observed. The In composition (x) in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases was about 0.2-0.3 and uniform for the contacts annealed at temperatures above 700°C [58]. Note that the formation of graded $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases was not observed by TEM and XRD. The observed microstructure agreed very well with that predicted by the phase diagram of Fig. 1. These two phases are correlated with the electrical properties and thermal stability of In-based ohmic contacts below.

Electrical properties of In-based ohmic contacts

The $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases have the energy gaps smaller than that of GaAs and also the barrier heights at the metal/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ interface were found to decrease with increasing In concentra-

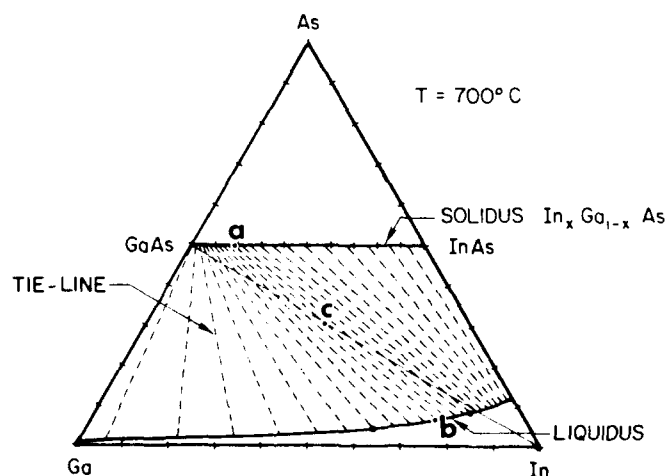


Fig. 1 Ternary In-Ga-As phase diagram calculated at 700°C [53,54]

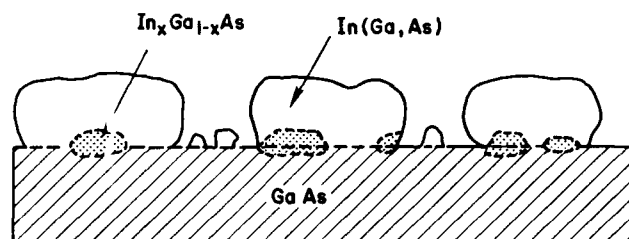


Fig. 2. Cross-sectional structure of In deposited on GaAs substrate and annealed at high temperature.

tion in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases [59]. Thus, it was concluded that formation of the ternary phases at the metal/GaAs interfaces provided low contact resistances.

The first demonstration that the low contact resistance of the In-based ohmic contacts was due to reduction of the barrier height was made by Woodall et al [60]. They grew graded n^+ - $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer on the GaAs by molecular beam-epitaxy method, in which InAs contacted the metal. Since the conduction band of InAs is pinned below the Fermi-level, no barrier to conduction through the metal/InAs interface is expected. The band diagram of this "ideal" zero barrier contact is schematically shown in Fig. 3(a). However, as described above, formation of such graded $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer is unlikely in ohmic contacts prepared by depositing In on GaAs and annealing. As observed by TEM, the concentration of In in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer was uniform [53]. The proposed band diagram of these contacts is shown in Fig. 3(b), where the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases are assumed to grow epitaxially on the entire GaAs surface [48]. For this contact, the measured low contact resistance was proposed to be due to reduction of the barrier height by dividing the high barrier at the metal/GaAs into two small barriers at the metal/ $\text{In}_x\text{Ga}_{1-x}\text{As}$ and the $\text{In}_x\text{Ga}_{1-x}\text{As}$ /GaAs interfaces. Therefore, the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases between the metal and the GaAs are the key phases controlling the electrical properties of the contacts.

Contact resistances vs $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases

In order to confirm that the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases have a dominant effect on the contact resistances, R_c values of In-based contacts prepared in our laboratories are plotted in Fig. 4 as a function of the (areal) percentage of the GaAs interface covered by the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases. The percentages were obtained by squaring the linear percentages which were measured from TEM micrographs of various In-based ohmic contacts prepared by FA or RTA. The R_c values on the vertical axis are those in which the contribution of the contact metal sheet resistances (R_s) were subtracted from the measured R_c values using an equation given by Marlow and Das [61] except one indicated by a closed circle which was an experimental value of the NiInW contact with low metal sheet resistance. It is noted that the R_c values decrease with increasing percentage of the GaAs interface covered by the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases. This result supports the above conclusion that the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases have the primary effect on the electrical properties of these contacts. From this figure, it is noted that the elements added with In to the contacts did not have a strong effect on the electrical properties. Therefore, to prepare low resistance contacts the total area of the GaAs interface covered by the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases should be as large as possible. This total area was strongly influenced by the fabrication parameters as described below.

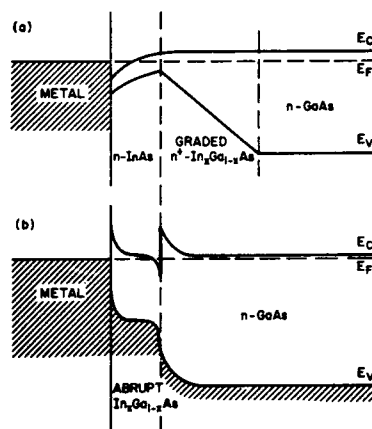


Fig. 3. Band diagrams of graded (a) and abrupt (b) $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers in contact with GaAs [48,60].

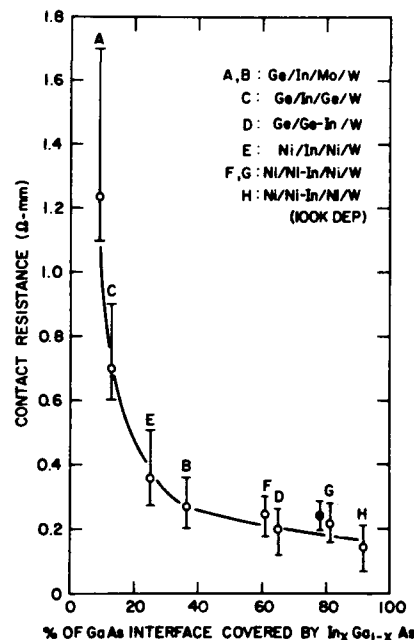


Fig. 4. Contact resistances of In-based ohmic contacts as a function of percentage of GaAs interface covered by $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases.

Fabrication parameters which affect formation of $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases

Fabrication process was found to influence the total area of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases in contact with the GaAs after contact formation. To increase the area, we should select process parameters which give (a) uniform distribution of In atoms in as-deposited samples, and (b) shallow In diffusion into GaAs substrates after contact annealing.

Substrate temperature

When In is deposited on the GaAs substrate at an ambient temperature, In forms islands as schematically shown in Fig. 2(a). With reduced substrate temperature, the mean interspacing between the islands decreases, their density increases, and a thin In layer continuously covers the substrate surface at very low substrate temperature. TEM observation of these contacts indicated that the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases in contact with GaAs were formed non-uniformly after annealing the contacts which were prepared at room temperature [57], and that the density of ternary phases increased for those deposited at 77K [53].

The R_c values measured by TLM are plotted by closed and open circles in Fig. 5 as a function of annealing temperatures for In-based contacts which were prepared at room [15,16] and liquid nitrogen temperature [53], respectively. (In order to compare the R_c values of the contacts prepared at liquid nitrogen temperature with those prepared at room temperature, the specific contact resistances were calculated from the R_c values measured by TLM.) It is seen that about an order of magnitude lower resistances are obtained by depositing In at cold substrate temperature. The

reduction of the R_c values by preparing the contacts at low temperatures was due to increase in the density of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases [53].

Deposition method

Formation of large, dispersive In islands was also reduced by reducing diffusion of In atoms on the GaAs substrates during deposition by evaporating simultaneously In and another element which had low surface diffusivity. In order to investigate the effect of coevaporation of In and other elements on the $\text{In}_x\text{Ga}_{1-x}\text{As}$ formation, two types of GeInW and NiInW ohmic contacts were prepared where In was deposited as a single layer or codeposited with Ge or Ni [48]. The total areas of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases contact with the GaAs were observed by TEM. It was found that about two times larger $\text{In}_x\text{Ga}_{1-x}\text{As}$ areas were in contact with the GaAs for the contacts which were

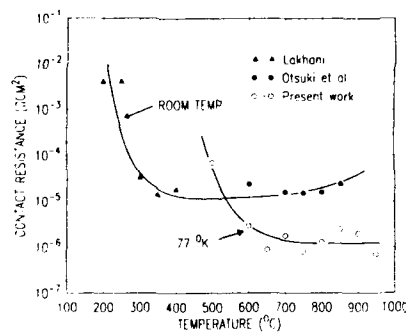


Fig.5. Contact resistance of In-based ohmic contacts prepared at room (closed symbols) and liquid nitrogen temperature (open circles) [53].

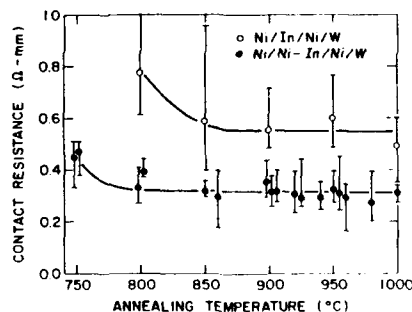


Fig.6. Contact resistances of NiInW contacts with single or coevaporated In layers [48].

codeposited with In and Ge or In and Ni than those with single In layers. The R_c values of the NiInW contacts with a single In layer (denoted as Ni/In/Ni/W) or coevaporated Ni-In layer (denoted as Ni/Ni-In/Ni/W) are shown in Fig. 6 by open and closed circles, respectively. It is seen that the R_c values of the contacts with the coevaporated Ni-In layers are smaller by a factor of about two compared with those with the single In layers.

There are other deposition methods which provide uniform In distribution over the GaAs surface: sputter-deposition from a single target, co-sputter-deposition of In and a low diffusivity element(s), deposition with ion-mixing etc. Also, formation of highly dense nucleation sites of In islands on the GaAs substrates, and deposition of In at high evaporation rates will provide uniform In distribution.

Indium thickness

The thickness of the In layer affected the density of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases in contact with the GaAs when the thickness was less than 5 nm [53]. However, the In thickness did not affect strongly this density in contacts with thicker In layers. As will be discussed later, the In thickness primarily effects the thermal stability of the contacts after contact formation.

Annealing method

When the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases contact the GaAs substrates at a shallow depth, the average composition (indicated by "c" in Fig. 1) within the reacted region moves toward the In corner, and the In concentration (x) in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases (indicated by "a" in Fig. 1) shifts to the InAs side. Therefore, to prepare the In-rich $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases at the metal and GaAs interface (which reduces the barrier height between the metal and GaAs interface), the diffusion depth of In should be shallow in the GaAs at a given In thickness. The annealing method, temperature, and time strongly influenced the diffusion depth of In into GaAs. The MoGeInW contacts were prepared by FA for 10 min or by RTA for ~ 1 sec, and the interfacial microstructures were analysed by Auger and TEM [47]. It was found that more In segregated at the metal/GaAs interfaces forming the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases for the contacts prepared by RTA compared with those prepared by FA. The contact resistances of these samples are shown in Fig. 7 by open (FA) and closed circles (RTA). The contacts prepared by RTA showed lower resistances by a factor of about two compared with those prepared by FA.

Deposition of a thin first layer

The In diffusion was also found to be controlled by the presence of a "diffusion barrier" layer between the In layer and the GaAs substrate during the annealing process. Formation of such a barrier layer reduced significantly the time during which In and GaAs interact at high temperatures, and thus prevented deep In diffusion into the GaAs. Deposition of a thin Ni layer before In deposition yielded lower resistance compared with contacts without a Ni first layer [48]. The first Ni layer formed a uniform Ni_2GaAs layer between the In layer and the GaAs substrate. This Ni_2GaAs layer was found to be stable even after annealing at 600°C , and transformed to NiGa and NiAs phases above 600°C [58]. Therefore, the In and GaAs reaction was suppressed until the samples reached $\sim 600^\circ\text{C}$, and the reaction occurred in a very short time as the samples were heated from 600 to e.g., 900°C . The R_c values of contacts without Ni first layers were higher than those with Ni first layers when annealed by the same method. This could be due to deep diffusion of In into GaAs.

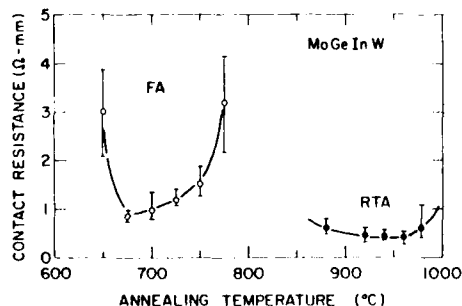


Fig. 7. Contact resistance of MoGeInW annealed by FA (open circles) or RTA (closed circles) [47].

Thermal stability of In-based ohmic contacts

As described previously the thermal instability of In-based ohmic contacts was caused by the presence of low melting point $\text{In}(\text{Ga,As})$ phases after contact formation. Therefore, to improve the stability the volume fraction of the $\text{In}(\text{Ga,As})$ phases should be minimized. How the thickness of the In layer and other elements added to In affected the thermal stability will be discussed below.

Indium thickness

When the In composition averaged over the region where In and GaAs react is high, the volume fraction of the In(Ga,As) phases in the contacts becomes large as predicted from the InGaAs phase diagram of Fig. 1. Therefore, the thickness of the deposited In layer strongly influences the thermal stability of the contacts after contact formation.

The In/W contacts with In thickness of 5 or 100 nm were prepared by depositing at 77 K and annealing at 900°C for a short time by RTA [53]. These contacts provided low resistances. Fractional changes in the R_c values of these contacts during subsequent isothermal annealing at 400°C are shown in Fig. 8. The R_c values of the contact with a 100 nm thick In layer increased upon annealing at 400°C, but those of contacts with a 5 nm thick In layer were relatively stable and increased slightly after annealing for 20 hrs. TEM observation of these contacts revealed that the volume fraction of the In(Ga,As) phases was significantly reduced by reducing the In thickness. Therefore, the improved stability of the In contact with reduced In thickness is attributed to the reduced volume fraction of the In(Ga,As) phases after contact formation.

Addition of other element(s)

Although reduction of the In layer thickness improved significantly the thermal stability after ohmic contact formation, the InGaAs phase diagram predicts that the In(Ga,As) phases coexist with the $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases even though the volume fraction is extremely small. To eliminate the In(Ga,As) phases, addition of an element which forms high melting point (T_m) intermetallic compounds with In is essential [48]. The effect of the additional elements on the thermal stability was studied for GeInW and NiInW contact systems. According to binary phase diagrams, In and Ge are not miscible and no intermetallic compounds are formed [62]. However, Ni and In are miscible up to 14 at.% In at 900°C, forming several intermetallic compounds with a wide range of Ni/In composition ratios [62]. These high melting point compounds provided additional thermal stability to ohmic contacts with thin In. (The top W layer was primarily used as a cap layer for the contacts and did not influence the metallurgical interaction with In.)

Fractional changes in the R_c values of the GeInW and NiInW contacts during isothermal annealing at 400 and 500°C are shown in Fig. 9 [48]. Note that the R_c values of the GeInW

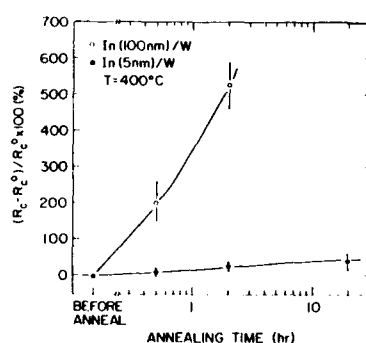


Fig. 8. Fractional changes of contact resistances of InW contacts during annealing at 400°C [53].

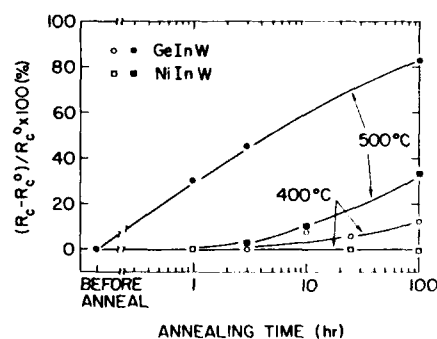


Fig. 9. Fractional changes of contact resistances of GeInW and NiInW contacts during annealing at 400 or 500°C [48].

contacts increase during isothermal annealing at 400°C, but those of the NiInW contacts stayed constant even after annealing for 100 hrs. TEM observation showed that the In(Ga,As) phases formed Ni_3In compounds which have the melting point higher than 900°C [58]. Therefore, addition of elements such as Co, Pd, Pt, or Mn will improve the thermal stability by forming high T_m compounds with In(Ga,As).

The micrograph of the NiInW contact after annealing at 400°C for 100 hrs is shown in Fig. 10 [50]. It is seen that the surface is extremely smooth, although the contact was formed by annealing at 900°C.

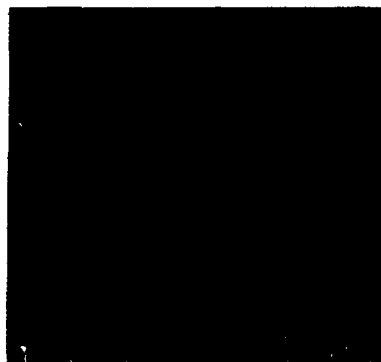


Fig. 10. Optical micrograph of NiInW ohmic contact annealed at 900°C by RTA and then annealed at 400°C for 100 hrs [50].

MESFET with NiInW ohmic contacts

Self-aligned refractory WSi MESFETs with NiInW ohmic contacts have been fabricated [51]. These devices showed excellent device performance. Schottky barrier heights of 0.77 eV and ideality factors of 1.1 were obtained, and the maximum square-law coefficient (K) values of 0.17 ($\text{mA}/\mu\text{m}^2$) were obtained for 1 μm gate FETs. These values are close to those obtained routinely in our laboratories in devices with AuNiGe ohmic contacts.

The thermal stabilities of the MESFETs with the NiInW ohmic contacts were studied as functions of annealing temperature and time. Changes in the K values for the devices with 1 μm -gates were measured during isothermal annealing at 400, 450, or 500°C and are shown in Fig. 11 [51]. The same sample was annealed successively at each temperature. No significant change

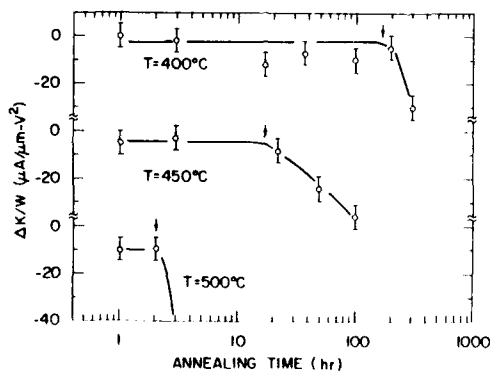


Fig. 11. Changes in K values during annealing at 400, 450, or 500°C for 1 μm MESFETs with NiInW ohmic contacts [51].

in the K-values was observed after annealing at 400°C for 180 hrs, 450°C for 18 hrs, and 500°C for 2 hrs. Note that significant decrease in the K values was observed for the MESFETs with the AuNiGe ohmic contacts after annealing at 400°C for less than 5 hrs. Thus, the thermal stability of the devices was significantly improved simply by replacing the AuNiGe with the NiInW ohmic contacts.

SUMMARY

In the present paper it was pointed out that the microstructure at metal/GaAs interfaces of indium-based ohmic contacts strongly influenced the electrical properties and the thermal stability. The fabrication process was found to control the microstructure. The processes and microstructures of the "traditional" and "recent" ohmic contacts are given in Table I.

Table I. Fabrication processes and microstructures of "traditional" and "recent" ohmic contacts.

	"traditional" contacts	"recent" contacts
<u>Fabrication process</u>		
In layer thickness	thick	thin
Annealing method	FA	RTA
Deposition method	layer	coevaporation
<u>Interfacial microstructure</u>		
Density of $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases	low	high
Density of $\text{In}(\text{Ga,As})$ phases	high	low
Melting points of In compounds	low	high

The main reason that the "traditional" contacts provided relatively high contact resistances, poor surface morphology, and also poor thermal stability was due to the small total area of $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases in contact with GaAs and formation of a large volume fraction of low melting point $\text{In}(\text{Ga,As})$ phases after contact formation. Additions of third elements to these "traditional" contacts did not improve the thermal stability, because the amounts of In were much larger than those these elements could absorb by forming high T_m In compounds. "Recent" NiInW ohmic contacts provide excellent thermal stability and low resistance due to the increase in the total area of $\text{In}_x\text{Ga}_{1-x}\text{As}$ phases in contact with GaAs and to reduction of the volume fraction of $\text{In}(\text{Ga,As})$ phases. MESFET devices prepared with this ohmic contact show excellent device performance and thermal stability far exceeding the requirements of the wiring, insulation, and packaging processes of current Si technology. In addition, the device stability during 450°C annealing allows increased flexibility in the development of the future packaging processes, the shallow penetration depth allows NiInW contacts in use in the shallow junction devices, and absence of contact edge deterioration reduces the source resistance by reducing distance between ohmic and Schottky contacts. The replacement of the current AuNiGe by NiInW ohmic contacts has the potential to significantly improve GaAs device performance and allows increased levels of integration.

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OHMIC CONTACT FORMATION MECHANISM IN THE Ge/Pd/n-GaAs SYSTEM

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Abstract

Annealed Ge/Pd/n-GaAs samples utilizing substrates with superlattice marker layers have been analyzed using high resolution backside secondary ion mass spectrometry and cross-sectional transmission electron microscopy. Interfacial compositional and microstructural changes have been correlated with changes in contact resistivity. The onset of good ohmic behavior is correlated with the decomposition of an intermediate epitaxial $\text{Pd}_4(\text{GaAs}, \text{Ge}_2)$ phase and solid-phase regrowth of Ge-incorporated GaAs followed by growth of a thin Ge epitaxial layer.

Introduction

The mechanism of ohmic contact formation in the standard alloyed Au-Ge-Ni/GaAs contact remains disputed to this day [1,2]. One of the primary reasons for this is the difficulty in analysis due to the non-planar interfacial morphology of this contact. Roughness on the order of $\sim 1500\text{\AA}$ is seen even after careful surface preparation [3]. Some proposed mechanisms are based upon this non-planar spiking nature of the contact [1] while others typically revolve around one of two themes. The first involves lowering of the barrier height between the contact and the GaAs. This may occur if a low conduction band discontinuity heterojunction, such as n-Ge/n-GaAs, is formed. The second theme centers around the formation of a highly doped n^+ GaAs interfacial layer. At sufficiently high doping levels, conduction may be dominated by electron tunneling. Formation of this layer could take place by diffusion of Ge into the GaAs or by dissolution of GaAs into the contact followed by regrowth of Ge-doped GaAs during the alloy cycle.

Most analysis techniques capable of looking for heterojunctions or interfacial doped layers are two-dimensional in nature. Even though they may only sample a thin region or are capable of high-resolution depth profiling, they average over the probe cross-sectional area. Hence, in order to obtain any useful information, the contact studied should be laterally homogeneous at each point in depth over the cross-sectional area of the analysis probe. The alloyed Au-Ge-Ni contact does not fit this criterion.

In this study, high resolution interfacial analysis of annealed Ge/Pd/n-GaAs [4,5] contacts is reported. These contacts undergo limited solid-phase reactions and retain interfacial planarity on a nearly atomic scale. Hence, resolution in depth profiling of these contacts will be limited by inherent analysis technique resolution rather than by sample morphology. A greater understanding of the ohmic contact formation mechanism is gained by correlating these high-resolution interfacial studies with the contact electrical behavior.

The predominant reaction in the Ge/Pd/GaAs contact is that between Ge and Pd. Excess Ge over that necessary to react with the Pd to form PdGe was found to be essential in obtaining low values of contact resistivity. In addition, a very limited reaction between the Pd and the GaAs was observed and speculated to be essential in the ohmic contact formation process. After sufficient annealing, the excess deposited Ge in the structures is transported across the PdGe layer to grow epitaxially on the GaAs [4].

Since the Ge/GaAs junction may lead to a low barrier heterojunction, it was not clear whether this low barrier or surface modification of the GaAs was responsible for ohmic behavior. In studies of the analogous annealed Si/Pd/GaAs system, it was found that ohmic characteristics resulted without the formation of a detectable group IV element/GaAs heterojunction. Transmission electron microscopy (TEM) showed evidence for solid-phase regrowth of a thin ($<100\text{\AA}$) GaAs surface layer after decomposition of the intermediate Pd-GaAs phase[6]. Further support for the mechanism of solid-phase regrowth of GaAs came from studies of the analogous Si/Ni/GaAs system[7]. In an investigation of the Ge/Pd/AlGaAs system, it was found that the onset of good ohmic behavior was correlated with the decomposition of the epitaxial Pd-AlGaAs phase[5]. In light of the previous work, it was speculated that decomposition of this intermetallic phase led to solid-phase regrowth of AlGaAs at the contact/substrate interface.

Experimental

Substrates were (001) GaAs wafers with the following epitaxial layers grown by molecular beam epitaxy (MBE): 100\AA GaAs:Si/ $8\times\{100\text{\AA}$ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$:Si/ 100\AA GaAs:Si/ $4\times\{100\text{\AA}$ $\text{Al}_{0.1}\text{Ga}_{0.9}\text{As}$ / 400\AA GaAs/ 1000\AA AlAs/ 5000\AA $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$ / 5000\AA GaAs buffer. Samples were degreased with trichlorethylene, ultrasonically cleaned with acetone and isopropyl alcohol, rinsed in HCl:H₂O(1:1 by volume) until hydrophobic, rinsed in deionized H₂O, and blown dry with N₂. For contact resistivity measurements, substrates with epitaxial layers doped with $1\times 10^{18}\text{cm}^{-3}$ Si were prepared with contact structures conforming to the transmission line model (TLM). Samples were then immediately loaded into an ion-pumped electron beam evaporator with a base pressure of 1.1×10^{-8} Torr. Pd (500\AA) was deposited at $6\text{\AA}/\text{sec}$ at 1.5×10^{-7} Torr. Ge (1300\AA) was then deposited, without breaking vacuum, at $12\text{\AA}/\text{sec}$ at 2.0×10^{-7} Torr. As a substrate reference, another sample was cleaned and loaded into the evaporator at the same time; on it, only 1300\AA of Ge was deposited. Samples with the Ge/Pd deposition were annealed in a flowing forming gas ambient (15% H₂ in N₂) at temperatures between 200°C and 325°C for 30 minutes. Unannealed and annealed samples were characterized by contact resistivity measurements (TLM), glancing angle x-ray diffraction with a Read camera, cross-sectional TEM, and secondary ion mass spectrometry (SIMS). TEM was performed using a JEOL 4000FX at 400keV. The SIMS instrument was an Atomica 3000-30 ion microprobe using 2.3keV O₂⁺ ions. Samples were profiled with the beam penetrating either from the contact surface down or from the substrate backside up through the contact. For the backside SIMS, the contact surface was protected using wax and the backside was mechanically thinned to $\sim 50\mu\text{m}$, etched to the $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$ layer using H₂O₂-NH₄OH, and the $\text{Al}_{0.6}\text{Ga}_{0.4}\text{As}$ and AlAs layers were removed using an HF based etch[8]. For calibration purposes, Ga- and As-implanted PdGe samples were also analyzed.

Results

As-deposited contacts were rectifying, even after H₂O₂ etching of the Ge top layer. After annealing at 200°C for 30 minutes, samples displayed poor ohmic behavior with contact resistivity greater than $10^{-4}\Omega\text{-cm}^2$. Samples annealed at 225°C displayed good ohmic behavior with $9\times 10^{-7}\Omega\text{-cm}^2$ contact resistivity. After annealing at either 250°C or 325°C, the contact resistivity reached $6\times 10^{-7}\Omega\text{-cm}^2$.

Glancing angle x-ray diffraction showed diffraction rings due to polycrystalline Pd in the as-deposited sample. The 200°C sample diffraction pattern exhibited diffraction rings due to polycrystalline PdGe and diffraction spots due to an epitaxial layer. The lattice constant of

this layer corresponds to either Pd_4GaAs or Pd_2Ge . The 225 and 250°C sample patterns only showed PdGe diffraction rings. In the 325°C sample pattern, PdGe rings and spots due to epitaxial Ge were evident.

Low magnification cross-sectional TEM views can be seen in figure 1. The superlattice and a 15Å oxide layer are evident in the sample with only amorphous Ge deposited (figure 1a). After a 200°C anneal, most of the Pd has reacted with the Ge to form polycrystalline PdGe (figure 1b). Excess amorphous Ge remains on the sample surface and a thin $\text{Pd}_4(\text{GaAs}, \text{Ge}_2)$ layer exists at the contact/substrate interface. After annealing at 325°C, the PdGe is on the sample surface and the excess Ge is now at the contact/substrate interface and is epitaxial to the substrate.

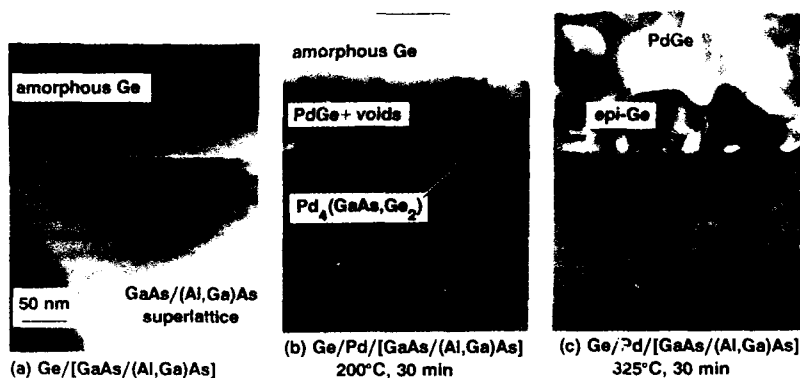


Fig.1 Cross-sectional TEM images of (a) as-deposited $\text{Ge}/[\text{GaAs}/(\text{Al,Ga})\text{As}]$, (b) $\text{Ge}/\text{Pd}/[\text{GaAs}/(\text{Al,Ga})\text{As}]$ after annealing at 200°C for 30 min, and (c) $\text{Ge}/\text{Pd}/[\text{GaAs}/(\text{Al,Ga})\text{As}]$ after annealing at 325°C for 30 min.

The reactions at the interface between the contact and the GaAs can be seen much more clearly in the higher magnification views in figure 2. The original GaAs layer under the contact, as measured in figure 2a was $93 \pm 3 \text{Å}$. After annealing at 200°C (figure 2b), the interfacial epitaxial layer had consumed GaAs such that $60 \pm 5 \text{Å}$ remained. The 325°C sample (figure 2c) displayed an upper GaAs layer of $85 \pm 4 \text{Å}$. Above this lies a $40 \pm 10 \text{Å}$ epitaxial layer which displays the same contrast as that in the upper epitaxial Ge layer. Some voids are seen in figure 2c between the two Ge layers.

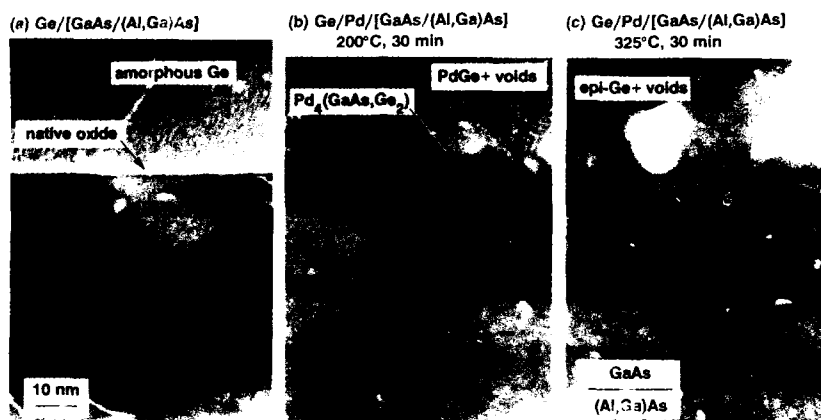


Fig. 2 Higher magnification cross-sectional TEM images of the interfacial regions in figure 1. The initial condition of the uppermost GaAs layer may be ascertained from (a). $\text{Pd}_4(\text{GaAs}, \text{Ge}_2)$ growth has consumed GaAs as seen in (b). Decomposition of the $\text{Pd}_4(\text{GaAs}, \text{Ge}_2)$ leads to a thicker GaAs surface layer in (c). This is indicative of solid-phase consumption and regrowth of a thin GaAs surface layer.

The backside SIMS spectra in figure 3 for the 325°C annealed sample shows that the Ge signal rises from background level in the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer, about mid 10^{18}cm^{-3} , to full height in the Ge epitaxial layer within less than 100Å. The Ga in the PdGe overlayer is at about the 1% level by comparison with a Ga-implanted PdGe standard. In figure 4, the backside SIMS Ge profile from the 325°C sample is overlaid with the Ge profile from the Ge/GaAs sample. The Ge sensitivity is enhanced in the PdGe due to the presence of Pd. The Ge signal in the annealed PdGe sample rises at the same rate as that in the Ge/GaAs sample but rises $25 \pm 10\text{Å}$ deeper.

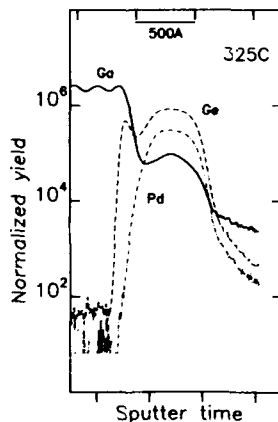


Fig. 3 Backside SIMS sputter depth profiles for 325°C 30min annealed $\text{Ge/Pd}[\text{GaAs}/(\text{Al,Ga})\text{As}]$ using a 2.3keV O_2^+ beam. The depth scale marker is for GaAs only.

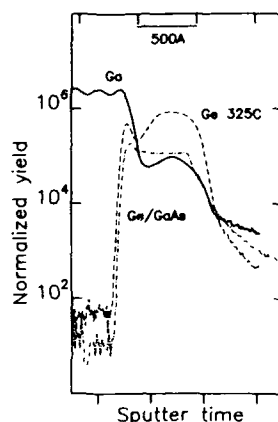


Fig. 4 Backside SIMS sputter depth profiles of an unannealed Ge/[GaAs/(Al,Ga)As] and 325°C 30min annealed Ge/Pu/[GaAs/(Al,Ga)As] samples using a 2.3keV O_2^+ beam. The depth scale marker is for GaAs only.

Discussion

An understanding of the ohmic contact formation mechanism develops from correlation of the contact electrical and metallurgical behavior. This is shown schematically in figure 5. Upon deposition or after heat treatment of less than 100°C, Pd moves through and disperses the oxide to form a thin epitaxial Pd_4GaAs layer. The thickness of this phase is limited to $\sim 100\text{\AA}$. The major reaction is between Pd and Ge to first form Pd_2Ge and then $PdGe$. After the Ge reaches the Pd_4GaAs , some Ge may be incorporated into this layer. While this interfacial epitaxial phase is present, as in the 200°C sample, the contact does not demonstrate good ohmic behavior. After annealing at temperatures $\geq 225^\circ\text{C}$, the presence of excess Ge drives the decomposition of the epitaxial $Pd_4(GaAs,Ge_2)$ layer. The result of this decomposition is the solid-phase regrowth of Ge-incorporated GaAs, followed by the growth of a thin epitaxial Ge layer. Deep ($>100\text{\AA}$) penetration of high levels ($>5 \times 10^{18}\text{cm}^{-3}$) of Ge is not found below the contact. At this point, the contact displays good ohmic behavior with contact resistivity in the $10^{-7}\Omega\text{-cm}^2$ range. Annealing at temperatures of $\sim 325^\circ\text{C}$ leads to solid-phase transport and epitaxy of the excess amorphous Ge. The contact resistivity, however, does not change.

Conclusion

The onset of good ohmic behavior is correlated with the decomposition of the intermediate epitaxial $Pd_4(GaAs,Ge_2)$ phase and solid-phase regrowth of Ge-incorporated GaAs followed by the growth of a thin Ge epitaxial layer. By using backside SIMS and TEM with thin marker layers, it is seen that all GaAs is accounted for in the reaction. About 35Å of GaAs is consumed during Pd_4GaAs formation. About 25Å of GaAs is seen to regrow. The 1% GaAs in the $PdGe$ layer corresponds to $\sim 10\text{\AA}$ GaAs. Hence, $35\text{\AA}(\text{consumed GaAs}) = 10\text{\AA}(\text{GaAs in contact}) + 25\text{\AA}(\text{regrown GaAs})$.

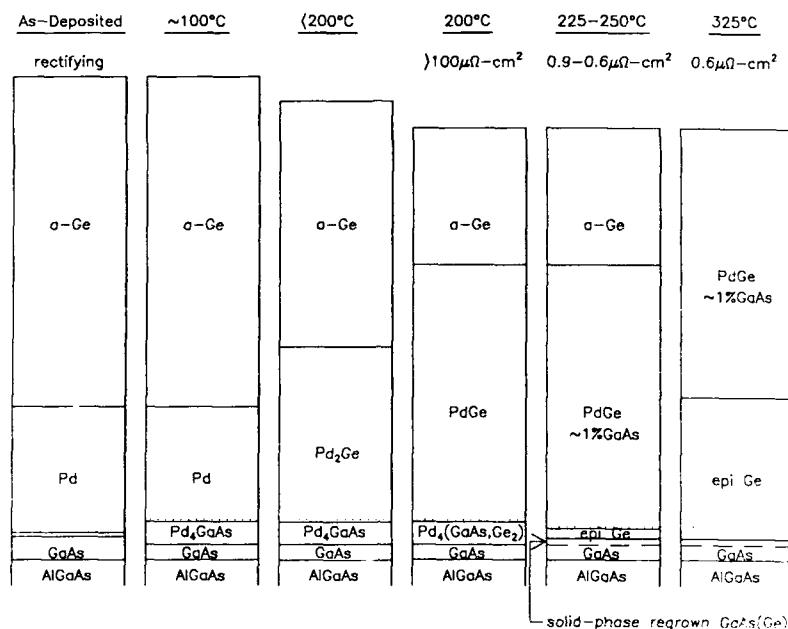


Fig. 5 Hypothetical reaction sequence as a function of anneal for the Ge/Pd/[GaAs/(Al,Ga)As] structure.

Acknowledgements

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THE AuZn/GaAs HETEROJUNCTION: EVIDENCE OF VARYING SOLID STATE REACTIONS

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ABSTRACT

Au-Zn is one of several metal systems applied to p-GaAs to form ohmic contacts. Although it exhibits a fair degree of reliability, the thrust toward higher power and adverse environments raises concern. Observations indicate that the electrical and mechanical properties as well as the stability of AuZn/GaAs vary with Zn thickness. In this study devices with thin and thick layers were tested visually, mechanically and using SEM and X-ray diffraction techniques. Results revealed significantly different reactivity and product chemistry that could significantly affect overall device performance.

INTRODUCTION

The criteria for an acceptable ohmic contact are well known. Contacts should exhibit low electrical resistance, good mechanical adhesion and long term stability under the intended environments. Ideally, the deposition process itself should be relatively simple and inexpensive with a high degree of control or reproducibility.

In the real laboratory or production situation, however, contacts are less than ideal in that all of the above requirements cannot be simultaneously met. The Au-Zn system is one such serviceable metallization system applied to p-GaAs, but concern exists with respect to survivability under conditions of ever increasing power and environments of high or cycling temperature [1]. Layers deposited by two different investigators do not necessarily behave similarly. It is well known that the electrical and mechanical characteristics differ with deposition techniques and processing parameters (temperature, time, etc.) [2,3]. However, the effect of the relative thicknesses of the metal layers deposited is less understood. In this study, two thicknesses of Zn in the overall AgAuZnAu/GaAs stack were examined: 3000Å and 400Å. Earlier observations using samples with thick and thin Zn layers deposited upon GaAs photovoltaic devices had indicated higher mean open circuit voltage (V_{oc}), less V_{oc} deviation and a higher threshold to damage by surges in reverse bias in the thick case. Yet the same units exhibited slightly decreased adherence.

Only limited information can be drawn from the Au-Zn phase diagram of Figure 1. Although of some use in identifying the various known compounds, the data presented are not necessarily broadly applicable to AuZn layers. Samples prepared in the generation of this binary diagram consisted of pure Au and pure Zn thoroughly mixed and homogeneously reacted into three dimensional solid crystals under equilibrium conditions of constant, well-defined temperatures for extended periods of time. In contrast, deposited Au and Zn films are contaminated by their close proximity to foreign surfaces, consist of two dimensional layers with very large surface areas, and interact at unknown conditions: the temperatures are neither well controlled nor extended to allow adequate time for full reaction or even complete crystallization [4].

EXPERIMENTAL PLAN AND MATERIALS

The plan involved depositing AuZnAu layers on GaAs substrates and testing. Except for Zn thickness, samples were in every way identical. After parallel processing they were examined visually, mechanically and by SEM and X-ray analyses. The substrate consisted of <100> n-type GaAs upon which a p-type layer was grown by metal organic chemical vapor deposition (MOCVD). Dopant densities were $2.5 \times 10^{17} \text{cm}^{-3}(\text{Se})$ and $2 \times 10^{18} \text{cm}^{-3}(\text{Zn})$ respectively. The pn junction depth was approximately 0.5µm.

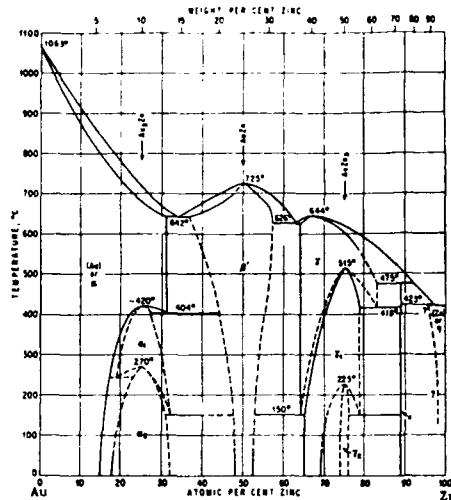


Figure 1. Equilibrium AuZn Phase Diagram.

The specular surface was prepared immediately before metal deposition, after solvent cleaning the GaAs was etched in a mixture of H_2SO_4 , H_2O_2 and distilled water (5:1:1). Metals were then sputter deposited using a Perkin Elmer 2400-8S deposition system. The samples prepared, listed in Table 1, consisted of four groups of wafers: A,B,C and D. In all cases the initial Au layer was 500Å followed immediately by either 400Å or 3,000Å of Zn and then 2000Å of a second deposition of Au. Samples in Groups A and B were then capped with a final 35KÅ layer of silver. Approximately 1000Å of this was deposited in the same sputtering unit without breaking vacuum; the remainder was applied by e-beam evaporation. Groups C and D were identical, but without silver. After metallization, all samples were cleaved in two. One half of each was temperature treated ("annealed") at 450°C for 4.0 minutes (85% N_2 ; 15% H_2), while the other was not (RT). Numerous other samples with the same metal layers on semi-insulating GaAs and SiO_2/Si substrates were also prepared as controls.

RESULTS

A summary of results is shown in Table 2.

TABLE 1: Sample Set

Group	Metal Stack	Zn	Temp.
A	AuZnAu/Ag	Thick/3000Å	450°C/RT
B	AuZnAu/Ag	Thin/400Å	450°C/RT
C	AuZnAu	Thick/3000Å	450°C/RT
D	AuZnAu	Thin/400Å	450°C/RT

TABLE 2: Characterization Techniques and Results

Technique	Focus Thin	Observed	Differences	Thick
Visual	Underside	Color	Yes	Gray
Mechanical	Flakes	Flexibility	Yes	Brittle
SEM	Surfaces	Inhomogeneity	Yes	Regular
		Reactions	Yes	Spherulitic
X-Rays	Metals	Phases	Yes	AuZn_3
				Au

Visual

Unassisted visual examination resulted in little obvious distinction between the uppermost Ag (Groups A and B) or Au (Groups C and D) surfaces of the prepared samples (Table 1). However, inspection of the underside of these metal stacks revealed striking differences. Specimens were examined after removal either from the GaAs surface by means of the ordinary liftoff procedure or from the deposition equipment fixturing. In thin Zn samples (groups B and D), regardless of the presence of Ag, the color of the underside was deep yellow, while with thick Zn (Groups A and C) the color was a dull metallic gray. Results were independent of the annealing treatment.

Mechanical

Because of their configuration the irregular specimens described above did not lend themselves well to any known means of calibrated mechanical testing. However, in general it can be said that those with thick Zn were significantly more brittle. Whereas thin samples would flex considerably under pressure, thick ones would shatter. This effect was repeatable and independent of the addition of Ag or the post processing annealing treatment.

It is clear from the above that the GaAs surface comes into intimate proximity with different AuZn phases in thin and thick cases. Accordingly, the important GaAs to metal interface - both electrically and mechanically - can be expected to be affected.

Scanning Electron Microscopy

Five significant distinctions between thick and thin Zn samples were observed via scanning electron microscopy (SEM) and energy dispersive X-ray analyses (EDAX): texture, coverage, reactions, reaction consistency and anomalous features. A summary of the data is given in Table 3. These results center upon samples without silver (Groups C and D) since an additional deposition of 35KÅ over the basic Au and Zn layers masked distinctions of importance. Also, observations are based upon specimens before annealing.

In the case of thick Zn, the uppermost Au was considerably more rough and granular. The overall appearance was distinct hillocks, as opposed to flat planes. EDAX analysis of the thick films' high areas revealed them to be Au rich, while low areas were predominantly Zn. On the other hand, the same analysis of surfaces of thin Zn samples revealed only Au. In addition, the incidence of incomplete coverage in the form of randomly occurring craters was more predominant in thin Zn.

There was evidence of different reactions between the Au and the Zn layers, implying the presence of different phases. To further investigate this, special GaAs samples were prepared with only the first two layers, Au and Zn, deposited. The resulting micrograph of a thin Zn sample before annealing, Figure 2a, demonstrates a nonuniform surface reaction. Dark areas correspond to a Zn rich surface, while light areas to Au. When the same area is examined at a 60° angle, Figure 2b, surface swelling is evident - again indicating reactivity of the dark areas.

TABLE 3: SEM/EDAX Results

Observed	Thin	Thick	Comments
Texture	Smoother	Coarser	More Hills and Valleys With Thick
	Less Granular	More Granular	Larger Spherical Modules With Thick
Coverage	Less Uniform	More Uniform	EDAX Differences in Zn and Au
Reaction	Dendritic	Spherulitic	Different Reactions
Reaction Consistency	Less Uniform	More Uniform	Fuller Coverage with Thick; Spotty Coverage with Thin
Anomalous Features	Reactivity Craters	Reactivity Craters Bubbles	More Predominant With Thin

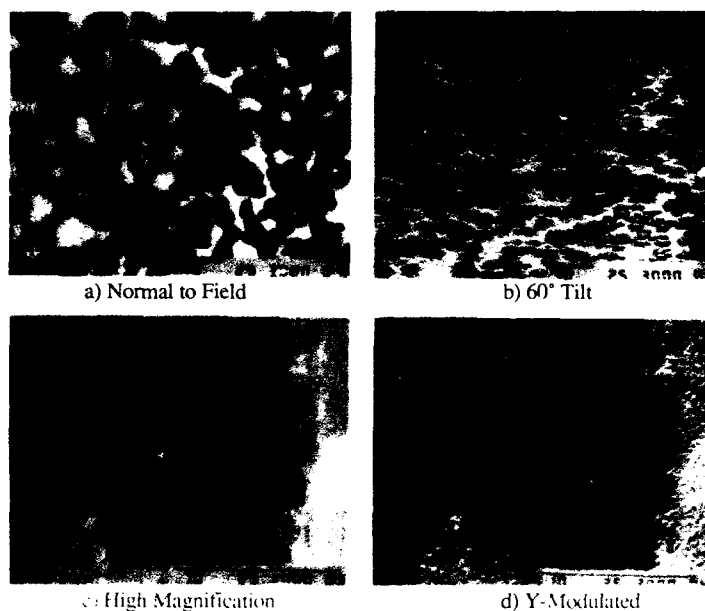


Figure 2.
Au and Thin
Zn (500Å and
400Å) on
GaAs Before
Annealing

Spherulitic crystallites are evident in an enlarged view of the same sample in Figure 2c. Here the existence of nucleation centers and the development of crystallite formation radially is clearly seen. Using the Y-modulation feature of the SEM, the topography can be accentuated, Figure 2d, and differences in surface penetration between unreacted (light) and reacted (dark) areas are demonstrated. In fact, based upon the scale, it is estimated that reacted areas exhibit a peak to peak height of up to 5000Å. This upon a surface of only 500Å of Au and 400Å of Zn implies reaction with, consumption of, or penetration into the GaAs substrate itself [5].

Thick Zn surface reactivity was also explored. In Figure 3a evidence of a different type of reactivity is seen by the irregular light and dark patches. However, for the most part coverage is more uniform than in the thin case. In Figure 3b, taken at an angle, anisotropic crystal formation upon the smaller hemispherical mounds is exhibited.

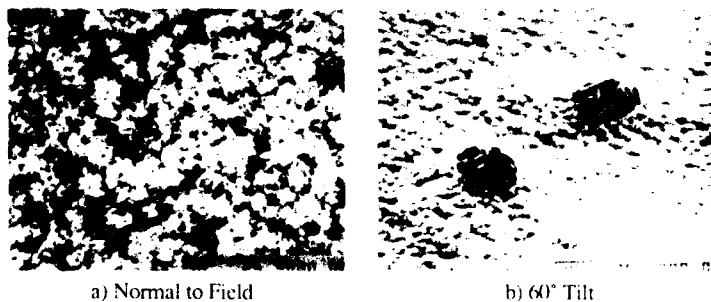


Figure 3.
Au and Thick
Zn (500Å and
3000Å) on
GaAs Before
Annealing

The same micrograph is dominated by two large, roughly circular irregularities that appear to be broken film blisters. This is one of many anomalous features that were seen during the course of this SEM investigation. Such bubbles, observed only in thick Zn samples, may be due to heating during the longer 3000Å Zn deposition. However, an exhaustive topographical study was not conducted, and neither the frequency of these in thick Zn, nor their complete absence in the case of thin Zn can be confirmed. The full effect of these and the other surface anomalies is not known at this time. However, it is obvious that any major disruption in the surface integrity of metal thin films is undesirable since there could be an effect upon final solar cell mechanical and electrical properties.

SEM analyses upon samples after annealing were also conducted. Thin Zn showed little difference compared to untreated samples. On the other hand for thick Zn, some softening of the granularity was observed although voids between grains remained indicating continued nonuniformity in coverage.

X-Ray Diffraction

The summary of X-ray powder diffraction data is shown in Table 4. Samples were tested before annealing (NA), after annealing (A) and after 468 temperature cycles at 120 °C (TC). The resulting crystalline phases detected are listed in the last three columns in which the symbols vw (very weak), w (weak), m (medium), s (strong) and vs (very strong) give some relative measure of signal strength and, therefore, phase presence. In interpreting results the finite penetration depth, to approximately 100 µm, of the X-ray beam must be kept in mind.

Samples with silver (Groups A and B) revealed only crystalline Ag in the unannealed case and AuAg solid solution after annealing. Notably, Au migration and/or development of crystalline Au and AuAg continued with even the limited thermal cycling performed in this study.

AuZn intermetallics were detected in samples without Ag (Groups C and D). As shown in Figure 4a for the case of thin Zn before annealing (Group D), there was a strong diffraction signal due to Au and a weaker response for AuZn₃. With annealing, Figure 4b, there is no presence of AuZn₃ whatsoever. The behavior of thick Zn, shown in Figures 5a and 5b, (Group C) differs significantly. Here both Au and AuZn₃ are major phases in the sample before annealing with Au effectively disappearing after annealing.

TABLE 4: X-Ray Diffraction Results

Group	Metal Stack	Compounds Observed		
		(NA)	(A)	(TC)
A	Au, Thick Zn, Au/Ag	Ag(s)	Ag(s)	-
		-	AuAg(vs)	AuAg(s)
		-	-	Au(s)
B	Au, Thin Zn, Au/Ag	Ag(m)	Ag(m)	-
		-	AuAg(s)	AuAg(w)
		-	-	Au(w)
C	Au, Thick Zn, Au	Au(s)	Au(vw)	-
		AuZn ₃ (s)	AuZn ₃ (s)	AuZn ₃ (s)
D	Au, Thin Zn, Au	Au(s)	Au(s)	-
		AuZn ₃ (w)	-	-
		-	-	Au ₃ Zn(s)

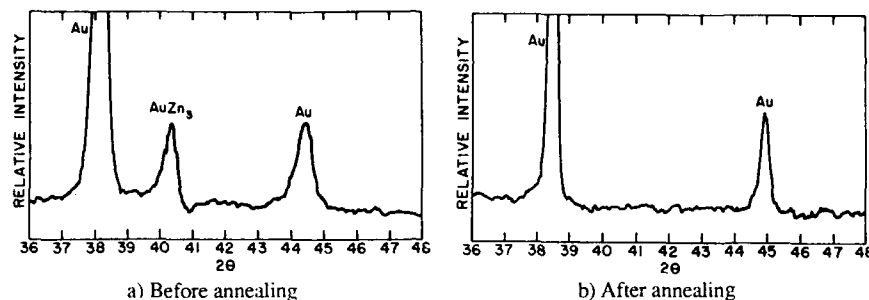


Figure 4. X-Ray Results: Thin Zn

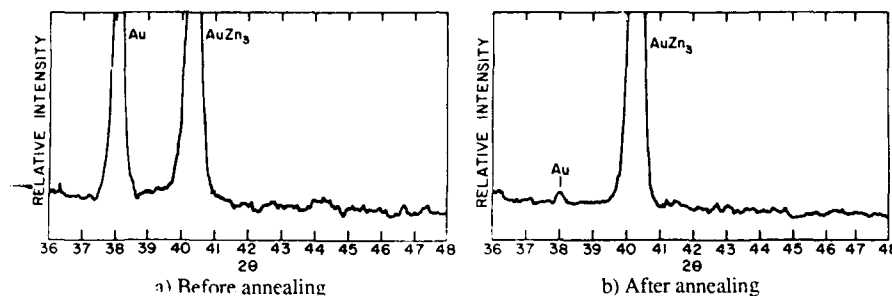


Figure 5. X-Ray Results: Thick Zn

There is an argument that the absence of an X-ray peak for AuZn_3 after thin Zn annealing does not necessarily mean no presence of AuZn_3 . The idea is that crystalline AuZn_3 may indeed exist, but it is buried under a 2000Å layer of crystalline Au (note the strong Au signal in this sample). However, this possibility is not supported by the thin Zn unannealed data in which a distinct AuZn_3 presence is shown regardless of an already-existing equally strong Au phase signal.

With temperature cycling, phases continue to evolve. In the thin Zn sample the strong Au presence disappears to be replaced by a completely new phase Au_3Zn . This is due to the atomic ordering of non-crystalline Au and Zn during excursions from low to high temperature. However, the highest temperature achieved was only 120°C - well beneath the range of any phase formation indicated in Figure 1. This Au_3Zn phase does not appear after cycling of thick Zn. However, changes do occur since the Au signal after annealing disappears leaving only a strong AuZn_3 crystalline presence.

X-ray analyses of the underside (GaAs side) of metal flakes from Group A and B samples revealed for both cases Au, Ag, AuZn_3 and AuAgZn_2 . However, with thick Zn, an additional peak at 41.3° was observed that does not correlate with any known Au, Zn, Ga, As, or oxide compound. The interpretation and significance of this signal remains in question.

DISCUSSION

Results indicate that the thickness of Zn in the AuZn system on GaAs is critical. More specifically, AgAuZnAu on GaAs samples processed identically except for the thickness of the

intermediate Zn were inherently dissimilar. Although in both cases the Au and Zn present definitely interdiffuse, the mixing of metals is not homogeneous [6] and results in distinctly different phases at the critical GaAs interface. The crystalline phases detected, although repeatable, do not correlate with the compounds indicated in the phase diagram based upon the relative proportions of Au and Zn present but are a function of diffusivity and thermal history [7]. With respect to the latter, the standard annealing process alters phase relationships in both thin and thick Zn cases. Finally, neither thick or thin systems are stable at up to 468 cycles at 120°C.

It was also observed that Zn in the thicker samples migrates more readily to the metal/GaAs interface and that the metallization is more brittle. SEM surface analysis revealed, especially in thin Zn units, irregularities sufficient to impact reliability as well as dissimilar reactivity levels and products. X-ray studies confirmed the presence of different AuZn phases at the GaAs interface. This study concludes that the properties of the AuZn to GaAs heterojunction are not dependent on the identity of the metals alone but vary greatly with thickness and process parameters which deliver different metallic products to this critical interface. These can be expected to trigger distinct solid state reactions with respect to the underlying GaAs which in turn affect electrical, mechanical and reliability characteristics [8].

Of key interest is the interdiffusion of the distinct metal systems into the GaAs surface. Ongoing research involves SIMS comparison of thin and thick Zn samples. Preliminary results confirm both a different mix of metals in the upper GaAs layer as well as different depths of penetration of the metals into the GaAs surfaces. With the annealing treatment, the interdiffusion of metals in the thin Zn samples is more marked and readily progresses to the level of the semiconductor junction while that for thick Zn samples is more limited. This suggests different GaAs to metal reactivity. The results of this study, showing different AuZn alloys existing at the metal to semiconductor interface, is consistent with the expectation of such different GaAs reactivity.

CONCLUSIONS

Au in samples with thicker Zn migrated more readily to the GaAs heterojunction, and the metallization was more brittle. Surface analyses revealed in thin Zn units irregularities sufficient to impact reliability. Also evident were dissimilar reactivity levels and products. X-ray studies confirmed the presence of different metallic compounds at the GaAs surface as a function of processing and environment. This study concludes that the properties of the AuZn to GaAs heterojunction are not dependent on the identity of the metals alone but vary greatly with thicknesses and process parameters. These affect solid state reactions and electrical, mechanical and reliability characteristics.

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EQUILIBRIUM PHASE DIAGRAMS FOR ANALYSIS OF THE OXIDATION OF III-V COMPOUND SEMICONDUCTORS

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ABSTRACT

The phases which result from the oxidation of III-V compound semiconductors can be predicted from a knowledge of the condensed phase portion of their equilibrium phase diagrams. Examples will be shown for arsenides, antimonides, and phosphides. Use of these diagrams explicitly presumes equilibrium growth conditions, and that assumption often fails. In such cases kinetic rather than thermodynamic factors dominate the determination of the observed phases. Examples of this phenomenon for anodic oxidation will be presented. Recent interest in high pressure oxidation conditions as a means of alleviating kinetic limitations will be discussed for InP. The phase diagrams can also be used to predict interfacial reactions under certain conditions and data for GaAs will serve to illustrate this point.

INTRODUCTION

Oxide phase diagrams [1] provide a variety of information relevant to predicting the composition of films which result during the oxidation of compound semiconductors. This paper is comprised of five Sections with the following contents: (I) Construction of III-V-Oxygen Equilibrium Phase Diagrams, (II) Products of Equilibrium Oxidation, (III) Modifications to Predicted Phases, (IV) Kinetic Considerations, and (V) Oxide-Substrate Reactions.

CONSTRUCTION OF III-V-OXYGEN EQUILIBRIUM PHASE DIAGRAMS

The process of constructing the III-V-oxygen phase diagrams has been dealt with in detail in the literature [1] so only a brief review of the basic principles will be presented here. For a given choice of Group III and Group V elements, one begins by specifying all the known condensed phases in the III-V-oxygen system. For purposes of illustration we will consider the specific case of Ga-As-O. The known condensed phases are Ga, GaAs, As, Ga_2O_3 , GaAsO_4 , As_2O_5 , As_2O_4 , and As_2O_3 . Gallium meta-arsenate, $\text{Ga}(\text{AsO}_3)_3$, may also exist but it is not well characterized. In addition, As_2O_4 disproportionates into As_2O_3 and As_2O_5 at a relatively low temperature. Once the phases have been specified, all possible phase diagrams can be written down by inspection. Figure 1 shows the possibilities for Ga-As-O (tie lines associated with As_2O_4 and $\text{Ga}(\text{AsO}_3)_3$ were not considered). The following implicit assumptions are involved in constructing any of the diagrams seen in Fig. 1: (a) solid solubility is ignored i.e. any tie line represents a two phase mixture of immiscible components, and (b) temperature and pressure are held constant. In conjunction with the Gibbs phase rule the latter constraint implies that all fields lying within the tie lines are three phase fields.

In order to differentiate which diagram represents the equilibrium phase diagram, one tests the relative stability of the various tie lines. Consider for example the relative stability of the Ga_2O_3 -As tie line versus the Ga- As_2O_3 tie line. Balanced equations are written ($2 \text{ Ga} + \text{As}_2\text{O}_3 = 2 \text{ As} + \text{Ga}_2\text{O}_3$), and thermodynamic data are used to evaluate which tie line is more stable. If available, the Gibbs energies of formation evaluated at the relevant oxidation temperature should be used. For example, the As- Ga_2O_3 tie line is more stable by 102 and 98 kcal at 300 and 500°K respectively. Since the Gibbs phase rule excludes the crossing of interior tie lines, this selection process serves to eliminate various forms of the phase diagram until only one final choice remains. The remaining diagram is designated as the equilibrium phase diagram. In many cases however, the Gibbs energies of formation are only known at 300°K, and for some of the lesser known materials such as GaAsO_4 , one must estimate even this data. As a consequence, extrapolating the form of the phase diagram to higher temperatures where practical oxidations occur may lead to potential errors.

Following these procedures, the equilibrium diagrams for representative arsenide, antimonide, and phosphide based semiconductors are presented in Fig. 2.

PRODUCTS OF EQUILIBRIUM OXIDATION

Under equilibrium oxidation conditions and assuming no loss of any of the phase products, the compositions of native oxide films on III-V substrates can be read directly from the phase diagrams by examining which tie lines are intersected by a line which connects oxygen to the respective III-V substrate. (Dashed line "A" in Fig. 2). Figure 2(b) shows that a multicomponent oxide film is expected on most semiconductors with the exception of InP and GaP, for which the diagrams predict single phase layers of InPO_4 and GaPO_4 respectively.

MODIFICATIONS TO PREDICTED PHASES

The oxide phases present on III-V materials are modified in two fundamental ways. The first results when growth does not occur under "near equilibrium" conditions, and will be discussed in detail in the next section. The second occurs when growth is near equilibrium, *i.e.* the phase diagram applies, but some phases are lost due to their relative volatilities. The thermal oxidation of GaAs is an example of the latter situation since both elemental arsenic and As_2O_3 have appreciable vapor pressures at typical oxidation temperatures. This process can be illustrated schematically by shifting dashed line "A" over to "B" in Fig. 2. The details of how "A" is shifted are determined by kinetic considerations. Application of the "lever rule" now shows that the film is depleted in As and As_2O_3 and that the surface zone is composed of both Ga_2O_3 and GaAsO_4 rather than just the latter product.

KINETIC CONSIDERATIONS

There are a number of growth techniques for which oxide phase formation is so rapid that growth occurs far from thermodynamic equilibrium. For example, gas phase plasma (RF or DC) and electrochemical (anodic) oxidation processes can grow films at rates around 1000Å/min. For GaAs, these films tend to be approximately 1:1 mixtures of Ga_2O_3 and As_2O_3 . In situations where kinetics dominates over thermodynamics, the oxide phases which result need no longer be in strict accord with the equilibrium phase diagram. Another example is the oxidation of GaP, which produces GaPO_4 under thermal oxidation conditions but mixtures of Ga_2O_3 and P_2O_5 when electrochemically anodized.

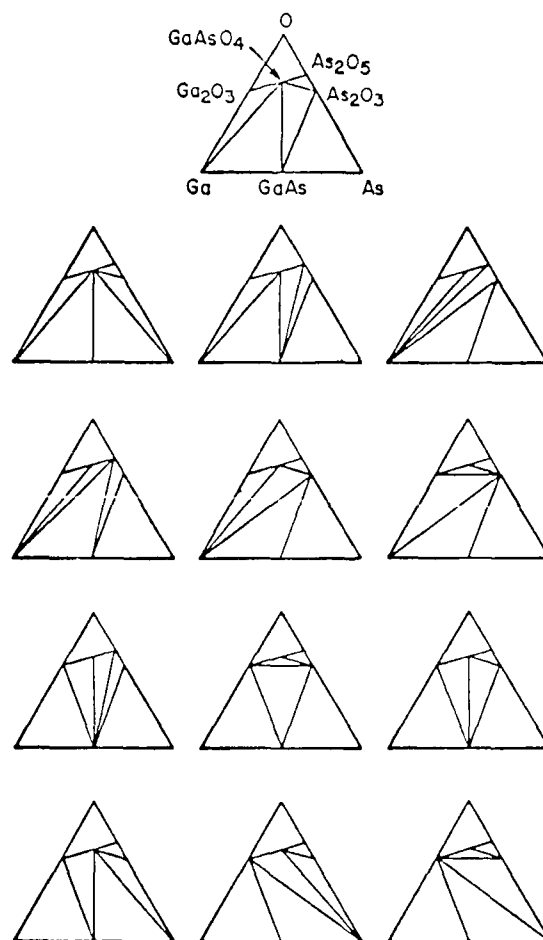


Fig. 1

Candidate forms of the equilibrium phase diagram for the condensed phase portion of the Ga-As-O system.

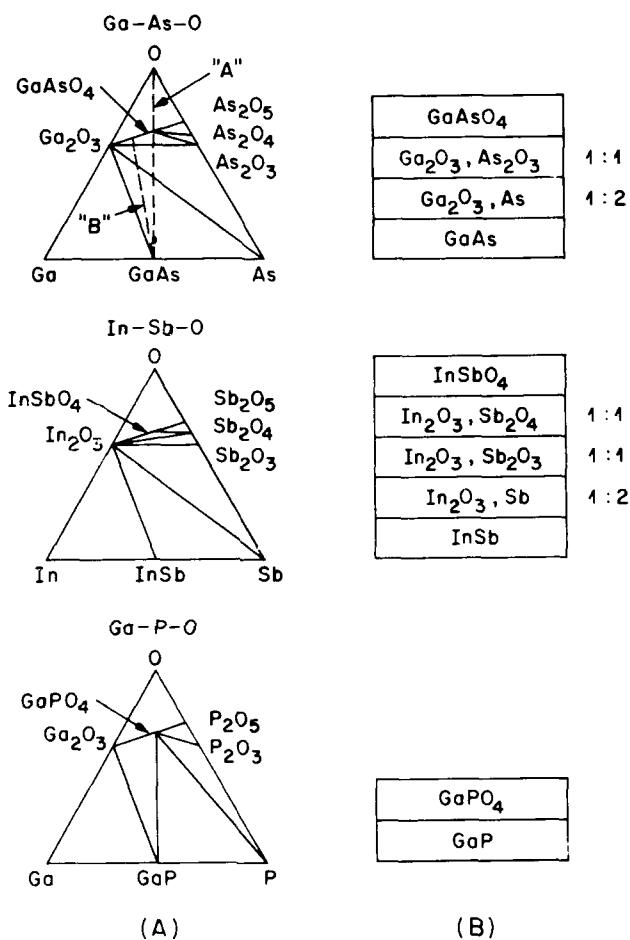


Fig. 2

(A) The form of the equilibrium phase diagrams for representative arsenides, antimonides, and phosphides from ref. [1]. The composition of the resulting oxides can be read from the diagrams by examining the tie lines intersected by the O-GaAs line "A". The resulting oxide film phases are shown in panel (B). If phases such as As_2O_3 or As are lost from the film, "A" has to be replaced with a line such as "B". The ratios of the phases in the film will also shift.

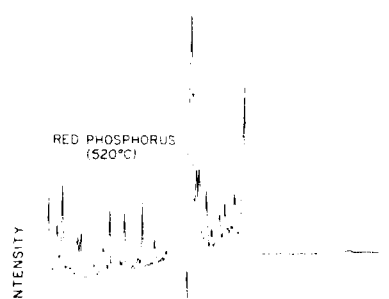


Fig. 3

Raman spectra of elemental red P and InP.

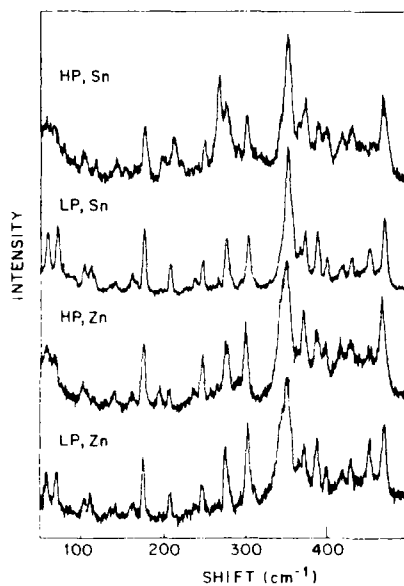
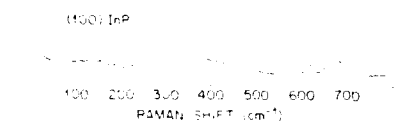
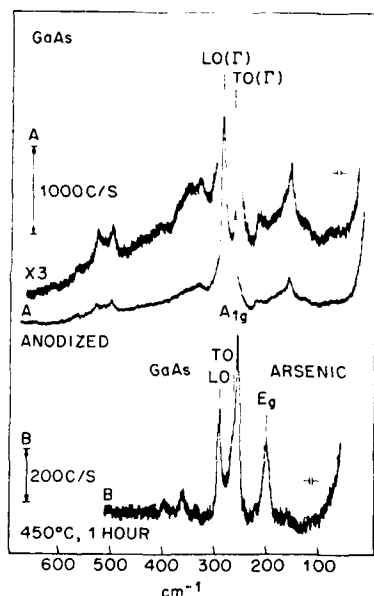


Fig. 4

Raman spectra of Sn and Zn-doped InP oxidized under high pressure (HP) and low pressure (LP) conditions. The phonon modes of red P are seen in both sets of spectra. Note the expansion of the horizontal scale relative to Fig. 3.



1 5

Raman spectra from (A) an electrochemically anodized GaAs wafer and (B) the same wafer after heating in vacuo for 1 hour at 450°C. The A_{1g} and E_g modes of crystalline arsenic are seen in addition to the LO and TO modes of the substrate.

One of the interesting problems associated with the In-P-O phase diagram is that single phase InPO₄ is predicted as the sole oxidation product from the equilibrium phase diagram. Although this prediction is borne out at relatively high oxidation temperatures (~650°C), Raman scattering [2] clearly shows the presence of elemental red P in films grown below 500°C. It was recently suggested [3] that high pressure oxidation might represent a path whereby the kinetic barriers which presumably influence the oxidation could be overcome in order to eliminate the elemental P.

Figures 3 and 4 show Raman spectra for InP, elemental red P, and thermally oxidized InP, the latter being run at 300 atmospheres of pure oxygen. It is clear that the phonon modes of red P are present in the oxidized films grown under high pressure conditions. It is thus seen that increasing the oxidation potential has not been effective in removing the elemental inclusions of red phosphorous which exist in these films for oxidation at 500°C. Oxidation at 650°C is also not practical because of blistering of the film. The elimination of the elemental P deposits in such films remains an unsolved problem.

OXIDE-SUBSTRATE REACTIONS

One of the consequences of growing an oxide film whose stoichiometry is far from equilibrium is that any subsequent thermal processing can drive both oxide-oxide and oxide-substrate interactions. An example of the former would be an anodic film on GaP which reacts according to $\text{Ga}_2\text{O}_3 + \text{P}_2\text{O}_5 = \text{GaPO}_4$ to yield the thermodynamically favored phase. An equally important class of reactions entails thermally induced interaction between some of the oxide components and the substrate. The anodic oxidation of GaAs followed by thermal treatment will be used to illustrate this case.

We start with an oxide whose initial components are Ga_2O_3 and As_2O_3 . Note in Fig. 2 that a tie line connects Ga_2O_3 and GaAs, *i.e.* no reaction is anticipated in that case. A tie line does not connect As_2O_3 with GaAs however. In order to "mentally" connect As_2O_3 and GaAs, note that the stable Ga_2O_3 -As tie line must be intersected. This implies that the following reaction is thermodynamically favored $\text{As}_2\text{O}_3 + 2 \text{GaAs} \rightarrow \text{Ga}_2\text{O}_3 + 4 \text{As}$. This reaction has been observed [4] after annealing anodic films at 400-450°C *in vacuo* and measuring the Raman spectrum as shown in Fig. 5. In all cases, elemental arsenic is generated via the previously mentioned reaction. The latter process represents a consideration in device processing of plasma or anodic oxides on many of the III-V materials.

SUMMARY

Equilibrium phase diagrams provide guidelines for estimating the phases present following the oxidation of III-V semiconductors. Their construction and use are mitigated by (1) the availability of a complete set of thermodynamic data, and (2) kinetic considerations involved under actual oxidation conditions. For oxide phases grown under nonequilibrium conditions, a variety of oxide-oxide and oxide-substrate reactions can occur under thermal processing conditions which drive the system toward equilibrium.

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MBE GROWTH OF $\text{Ca}_{1-x}\text{Sr}_x\text{F}_2$ ON (100), (111), (511), AND (711) GaAs SURFACES

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ABSTRACT

We have used molecular beam epitaxy to grow $\text{Ca}_x\text{Sr}_{1-x}\text{F}_2$ films of various thicknesses on GaAs substrates with different orientations, i.e. (100), (111)A, (511)A, (511)B, (711)A and (711)B. On all orientations, the same crystallographic direction is normal to the surface in both the substrate and fluoride film. For all orientations except (111), the fluoride surface is reconstructed with (111) facet. Without annealing, the best crystallinity is obtained for the (100), (111) and (511)B orientations.

INTRODUCTION

Calcium fluoride (CaF_2) and strontium fluoride (SrF_2) are insulators with wide bandgaps and low permittivities (12.1eV and 6.8, 11.2eV and 6.5, respectively) which can be grown epitaxially on a number of substrates. Their crystal structure is similar to diamond and zincblende structures with an additional atom in the basis. The lattice constant of mixed $\text{Ca}_x\text{Sr}_{1-x}\text{F}_2$ can be tuned between 5.464Å and 5.7996Å to match that of several technologically important semiconductors. Fluorides have therefore been considered for making high quality insulator-III-V interfaces, for passivation of III-V surfaces, and for providing crystalline substrates for semiconductor regrowth necessary for three-dimensional integration and opto-electronic devices. The principal problem associated with the high temperature growth of such heterojunctions is that the thermal expansion coefficients of the fluorides are about three times larger than that of GaAs and other III-V semiconductors.

The growth of $\text{Ca}_x\text{Sr}_{1-x}\text{F}_2$ lattice matched to GaAs has been demonstrated on (100) [1-4], (111)A [5,6], (111)B [1,4,5,6] and (110) [3] substrates. Fluorides grown on (100) substrates with a GaAs buffer layer were reported to have very flat surfaces with the best crystallinity among these three orientations. The crystallinity of the films grown on the (111)-oriented substrates was not as good, perhaps due to the fact that the film was grown directly on the substrate without a buffer layer. The (110) films had flat, mirror-like surfaces, but the crystallinity and the electrical properties of the interface were not as good as those of (100) films.

In this paper, we report on the growth of $\text{Ca}_{0.5}\text{Sr}_{0.5}\text{F}_2$ on GaAs (100), (111)A, (511)A, (511)B, (711)A and (711)B by molecular beam epitaxy. These interfaces are mismatched by less than 0.4% both at room and growth temperatures. The (100) orientation was investigated because it is the most widely used for GaAs-related devices, and the growth of GaAs in the (100) direction by MBE is very well understood. The optimization of the $\text{Ca}_x\text{Sr}_{1-x}\text{F}_2$ growth along this direction is therefore highly desirable. The growth of CaF_2 on Si(111) has been successful in view of the stability and low energy of the (111) fluoride surface [7]. Smooth surfaces and good crystallinity have been obtained. Finally, the structure of the (m11) high Miller-index surfaces of GaAs (m=5 and 7), which correspond to (100)-vicinal planes, has been investigated. A- and B- (511) and (711) GaAs surfaces prepared by ion sputtering and annealing are stepped [8]. The MBE grown GaAs epitaxial layers on these substrates are also found to be stepped. These orientations have been predicted to allow rapid and defect-free epitaxial growth [9] and been shown to lead to high quality films [10]. (m11) surfaces exhibit (100) terraces on

which nucleation occurs more easily than on the (111) surface, but also have (111) direction risers which contribute to good surface planarity.

EXPERIMENTAL CONSIDERATIONS

The growth of the GaAs buffer layers and of the fluoride films was performed in a molecular beam epitaxy system designed and built at Princeton University. The growth chamber was equipped with effusion cells for CaF_2 , SrF_2 , Ga and As, a 5keV electron gun and phosphorus screen for reflection high energy electron diffraction (RHEED), a residual gas analyzer, an ion gauge flux monitor and a quartz crystal thickness monitor. The growth chamber was connected to a surface analysis chamber equipped with a single-pass cylindrical mirror analyzer for Auger electron spectroscopy (AES), a four-grid low energy electron diffraction (LEED) optics and a 2keV Ar^+ sputtering gun for Auger depth profiling. The samples were introduced through a load-lock chamber equipped with a sample preheating stage and a metallization stage.

The GaAs substrates were Si-doped (n-type) with carrier densities in the range of $1\text{--}2 \times 10^{18}/\text{cm}^3$. The wafers were treated with the following preparation sequence: trichloroethylene, acetone and methanol rinses; hot sulfuric acid and room temperature sulfuric acid baths to remove the residual organic solution; a 5:1:1 solution of sulfuric acid, hydrogen peroxide and water etch for 2 minutes (for (100), (511)A, (511)B, (711)A and (711)B) or 1½ minute (for (111)A). The wafers were immediately rinsed with deionized water for 20 minutes to form a native oxide. Wafers in Mo sample holders were preheated to 150°C in the load-lock, transferred into the growth chamber, and heated to 570°C to desorb the native oxide under arsenic flux. The samples were then heated to 620°C under arsenic flux to obtain more complete surface reconstructions. The starting reconstructions were (2×1) and (2×2) for the (100) and (111) surfaces, respectively. The RHEED pattern for (511) and (711) substrates showed characteristics of stepped surfaces: oblique and discontinuous streaks corresponding to intersections between the reciprocal rods of the stepped structure and the broad reciprocal rods of the short (100) terraces. The patterns of the (m11) surfaces remained unchanged throughout the growth. Then the samples were cooled to the GaAs growth temperature, i.e. 600°C for the (100), 540°C for the (111)A orientations and 580°C for the high Miller index surfaces.

During the growth of GaAs, the As to Ga flux ratio was set at about 1.5. The RHEED intensity oscillations of the specular beam on the (100) substrate had a period of two seconds, indicating a growth rate of about 1Å/sec. During the growth of the GaAs buffer layer, the RHEED patterns were (4×2) for the (100) substrate and (2×2) for the (111) substrate.

The fluoride sources were single crystal chunks with 99.995% purity. Graphite-coated PBN crucibles were used in the fluoride effusion cells to prevent chemical reactions between the fluorides and the PBN. During the growth of the fluorides, the substrate temperature was set at 500°C for the (100) and (m11) films, and 540°C for the (111)A films. The growth rate for the fluorides was ~2Å/sec. The thickness of the GaAs buffer layers was checked with Auger depth profiling and secondary ion mass spectrometry (SIMS), and found to be within 10% of the targeted thickness. The growth rates of the fluoride layers were determined by optical transmission interference fringes and direct profilometry. We also verified the composition of the fluoride films by the AES, Rutherford backscattering (RBS) and SIMS. These measurements indicated a reproducibility of 5% in the Ca to Sr ratio.

Scanning electron microscopy (SEM) with 25keV electrons in the backscattering mode was used to investigate surface morphology and in the electron channeling mode to study surface crystallinity. RBS using 1.8 MeV $^4\text{He}^+$ ions in the random incidence and channeling directions was used to study film stoichiometry and crystallinity. Finally, Raman scattering was used to study the interfacial strain and crystallinity of the GaAs buffer layer using the 514 nm excitation from a Ar^+ laser.

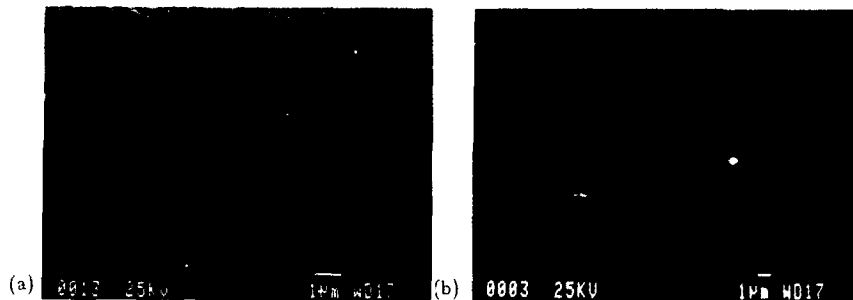


Figure 1: SEM micrographs of (a) 150 Å (b) 3000 Å $\text{Ca}_5\text{Sr}_5\text{F}_2$ grown on GaAs(100)

RESULTS AND DISCUSSION

A. (100) orientation

The (100) GaAs buffer layer is flat, as seen from the long streaks in the RHEED pattern during growth and SEM micrograph of the 1 μm thick GaAs epitaxial layer. The electron channeling pattern (ECP) of this GaAs layer is very sharp and indicates a high degree of crystallinity within a few hundred angstroms of the surface.

The SEM micrograph of a 150 Å $\text{Ca}_5\text{Sr}_5\text{F}_2$ film shows a rough surface with about 20% of the GaAs area uncovered or covered with a thin fluoride layer (Fig. 1a). AES spectra taken on the same surface confirm the inhomogeneity of the film by showing signal coming from the GaAs substrate (1070 eV Ga and 1228 eV As peaks). Macroscopic roughness and discontinuity are not seen in $\text{Ca}_5\text{Sr}_5\text{F}_2$ films with thicknesses greater than 300 Å; presumably fluoride islands have coalesced by this thickness. SEM micrographs show flat, mirror-like surfaces on the scale of 1000 Å (Fig. 1b). No Ga or As signal was detected in the AES spectra, confirming the continuity of the films.

The RHEED pattern of >2000 Å fluoride films show spots characteristic of three-dimensional structure as well as rings corresponding to mosaic-like structure. This suggests that the growth of the fluoride is not two-dimensional and that the surface is composed of different domains. Normal incidence LEED shows a superposition of different patterns characteristic of a surface covered with facets (50-100 Å). The orientation of the facets corresponds to (111) planes. This phenomenon has been investigated at length for CaF_2/Si . The (100) orientation is indeed not the most favorable for the growth of fluoride because the molecular dipole raises the surface free energy [11]. Faceting and formation of low energy (111) surfaces is therefore the manifestation of the instability of the (100) surface. The initial roughness and discontinuous growth of the thin (100) fluoride film (150 Å) is directly related to this problem.

The normal incidence ECP of a 3000 Å $\text{Ca}_5\text{Sr}_5\text{F}_2(100)$ film shows the four broad intersecting lines characteristic of the (100) surface of a cubic structure crystal, and therefore gives clear confirmation of the (100) orientation of the epitaxial film (Fig. 2a). A series of RBS measurements was also done on the 3000 Å thick $\text{CaF}_2(100)$ film. The best χ_{min} , defined as the ratio of the backscattering yield in the channeling to random directions, is 9.9%, indicating fairly good crystallinity. The dependence of χ_{min} on film thickness is still under investigation.

B. (111)A orientation

The growth of GaAs in the (111)A direction is more difficult to refine than in other directions. In particular, the range of substrate temperature for obtaining good buffer layers is quite narrow (530-550 °C). Below this range, the RHEED pattern becomes spotty, indicating non-planar growth. Above this range, (110) faceting occurs, as seen from the V-shape features in the pattern. The surface structure cannot be improved by correcting the temperature once it gets out of the optimal range. Under optimal growth

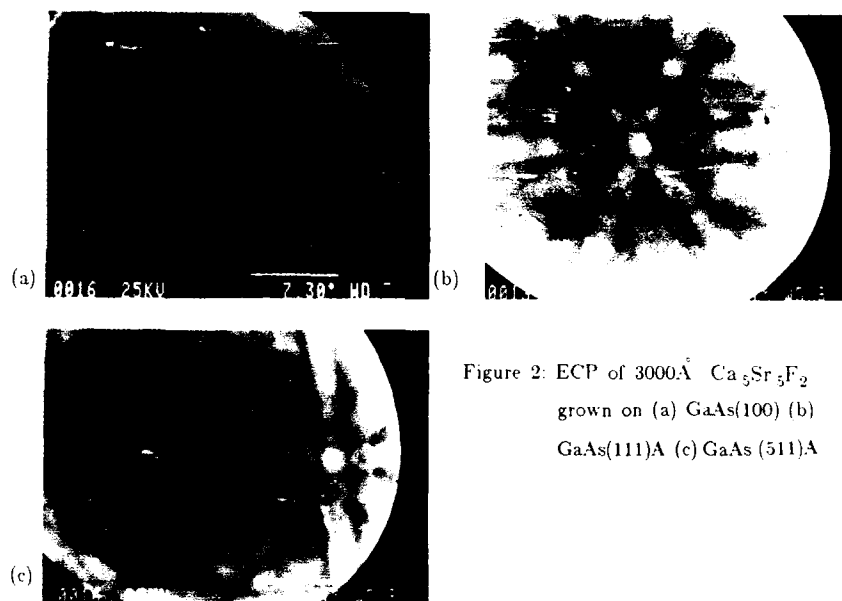


Figure 2: ECP of 3000 Å $\text{Ca}_5\text{Sr}_5\text{F}_2$
grown on (a) GaAs(100) (b)
GaAs(111)A (c) GaAs(511)A

conditions, RHEED shows a (2×2) reconstruction of the GaAs with long streaks suggesting a flat (111) surface. The SEM micrograph also shows a flat surface with a few round defects (density $\sim 5 \times 10^3/\text{cm}^2$). Residual carbon contamination on the substrate surface is probably the origin of these defects. SIMS indicates that about 5% of a monolayer of carbon remains at the interface between the substrate and the buffer layer. The ECP is also very sharp, indicating good surface crystallinity.

Contrary to the (100) case, the SEM micrograph (Fig. 3a) of a 150 Å fluoride film shows very smooth surface morphology, and no substrate signal is found in the AES spectra. The thin (111) $\text{Ca}_5\text{Sr}_5\text{F}_2$ films appear therefore to be flat and continuous. Some round defects, which presumably originate on the (111) GaAs surface, are also detected. The 2000 Å and 3000 Å thick films, however, exhibit rougher surfaces on a scale of a few thousand angstroms (Fig. 3b). The RHEED pattern observed after growth exhibits long streaks superimposed on well defined diffraction spots. This suggests that the (111) fluoride surface is microscopically flat over sizable areas but also contains small areas of roughness presumably associated with the grain boundaries. LEED always shows a clear six-fold symmetric (1×1) pattern with sharp spots, indicating that the surface is microscopically flat within the coherence length of LEED and has the (111) orientation of the substrate. This confirms that the roughness of thicker fluoride films is from the grain-like structure. The orientation and crystallinity of the near-surface region of the film was also confirmed with normal incidence ECP (Fig. 2b). The quality and sharpness of the ECP of (111)A films was in general better than that of (100) films.

The (111) orientation is believed to be the most favorable orientation for the growth of the fluorides due to the low energy of this surface. However, we find that the growth of a high quality (111) GaAs buffer layer is more difficult than for other orientations. These observations suggest therefore that the defect found on (111) fluoride films are inherited from the GaAs buffer layer.

The χ_{min} from RBS for 0.3 μm and 1 μm fluoride films were 19% and 11%, respectively, suggesting that the crystallinity of the $\text{Ca}_5\text{Sr}_5\text{F}_2$ is worse at the interface than in the bulk of the film. In addition, a sample grown at 500 °C produces a considerably worse χ_{min} of 50%, indicating that the optimum growth temperature is higher for the

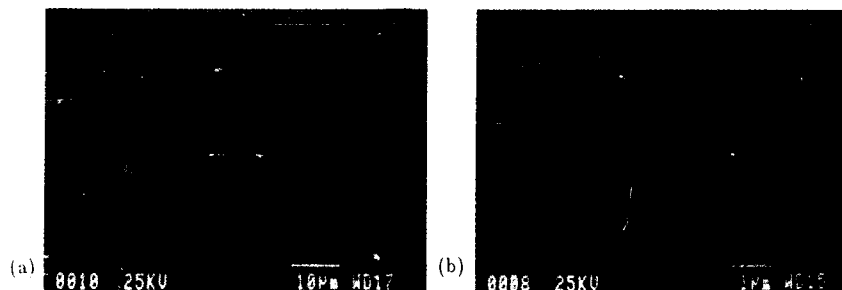


Figure 3: SEM micrographs of (a) 150 Å (b) 3000 Å $\text{Ca}_5\text{Sr}_5\text{F}_2$ grown on GaAs(111)

(111) fluoride film than for the (100) film. This difference in optimum growth temperature on the two semiconductor orientations follows similar observations in the $\text{CaF}_2\text{-Si}$ system [12].

C. (m11) orientation

GaAs (511) and (711) epitaxial layers have been studied; details will be published elsewhere [13]. Combined LEED, RHEED and ECP studies show that A and B (511) and (711) GaAs surfaces prepared by MBE exhibit a regular stepped structure with (100)-terraces and (111)-risers. The χ_{min} along the $\langle 100 \rangle$ channel is 18%, 4%, 16% and 13% for 1800 Å layers on GaAs (511)-A, (511)-B, (711)-A and (711)-B epitaxial layers, respectively. The ECP are very clear on all surfaces. The surface morphology is very flat for (511)-B and (711)-A, and somewhat rougher on (511)-A and (711)-B. We followed the sample preparation and growth procedure for all (m11) surfaces. All the fluoride films on (m11) GaAs substrate had the same thickness of 3000 Å. The SEM micrographs of (511)-B and (711)-A show very flat and mirror-like surfaces while those of (511)-A and (711)-B show a rougher morphology. We believe that this is directly related to the morphology of the GaAs buffer layer.

The RHEED patterns for all (m11) substrates taken after the growth of the fluoride exhibit spots, indicative of three-dimensional structures, and sharp interconnecting lines due to surface facets. The angle between the lines is about 110°, suggesting that the facets again correspond to (111) planes and have the same electrostatic origin as on the (100) surface. The presence of facets is also confirmed with LEED.

The near surface crystallinity of the films is good, as seen from ECP (Fig. 2c). By measuring the angles between the surface normal and the (100) and (111) directions (easily identified through their four-fold and six-fold symmetric ECP's), we have confirmed that the orientation of the fluoride overlayers follow the orientation of GaAs substrate.

The crystallinity of the (m11) fluoride films seems to be strongly related to the crystallinity of the GaAs buffer layer. The χ_{min} obtained from RBS is 54%, 25%, 54% and 45% for (511)-A, (511)-B, (711)-A and (711)-B along the $\langle 100 \rangle$ channel. The consistently better results obtained with the (511)B orientation is clearly correlated with the bulk and surface quality of the GaAs buffer layer. The reason for the higher quality growth along this direction is not understood at this point, but may be related to the microscopic details of the interface bonding. It is clear, however, that the GaAs buffer layer and the GaAs-on- $\text{Ca}_x\text{Sr}_{1-x}\text{F}_2$ layer grow well in this direction [14]. Recent studies indicate, in particular, that the surface of the top GaAs layer recovers the stepped structure characteristic of the (m11) surfaces [14].

SUMMARY

$\text{Ca}_5\text{Sr}_5\text{F}_2$ films have been grown by MBE on GaAs (100), (111)A, (511)A and -B and (711)A and -B substrates. The substrate orientation is preserved in the epitaxial films. The films grown on (100), (111)A and (511)B GaAs exhibit the best crystallinity. (111) faceting occurs on the (100) and (111) fluoride surfaces and causes inhomogeneities in the thin (150Å) (100) films.

ACKNOWLEDGEMENT

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THE EFFECT OF ANNEALING ON THE STRUCTURE OF EPITAXIAL CaF_2 FILMS ON Si(100)

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ABSTRACT

We have studied the effect of different annealing conditions on the crystallinity and morphology of 1000Å epitaxial CaF_2 films on Si(100). The crystallinity of the films is improved by the anneals, with the highest anneal temperatures giving the greatest improvement. The results are consistent with the model previously proposed to explain the success of rapid thermal annealing in improving thicker epitaxial CaF_2 films.

I. INTRODUCTION

Research into the growth of epitaxial insulators, especially CaF_2 on Si has been a fertile area of investigation for both fundamental and technological reasons.¹ While there have been a number of demonstrations of the potential utility of CaF_2 /Si structures, there remain problems associated with obtaining optimal CaF_2 layers on Si(100) surfaces. The epitaxial quality of CaF_2 films deposited on Si(100) by molecular beam epitaxy (MBE) is a sharply peaked function of the substrate temperature during deposition.² Even the best as-deposited films contain misoriented CaF_2 (111) crystallites and have a very rough morphology, which has been explained by the high energy of the CaF_2 (100) surface.³ A rapid thermal anneal (RTA) can be used to improve the epitaxial quality of CaF_2 films greater than 3000Å thick grown on Si(100).⁴ Using RTA it is possible to create films with superior crystallinity, smooth morphology, and few or no misoriented grains. It has been hypothesized that the driving force for the regrowth which leads to the improvement of these and other epitaxial layers is the minimization of the surface energy density in the films, both that associated with the substrate-overlayer interface and that associated with grain boundaries.

In the present work, we have studied the effect of different (non-rapid) annealing conditions on the crystallinity and morphology of 1000Å epitaxial CaF_2 films on Si(100) substrates. Films of this thickness have not been amenable to improvement by RTA because the high temperature of the RTA process leads to their evaporation. We find a systematic dependence of the film quality on the annealing temperature. The results are consistent with the model previously proposed to explain the RTA results.

II. EXPERIMENTAL PROCEDURE

All of the films were produced in an MBE system having a base pressure of $\leq 10^{-10}$ Torr. Si substrates were cleaned as described previously.⁵ CaF_2 was evaporated from a graphite crucible in a Knudsen effusion cell operating at about 1200°C. The substrate temperature was maintained at 500°C during the growth of the ~1000Å films. Immediately after growth, the temperature of the substrate was adjusted to the desired annealing temperature between 400 and 850°C. All anneals lasted 30 minutes except those at 400°C which were for 90 minutes. The films were examined using Rutherford backscattering/channeling (RBS), plan view and cross sectional transmission electron microscopy (TEM), and scanning electron microscopy (SEM).

III. RESULTS

The crystallinity of 1000Å CaF_2 films on Si(100) is improved by anneals after growth with the highest anneal temperatures giving the greatest improvement. Figure 1 shows the dependence of χ_{min} (the ratio of the backscattered high energy $^4\text{He}^+$ ion yield in the aligned $\pm 100^\circ$ direction to a random direction) on the annealing conditions. The χ_{min} of an unannealed film is $\sim 27\%$, indicating that, while epitaxial, the film contains many defects. A 90 minute anneal at 400°C appears to have little if any effect on the crystallinity. In contrast, 30 minute anneals at temperatures between 500 and 850°C have a large impact on the χ_{min} , with the lowest measured value of 7% being observed in films annealed above 800°C .

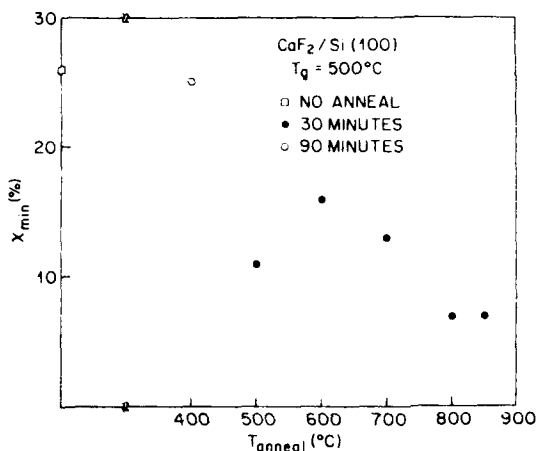


Figure 1. Dependence of χ_{min} on the annealing temperature. All films were grown at 500°C . All anneals were for 30 minutes, except those at 400°C , which were for 90 minutes.

The nature of the changes in crystallinity brought about by the anneals is elucidated by studying diffraction patterns from the films. Figure 2 shows transmission electron diffraction (TED) patterns from three films. The as deposited film (Fig. 2a) shows diffraction rings from misoriented CaF_2 . The rings have disappeared after an anneal at 400°C (Fig. 2b), although selected area diffraction on small grain-like structures in the film shows that there is still a small amount of misoriented material. It is noteworthy that TED shows the 400°C annealed film to contain considerably less non-epitaxial material than the as deposited film, even though both have nearly the same χ_{min} . χ_{min} is very sensitive to slight mosaic spread and low angle grain boundaries which TED may not detect. After an 850°C anneal (Fig. 2c) there is no indication in the diffraction pattern for misoriented CaF_2 . The diffraction patterns of all films annealed at 500°C and above show diffraction patterns similar to that shown in Fig. 2c.

Figure 3 shows plan view TEM micrographs of the same three CaF_2 films. Although most of the as deposited film (Fig. 3a and b) is epitaxial, it contains many sharply faceted misoriented grains which have random in-plane orientation. The symmetry of many of these grains as well as a strong 220 ring in the diffraction pattern in Fig. 2 suggests that many of them have (111) texture. The 111 ring in the diffraction pattern in Fig. 2 is, however, not allowed for this orientation, indicating that some of the grains have other orientations, perhaps (110) or (112). After annealing at 400°C (Fig. 3c and d), most of the misoriented grains have disappeared. Those that remain are smaller and less numerous than in the as deposited films, as well as being less faceted. The film annealed at 850°C (Fig. 3e and f) contains few, if any, misoriented grains. Cracks have developed in the film, however,

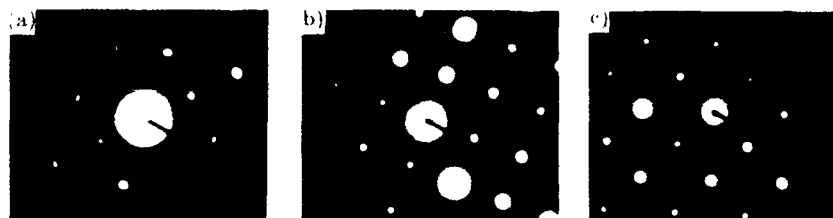


Figure 2. Plan view selected area transmission electron diffraction patterns of CaF_2 films on Si(100): (a) as deposited; (b) after annealing 90 minutes at 400°C ; (c) after annealing 30 minutes at 850°C .

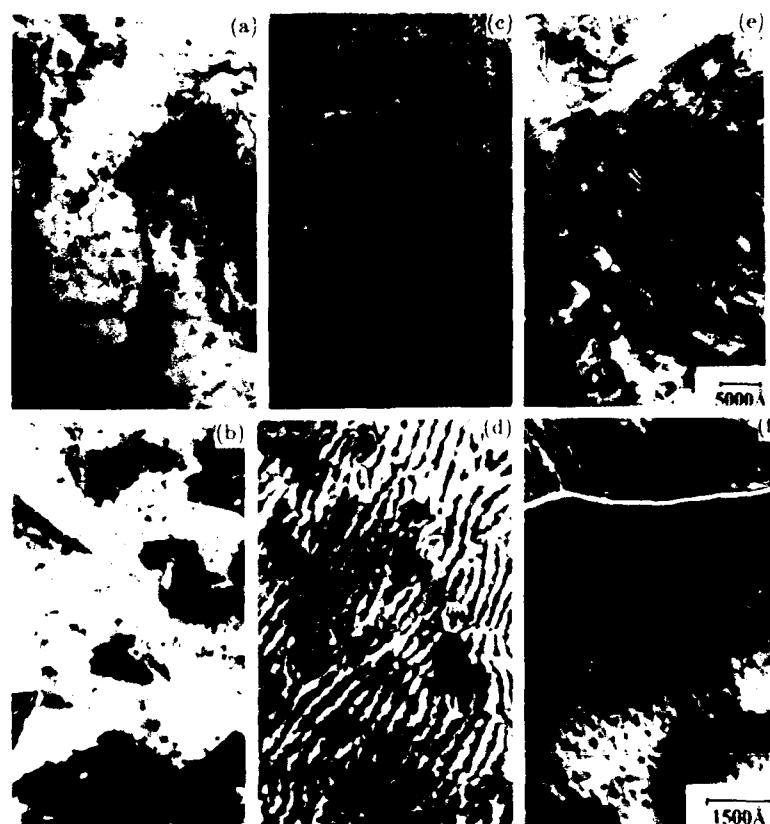


Figure 3. Plan view TEM micrographs of CaF_2 films on Si(100): (a) and (b) as deposited; (c) and (d) after annealing at 400°C for 90 minutes; (e) and (f) after 30 minutes at 850°C .

presumably due to the high thermal mismatch between CaF_2 and Si. Cracks are seen in all of the annealed films; they appear to become wider as the anneal temperature increases.

SEM micrographs of the same three CaF_2 films are shown in Figure 4. The surface morphology of the as deposited film (Fig. 4a) is rough and shows sharp facets, as previously reported for thicker films.³ At 400°C (Fig. 4b) the roughness has decreased, and the large faceted areas have become smaller and more rounded. By 850°C the film is quite smooth, except for the cracks mentioned above, one of which bisects the micrograph in Fig. 4c.

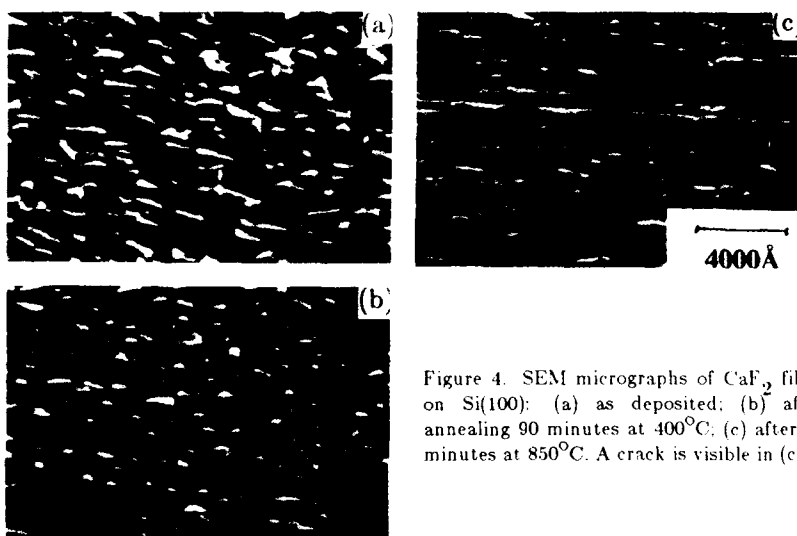


Figure 4. SEM micrographs of CaF_2 films on Si(100): (a) as deposited; (b) after annealing 90 minutes at 400°C; (c) after 30 minutes at 850°C. A crack is visible in (c).

Figure 5 shows cross sectional TEM images of the same three CaF_2 films. The faceting of the as deposited surface (Fig. 5a) is clear. The pyramidal shape of the facets is consistent with (111) faceting as proposed earlier.⁶ After annealing at 400°C (Fig. 5b), the surface is much smoother with some irregularities and cracks. After annealing at 850°C (Fig. 5c), the surface is very flat, with frequent cracks. There is no evidence for interfacial reactions of the type seen in some CaF_2 films which have undergone RTA,⁶ although a smaller degree of substrate-overlayer interaction cannot be ruled out on the basis of the current data.

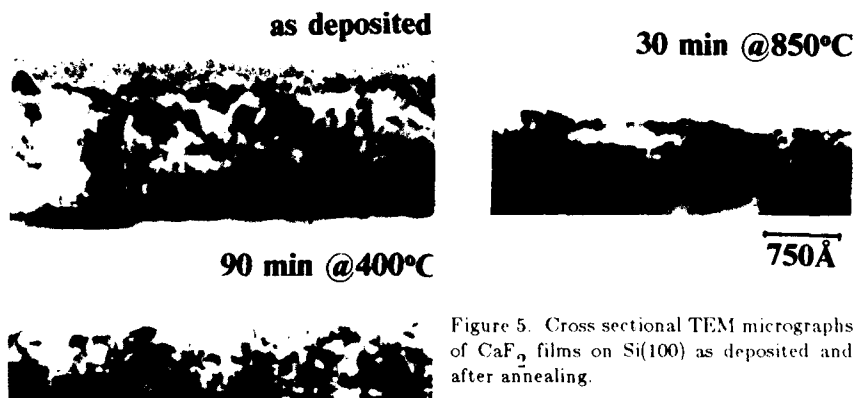


Figure 5. Cross sectional TEM micrographs of CaF_2 films on Si(100) as deposited and after annealing.

IV. DISCUSSION

Anneals at all temperatures between 400°C and 850°C improve the epitaxial quality of 1000Å CaF_2 layers deposited on Si(100) at 500°C. The nature of this improvement is the removal of misoriented grains in the film itself and the smoothing of the film surface. Anneals performed under the conditions studied here also introduce cracks into the films. These changes are visible in all of the annealed films which have been studied, although the changes are more dramatic in those annealed at the highest temperatures. The nature of these modifications is the same as has been seen in thicker CaF_2 films on Si(100) which have been RTA-ed.⁴ In the RTA case, however, film cracking was eliminated by the introduction of thermal soaks to the annealing cycle.⁵ It is likely that such soaks may eliminate the cracking problem here, as well.

While the origin of the misoriented grains is not clear, it may arise from the large difference between the energies of the (100) and (111) surfaces of CaF_2 which, in the absence of other constraints, tends to lead to preferential orientation of the CaF_2 (111) direction perpendicular to the growth surface. As long as the misoriented grains compose a relatively small fraction of the film, their annihilation during annealing is driven by the energy of the grain boundary between the misoriented grain and the generally epitaxial film.

The initial faceting of the CaF_2 surface probably also arises from the large difference between the (100) and (111) surface energies. The smoothing which occurs during growth, however, can be explained by surface diffusion. The lowest temperature at which these anneals occur is ~ 0.4 times the melting temperature of CaF_2 , well above the temperature which is expected to give sufficient surface mobility to allow for smooth growth of this material.⁷ The smoothing is not likely to be due to evaporation of the top of the film, since a significant amount of smoothing is seen at only 400°C, some 800°C below the temperature at which CaF_2 is evaporated from an effusion cell.

V. CONCLUSIONS

Annealing of 1000Å CaF_2 films on Si(100) in ultra high vacuum for 30-90 minutes is effective in improving their crystallinity and morphology. The greatest improvement is seen in films annealed at temperatures above 800°C. The improvement in crystallinity is due to the elimination of misoriented material and is driven by the minimization of grain boundary energy. The morphological improvement is most likely due to the high surface diffusivity of CaF_2 during the anneal. Cracks in the film which arise during annealing are due to the large thermal mismatch between the substrate and overlayer. For thicker films which have undergone RTA, cracking has been eliminated by the use of thermal soaks. Similar modification of the annealing cycle in the present case should also lead to crack elimination.

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The Adsorption of Gallium on the Cleaved Surface of InP, InAs and InSb

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Studies of chemical trends may provide additional insights in complicated reactions between adsorbates and substrates. Here, the interaction of gallium with InP, InAs and InSb cleaved surfaces was investigated by using photoemission spectroscopy (UPS).

Ga was evaporated from a Knudsen-type cell which was placed at a distance of approximately 15 cm in front of the surfaces cleaved in situ. After the evaporation rate, which was monitored by using a quartz oscillator, had stabilized the amount of Ga deposited was determined from the exposure time. The film thicknesses given in Å are nominal values since Ga was found to exhibit island growth. The energy distribution curves (EDC-s) of the photoemitted electrons, which were excited by HeI and HeII radiation provided by a home-built discharge lamp, were recorded by using a single or a double-pass cylindrical mirror analyzer.

As an example, Fig.1 shows the valence-band emission as a function of the amount of Ga deposited on InAs. No dramatic changes are observed up to 15 Å of Ga while above that value additional intensity builds up in the energy range between the valence-band maximum and the Fermi level E_F . Since a well-developed Fermi edge is eventually detected while, on the other hand, even for 60 Å of Ga deposited features of the InAs valence-band are still discernible metallic islands are obviously present which finally coalesce after 120 Å of Ga were evaporated.

Similar conclusions are reached for Ga:InP while Ga:InSb behaves somewhat differently. The EDC-s of photoemitted electrons shown in Fig.2 are again indicating island growth but they are revealing no sharp Fermi edge which, on the other hand, was clearly observed with Ga on InAs (Fig.1), InP as well as with other III-V compound semiconductors [1,2]. With Ga:InSb the intensity is rather decaying to zero towards the Fermi level. Two features A and B approximately 3.5 and 1.8 eV below E_F , respectively, are found to develop with increasing Ga coverage. In analogy to what was reported for Sb:GaAs [3] and Ga:GaSb [4], structure B is assigned to free antimony on the growing metal film. Line A, on the other hand, seem to indicate the presence of antimony

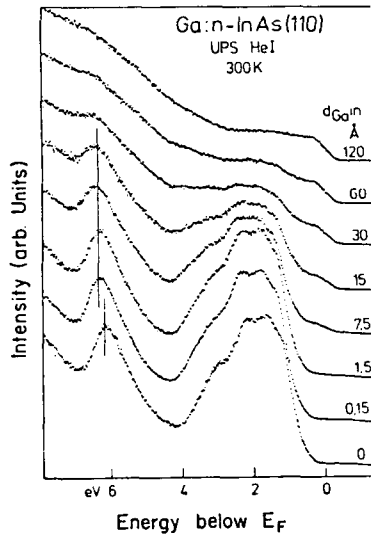


Fig.1: Valence band photoemission spectra for increasing Ga coverage on InAs. The full line linking the spectra around 6 eV below E_F indicates that the band bending is already completed at coverages equivalent to 0.1 ML (1 ML = 7.71×10^{14} atoms/cm² for InAs (110) at 300 K)

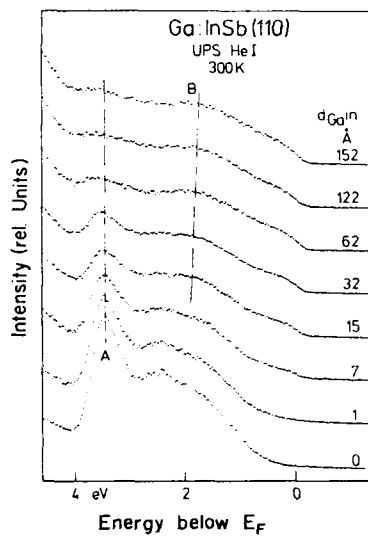


Fig.2: Valence band photoemission spectra for increasing Ga coverage on InSb. Note the absence of the Fermi edge in the spectra for high Ga coverage.

being bound in a ternary compound such as InGaSb.

The absence of a Fermi edge and of Ga-MVV auger electrons in the EDC-s shown in Fig.2 may be understood by following the development of photoemission from the In(4d) core levels which is shown in Fig.3. A doublet A-B is observed to grow on the

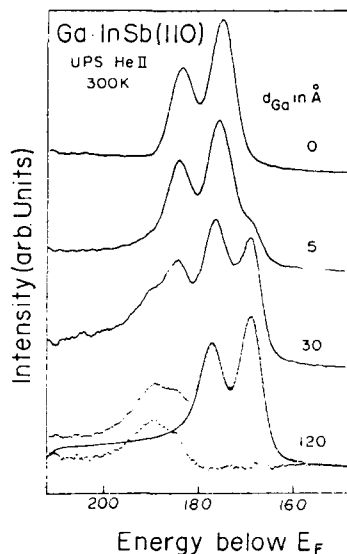


Fig.3: Shallow core level spectra for increasing Ga coverage on InSb. In the spectrum for 120 Å the experimental data are shown in dots. A set of two D-S shaped curves could fit the low binding energy side of the data with a s-o splitting of 0.85 eV, branching ratio = 0.66 eV, $\Gamma_L = 0.1$ eV, $\Gamma_G = 0.4$ eV, D-S asymmetry = 0.15 and an integral background. The difference spectrum is showed at the bottom of the curve. See the text.

low-energy side of the In(4d) doublet recorded with the clean surface and finally to dominate the whole spectrum. This new doublet exhibits the In(4d) spacing (0.85 eV), it may be fitted by a Doniach-Sunjić line shape which is characteristic for metals, and it is thus indicating the presence of metallic indium which originates from a cation exchange with evaporated Ga. The fit of the In(4d) lines shown after the deposition of 120 Å of Ga was achieved with an asymmetry of 0.15, branching ratio equal to 0.66 and a Lorentz width of 0.1 eV convoluted with a Gaussian exhibiting a FWHM of 0.4 eV which is the experimentally determined resolution of the system. A smooth background was considered in the fit but no additional components had to be included in the fitting routine. The difference spectrum shown at the bottom of the Fig.3 reveals a broadened Ga(3d) signal. This finding supports more than one chemical configuration for Ga. Taking into account the ratio of the ionization cross-sections $\sigma_{In}/\sigma_{Ga} = 3$ at $h\nu = 40.8$ eV [4], the lower curves in Fig.3 give an intensity ratio In(4d)/Ga(3d) = 0.7. The incoming Ga has thus exchanged sites with In to a large extent by forming GaSb at the interface. The absence of a well-developed Fermi edge in Fig.2 may be explained by considering that at $h\nu = 21.2$ eV the excitation cross-section of Sb(5p) electrons is by a factor of approximately

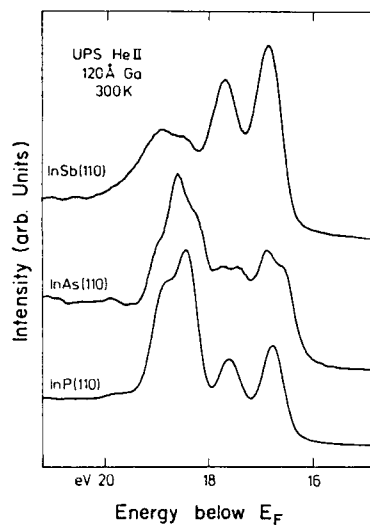


Fig.4: Shallow core level spectra for 120 Å Ga on InSb, InAs and InP. The spectrum for Ga:InAs shows at least two chemical states for In and Ga. The spectrum for Ga:InSb is analyzed in the figure 3.

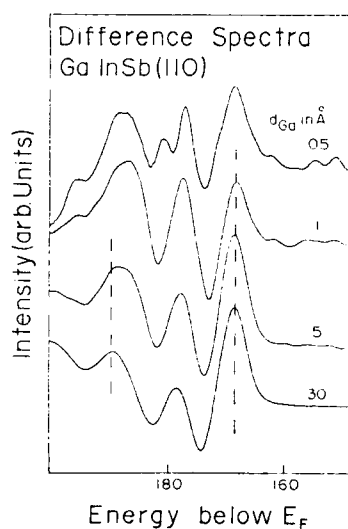


Fig.5: Difference spectra for Ga:InSb. The structure at 16.8 eV shows the presence of metallic In. The structure around 18.8 eV is related to Ga(3d) core level and the changing of its maximum position indicates different chemical states for Ga with increasing coverage.

400 larger than those for Ga as well as In valence-electrons [5].

Fig.4 shows photoelectron EDC-s of Ga(3d) and In(4d) core levels recorded by using HeII radiation after the deposition of 120 Å of Ga on InP, InAs, and InSb. The differences between the spectra are striking. With InP, metallic Ga and In are observed, which is in agreement with earlier findings [2], while on InAs both Ga and In are present in two chemically different states at least. The energetic positions of the maxima in the spectrum seem to indicate the presence of metallic Ga and In as well as of a ternary compound such as InGaAs.

With Ga on InP and InAs cation-exchange reactions were already reported earlier [2,4,6]. While those systems are somewhat difficult to analyse by using UPS the difference spectra shown in Fig.5 are revealing details on the reactivity at Ga-InSb interfaces. The broad line centered at approximately 18.8 eV below the E_F results from Ga(3d) core-level emission. Its centroid shifts from 18.66 to 18.84 eV below E_F or, with other words, the Ga(3d) binding energy becomes larger when the Ga coverage is increased from 0.5 to 30 Å. The presence of the In(4d_{5/2}) peak at 16.8 eV below E_F , which is characteristic for metallic In, confirms a cation exchange to take place. Therefore, the Ga(3d) signal peaking at 18.66 eV below E_F is assigned to a thin epitaxial layer of GaSb. At larger coverages, the disruption of more substrate bonds most possibly causes disorder to occur at the interface which conclusion is supported by the ill-defined features in the valence-band spectra shown in Fig.2.

In Table 1, intensity ratios of the In(4d) and the Ga(3d) core-level lines are compared with some thermodynamic data which are the formation energies of the respective In-V and Ga-V compounds and the heat of solution for In in Ga. The heats of reaction for the formation of Ga-V compounds by cation exchange, which may be approximated by the difference of the heats of formation of the compounds involved, are indeed supporting the experimental finding of cation exchange up to a monolayer coverage. The experimental intensity ratios In(4d)/Ga(3d) are scaling with the ratio of the heat of condensation of Ga (-68.3 Kcal/mole [9]) and the heat of formation of the respective Ga-V compounds. This finding confirms the conclusion that for larger amounts of Ga deposited more substrate bonds become disrupted resulting in disorder at the interface.

Table 1: $\Delta H_f^O(A-B)$ is the formation enthalpy for the compound A-B [7,8,9], $\Delta H_{sol}(A-B)$ [4] is the heat of solution of A in B, ΔH_R^N is the normalized interface enthalpy [4] and ΔH_{con} is the energy of condensation of Ga [9].

Ga:In-V	$\Delta H_f^O(In-V)$	$\Delta H_f^O(Ga-V)$	$\Delta H_{sol}(Ga:In)$	ΔH_R^N	$\frac{In4d}{Ga3d}$	$\frac{\Delta H_{con}}{\Delta H_f^O(Ga-V)}$
	(Kcal/mol)					
InP	-22.4	-29.0	+0.06	-6.6	0.6	2.4
InAs	-13.8	-17.0	+0.06	-3.2	0.3	4.0
InSb	-7.4	-10.0	+0.06	-2.6	0.7	6.8

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PART V

Heteroepitaxy on Silicon I

METHODS TO DECREASE DEFECT DENSITY IN GaAs/Si HETEROEPITAXY

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ABSTRACT

In this paper, the fundamental mechanisms of procedures improving the structural quality of GaAs grown on Si are discussed. Patterned growth, strained layer superlattices and proper thermal cycling are promising approaches to achieve a high quality of GaAs layers grown on Si substrates.

INTRODUCTION

Recent developments in the field of GaAs/Si heteroepitaxy have been spurred [1] by the possibility of combining high-speed GaAs material with well-established Si technology, thus gaining better thermal conductivity, higher fracture toughness, smaller weight and larger diameters wafers offering the possibility for integration of optoelectronic and digital devices. Unfortunately, many problems are encountered in growth of GaAs on Si, such as growth of polar crystal on nonpolar substrate, lattice mismatch of 4.1%, and a considerable difference in thermal expansion coefficient between epilayer and substrate. As a consequence of these problems, the quality of GaAs epilayers on Si substrates is very poor. This is evidenced clearly by the width of the X-ray rocking curve, which is typically more than an order of magnitude broader than in GaAs/GaAs homoepitaxy [2]. The dominant defects in the GaAs epilayer are misfit dislocations formed at the interface with Si, stacking faults, microtwins and threading dislocations which propagate through the epilayer.

ORIGIN OF DEFECTS IN THE EPILAYER

Interfacial Contamination

In addition to the problems caused by lattice and thermal mismatch, one of the most important origins of defect formation in the epilayer are irregularities and residual contamination at the interface (Figs. 1 a, b). Protrusions such as shown in this figure clearly originate at oxide or carbide contaminants at the substrate. Many of them can be avoided by proper cleaning. The most commonly used method for preparation of the Si substrate is the Ishizaka method [3]. However, after such cleaning islands of impurities can still be observed [4]. Cross sectional transmission electron microscopy (TEM) shows typically a white band at the interface between the GaAs and Si, which has frequently been attributed to artifacts of the TEM sample preparation. Our own investigation of metal/GaAs heterostructures deposited in-situ in ultra high vacuum did not reveal such a white band. Only air-exposed surfaces showed such a white band at the interface [5,6]. In GaAs/Si heteroepitaxy formation of this white contrast does not occur after application of a Ga reduction process as suggested by Kroemer [7,8], confirming that in most cases this white contrast is indicative of contamination at the hetero-interface.

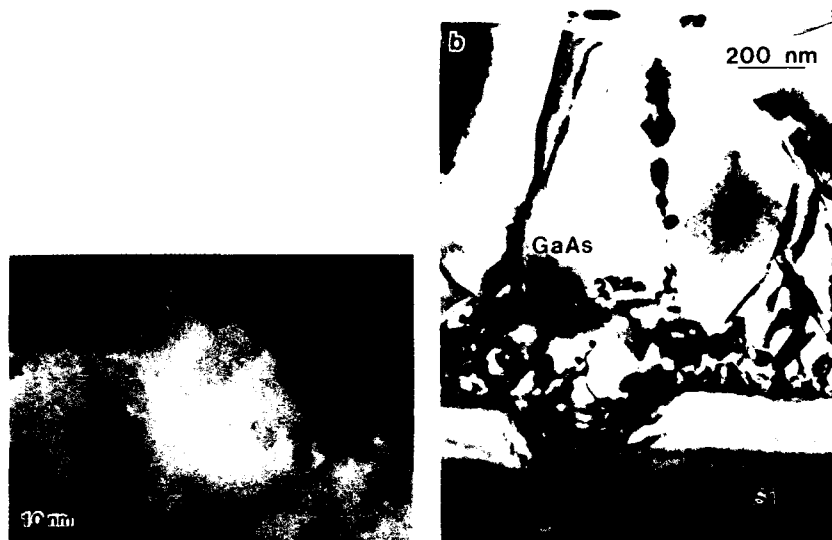


Fig. 1: TEM micrographs of GaAs grown on: a) (211) Si surface, b) (100) Si surface. Protrusions with oxygen and carbon contamination were found on both surfaces. Such contamination are additional sources for dislocations and stacking faults formation as indicated on these micrographs.

Island Nucleation

Initial growth of GaAs on Si is often observed to start from islands [9-11]. Coalescence of the islands can result in the formation of additional defects. Islands with small lateral dimensions are strained and free of dislocations. The thickness of such islands can easily exceed the critical thickness as e.g. calculated by Matthews and Blakeslee [12]. Upon increasing lateral dimensions of the islands, misfit dislocations become visible at the interface. One possible mechanism for misfit dislocation formation for large islands is the glide of half loops from the island surface to the interface. Such half loops generate misfit dislocations at the interface which relieve interfacial strain. The "arms" of such half loops form threading dislocations in the epilayer. Two types of misfit dislocations were detected at GaAs/Si (100) heterointerfaces: 90° dislocations with Burgers vector parallel to the interface which are sessile (Lomer type), and glissile 60° dislocations with Burgers vector inclined to the interface. These dislocations relieve a smaller amount of stress compared to Lomer-type dislocations [13]. Therefore a higher density of these dislocations is required to relieve the same stress. Moreover, the 60° dislocations can glide back into the epilayer, which makes them less desirable.

Polar on non-polar growth

Polar on non-polar growth is connected with the appearance of antiphase domains (APDs). Their appearance is most probably due to the presence of single steps at the Si surface and the preferred bonding of As with Si. The presence of single steps was observed by using many surface sensitive techniques [14] and it was confirmed by cross-sectional TEM using the Atomic

Resolution Microscope in Berkeley with a point-to-point resolution of 1.7 Å [15]. APDs can be detected by chemical etching of the surface [16] or by TEM using the convergent beam technique [17, 18] or dark field imaging for 200 and -200 reflection [19]. The dark field imaging technique allows to detect *differences* in polarity, but the convergent beam technique can be used to determine directly the polarity of even a single domain on a microscale [17].

Such APDs are three-dimensional islands and the boundaries (APBs) between these islands can be formed on low index as well as on high index planes. Our own observations show that very often such boundaries macroscopically appear to be formed on various planes (Fig. 2), such as for example on {111} planes, although microscopically they consist of terraces of {110} APBs [18]. Formation of APBs on {110} planes would confirm Petroff's prediction that {110} and {112} APBs with alternating As-As and Ga-Ga bonds have the lowest energy of formation [20].

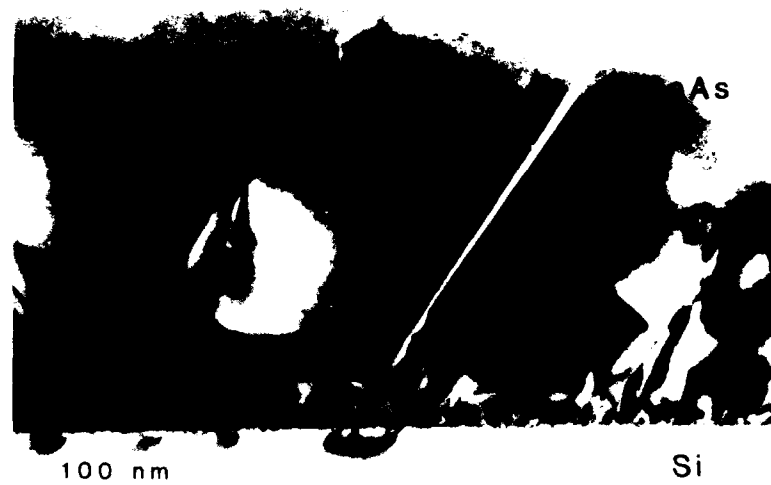


Fig. 2: TEM micrograph of GaAs grown on (100) Si showing an antiphase boundary, as confirmed by CBED analysis [18]. The antiphase boundary is composed of small facets along {110} planes (edge-on or inclined) which, when viewed as a whole, appears to be parallel to the {111} microtwin planes shown on this micrograph.

It has been reported that misorientation from the nominal (100) orientation by rotation of 2°-4° about the [011] direction leads to the disappearance of antiphase boundaries [21-23]. Our own observations show that even for such misoriented substrates antiphase domains can be found if the growth conditions are not optimized, preferentially in the areas close to the interface [24]. Many of these domains terminate inside the epilayer so that only a small number of APBs extend to the surface. Drastic changes of the APD density are observed upon changing the growth parameters. After post-growth annealing APD free layers even on nominal (100) substrates were found [16]. The growth of APD free GaAs is an essential achievement in GaAs heteroepitaxy, reached within the last two years.

Different Thermal Expansion Coefficients

Photoluminescence studies have shown that tensile strain is present in GaAs grown on Si, rather than compressive strain as expected from the lattice mismatch between GaAs (5.653 Å) and Si (5.431 Å). We found that the number of misfit dislocations is related to the stress relief at the growth temperature and this number is too high for room temperature [25]. The difference in thermal expansion coefficient ($\alpha_{\text{GaAs}} = 6.8 \times 10^{-6}/^\circ\text{C}$, $\alpha_{\text{Si}} = 2.6 \times 10^{-6}/^\circ\text{C}$) produces new strain during cooling from the growth temperature opposing the lattice mismatch strain [26]. The tensile strain observed experimentally is considerably lower than the expected value 2.4×10^{-3} , indicating strain relief by plastic flow. Cooling from 600°C to only 400°C is sufficient to generate a biaxial tensile stress far above the experimentally determined critical resolved shear stress of 15 MPa at 400°C [27], which will result in the glide of additional threading dislocations of various types from the interface into the epilayer. In addition, misfit dislocations at the interface can be forced to dissociate on a {111} plane inclined to the interface, leaving one partial dislocation at the interface and forming an extended stacking fault. The formation of extended stacking faults by glide processes was first found in plastically deformed semiconductors cooled under high stress [28,29]. An alternative explanation of formation of such planar defects can be their nucleation at the initial stage of growth for strain relief [30].

HOW TO DECREASE DEFECT DENSITY?

Conventional two-step growth

A very successful method for the growth of GaAs on Si is two-step growth in which an initial buffer layer ~100-300 Å thick is grown at low temperature (~400°C), and then at ~650°C to continue growth. The dislocation density decreases with layer thickness due to the interaction and annihilation of dislocations. Pearton et al. [31] showed directly by X-ray rocking curve analysis the increase of crystalline quality with GaAs layer thickness. However, with increasing layer thickness new problems occur with cracking, wafer bowing and decreased energy dissipation through a thick GaAs layer during device operation, which limits the thickness of useful GaAs/Si to 2-3 μm.

Two-dimensional Initial Growth

GaAs generally starts to grow on Si in the form of islands [9]. Several reasons might lead to such three-dimensional growth. Island formation may be connected with strain due to lattice mismatch, surface tension of the epilayer, preferred growth at surface steps or growth only in areas free of impurities. Coalescence of such islands is very often connected with formation of additional defects such as dislocations and antiphase boundaries. It was shown that even in the case of GaP grown on Si where mismatch is much smaller than between GaAs and Si three-dimensional growth occurs [32,33].

One promising method is to start with a lattice-mismatched system such as AlGaP which provides very good wetting of the substrate. Umeno's group reported first the role of Al during growth of GaP on Si [32, 33]. The addition of small amounts of Al causes perfect two-dimensional growth (Fig. 3). This might be due to the high affinity of Al for oxide formation, allowing to grow Al compounds on clean and contaminated surfaces [32].

Another very promising method is migration-enhanced epitaxy in which the Ga and As flux is alternating [34] or modulation enhanced epitaxy with continuous As flux and intermittent Ga flux [35]. It was demonstrated that this kind of growth ensures two dimensional growth and results in very narrow PL lines.



Fig. 3: High resolution image of the AlGaP/Si interface showing perfect two dimensional growth by adding of Al to GaP (in contrast to three dimensional growth of GaP on Si).

Post-Annealing

a) Furnace Annealing

If the heteroepitaxial layer is grown strain-free with the correct density of misfit dislocations at the interface, any change of temperature will induce strain, the sign and magnitude of which depends on the difference between growth temperature and annealing. Thus it is possible to move dislocations by thermal cycling during or after the growth. It was reported that annealing at 850°C under arsenic overpressure results in dislocation rearrangement at the interface forming a majority of Lomer type dislocations and decreasing the number of stacking faults [36, 37]. Our own observations do not confirm these results fully. Furnace annealing at 800°C for 10 min changed only slightly the defect rearrangement [Fig. 4]. The dislocation density remains in the same range as for "as-grown samples" but they are more tangled. A slight decrease in stacking fault density was observed. This discrepancy can indicate a strong dependence on the detailed annealing conditions, requiring careful optimization.



Fig. 4: TEM micrograph of GaAs/Si (100) after furnace annealing.

b) Rapid Thermal Annealing

Noticeable improvements in the quality of GaAs/Si epilayers grown by MBE were observed after rapid thermal annealing (RTA) at 800°C for 10 sec by the capless close-proximity method in a commercial heatpulse furnace. The density of stacking faults after this treatment was very low [Fig. 5], possibly because of the different cooling rate compared to furnace annealing. Partial dislocations which were mobilized during annealing and could glide back to the interface to recombine with the second partial. During rapid cooling they were "frozen" in this state and did not dissociate again into partials. This mechanism is beneficial for the removal of stacking faults, but

prohibits stress relief during cooling down, and this is evidenced by cracking of the GaAs epilayers which experienced RTA. Cracking was even more severe than in as-grown samples. The heterointerface is observed to be more undulated after RTA, compared to as-deposited samples. Independent electrical measurements of devices after RTA [38] showed noticeable improvement for forward and reverse bias characteristics. Leakage currents were reduced by more than two orders of magnitude after this treatment.

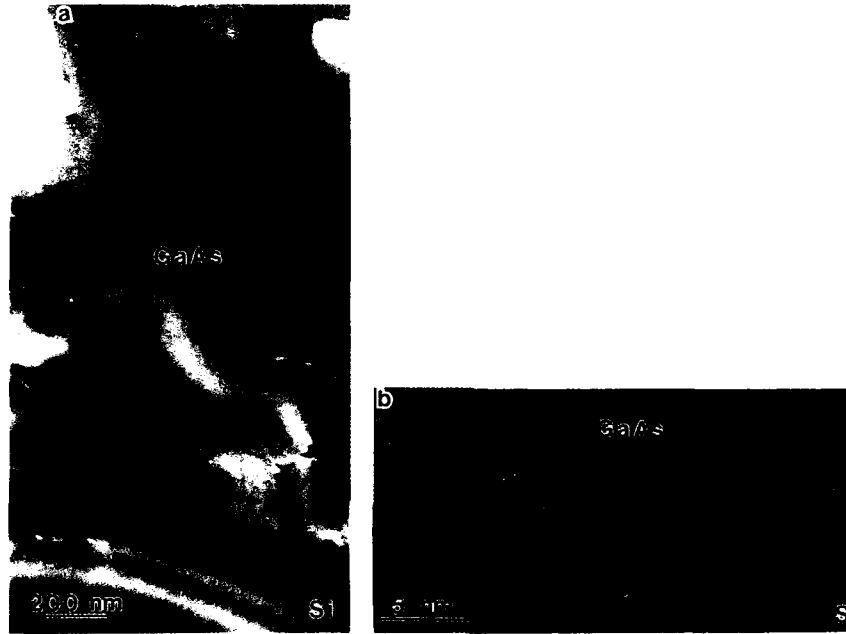


Fig. 5: a) TEM micrograph of the GaAs/Si (100) interface after RTA annealing.

b) High resolution image of the GaAs/Si interface showing ondulation of the interface after RTA and complete elimination of the stacking faults.

c) In-situ Annealing

It was reported that in-situ annealing at 800°C for 5 min. during growth is more efficient in defect reduction than ex-situ annealing [39]. This causes visible dislocation bending, providing a better chance for threading dislocations to interact and, ideally, to move to the periphery of the wafer. After this treatment the density of dislocations was reduced to $2 \times 10^{-7}/\text{cm}^2$ [39].

Yamaguchi et al. [40, 41] carried out an even more successful thermal treatment during MOCVD growth. It involved thermal cycling during growth in which annihilation and coalescence of dislocations were caused by dislocation movement under the alternating thermal stress. The growth of the GaAs was interrupted several times, and the substrate temperature was lowered to room temperature, followed by a temperature increase up to 900°C and subsequent annealing for up to 15 min at this temperature in an arsine atmosphere. After this treatment, the substrate temperature was again lowered to 700°C and a new layer of GaAs was grown in the same fashion. This process was repeated several times. The reported dislocation density for GaAs grown on Si

with such thermal cycling was estimated from the etch pit density to be as low as $1-2 \times 10^6/\text{cm}^2$. Such thermal cycling during growth appears to be a very promising approach for decreasing the defect density in the heterolayer.

Patterned Growth

The goal to grow a lattice mismatched heteroepilayer with a network of misfit dislocations confined to the interface and no threading dislocations in the epilayer is difficult to achieve for a homogeneous 3" wafer. It would require glide of the threading "arms" of misfit dislocations across the whole wafer without being blocked by other threading dislocations. However, it appears to be much easier to achieve this goal if the growth area is confined to a small part of the substrate, e.g. by patterning lines or mesas on the substrate.

One example of such patterned growth is the growth of GaAs on Si through openings in an oxide or nitride [42-44]. Our own results [45] show that GaAs grown above the SiN mask was polycrystalline, but in the open areas where the nitride was removed monocrystalline GaAs was detected with much lower dislocation density than in typical two step growth [Fig. 6]. The stacking fault density was much lower in the entire pattern, increasing only at the border with nitride. This decrease in defect density is probably connected with the stress release at the periphery of patterns in polycrystalline areas. Post-growth annealing at 850°C in arsenic overpressure results in significant grain growth in the remaining polycrystalline GaAs overgrown on the amorphous areas such as oxides or nitrides, and elimination of the defects at the transition region from polycrystalline to single crystal growth. An increase of Hall mobility of 30% was observed in these annealed samples. Fitzgerald et al. proposed patterned growth by growing a lattice mismatched $\text{In}_{0.05}\text{Ga}_{0.95}\text{As}$ layer on free standing mesa structures of GaAs (2 μm high with 60nm diameters and larger). Only misfit dislocations were observed in these structures. The epi-layer was dislocation free, no threading dislocations were detected by cathodoluminescence in these structures. This method may also be useful in the growth of GaAs on Si substrates, however particular design patterns should be tested in order to determine if the result is compatible with device applications.



Fig. 6: Cross-section TEM micrograph near the patterned boundary. Note stacking faults present at the boundary with polycrystalline material grown over SiN and very low density of defects within the stripe of 100nm width GaAs.

Strained Layer Superlattices

As mentioned before, in order to obtain device quality epitaxial GaAs material, a reliable method for suppressing defect propagation in the epilayer is necessary. One promising method is to use strained layer superlattices (SLSLs), which cause dislocations to bend into the strained interface, thus promoting dislocation interactions. It was reported [8] that by application of SLSLs of InGaAs/GaAs with 10 nm thick periods grown on Si (211) blocking of dislocation propagation did not occur at all interfaces inside the SLSLs, but occurred almost entirely at the uppermost interface between the strained layers and the final GaAs layer [Fig. 7]. It was concluded that reduction of dislocation density was only weakly dependent on the number periods of the strained-layer superlattices. InGaAs/GaAs strained-layer superlattices proved to be more efficient in dislocation bending than InGaAs/InGaP SLSLs. Because it was recognized that the number of periods did not influence the reduction of dislocation propagation and that the upper interface of SLSLs is most efficient in dislocation bending, packages consisting of 5 periods of SLSLs (InGaAs/GaAs) were applied. Indeed, each set of SLSLs caused additional dislocation bending, but in some areas additional dislocations were formed at the lower interface between the buffer layer and the SLSL (Fig. 8). Therefore, in some areas the dislocation density was slightly higher. However, on the average, the dislocation density in this sample was in the $\sim 2 \times 10^7/\text{cm}^2$ range, which is very low taking into account that all misfit dislocations in the GaAs grown on Si(211) are 60° dislocations with Burgers vector inclined to the interface.



Fig. 7: TEM cross-section micrograph of the GaAs/Si interface with 50 periods of InGaAs(25%In)/GaAs SLSL grown directly at the interface with Si. Note the large number of stacking faults formed at the interface, propagating through the SLSL and stopping at the last interface with epilayer of GaAs. Bending of dislocations was most effective at this interface as well.



Fig. 8: TEM micrograph of the GaAs/Si interface with the application of three packages of ten periods each of the InGaAs/GaAs SLSL. Note dislocation bending at each package interface (occasionally, the formation of new dislocation was observed). Application of packages of SLSL was most successful to decrease dislocation density in the epilayer.

This kind of SLSL was applied to growth of GaAs on Si(100) and results obtained were very similar [47] to the ones obtained on Si (211) surfaces. Yamaguchi et al. [48] reported that strain is related to the composition of SLSLs and their thickness. Two kinds of critical thickness are important to achieve successful application of SLSLs: a critical thickness h_{c1} must be exceeded to introduce enough strain necessary for dislocation bending and the layers should not exceed a critical thickness h_{c2} which causes the generation of new dislocations.

CONCLUSIONS

This report on the mechanisms to reduce the density of structural defects in heteroepitaxial growth of GaAs on Si leads to the promising conclusion that such growth is possible and higher quality of the epilayer appears to be possible. The first step, the controlled growth of antiphase domain free GaAs/Si has been achieved. The cleaning of the Si substrate has been improved, but is not yet satisfactory. Of special interest should be approaches avoiding the high temperature substrate annealing steps currently used. Such high annealing temperatures result in roughening of the Si surface and are generally incompatible with patterned epitaxy. A promising approach is the use of Ga reduction and/or the growth of ternary, Al-containing buffer layers as pioneered by Umeno's group [32, 33].

Further defect reduction strategies such as thermal cycling during the growth, post-growth annealing and the use of strained layer superlattices have to be optimized. Combined use of some of these methods together with the possibilities of patterned epitaxy appear to make high-quality growth of lattice mismatched heterostructures such as GaAs/Si achievable. Only such optimized low-defect material will allow to make practical use of the numerous devices possible with this technology, including minority carrier devices, the feasibility of which already have been demonstrated in GaAs/Si heteroepitaxy.

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THE USE OF SUPERLATTICES TO BLOCK THE PROPAGATION OF DISLOCATIONS IN SEMICONDUCTORS

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ABSTRACT

Since the discovery in 1973 that GaAs/GaAsP superlattices can be grown with low dislocation densities, considerable interest has developed in utilizing superlattices as dislocation filters in multilayer semiconductor device structures. Many attempts to implement this process have been described, with varying degrees of success being achieved. Some investigators have reported favorable results; some have observed no effect; and in some cases the situation was actually made worse. This paper analyzes these reports and attempts to clarify the confusion that has arisen. Suggestions are made for improved effectiveness. Factors considered include the strain between layers, the layer thickness, the concept of critical thickness, the dislocation geometry, and the influence of buffer layers and growth conditions.

INTRODUCTION

In the late 1960s John W. Matthews published a series of papers describing his observations of transformations between misfit and threading dislocations in thin films. The first films were of various metals deposited epitaxially upon non-lattice-matched metal substrates [1,2]. Subsequently, an experiment with the semiconductors Ge on GaAs was carried out, where low-temperature growth produced a strained, curved epitaxial layer that unbent upon annealing, with the simultaneous introduction of misfit dislocations at the Ge/GaAs interface [3]. Based upon these observations Matthews developed the novel idea that misfit strain between an epitaxial layer and its substrate, if properly chosen, could be used to force dislocations in a given substrate to bend over into a misfit configuration and then run out of the crystal, producing a dislocation-free epitaxial layer.

In the mid-70s Matthews and colleagues tried to put this concept into practical use with the semiconductor system GaAsP on GaAs. The first attempts to implement this procedure used single layers of GaAsP strained by a small fraction of 1% with respect to the GaAs substrate. These single-layer experiments were largely unsuccessful at the time, but a pronounced effect was observed with superlattices, and several papers were published that demonstrated a drastic reduction in the dislocation density of GaAsP/GaAs superlattices [4]. Although some things remained unclear at that time, Matthews' publications displayed an amazing depth of understanding of dislocation processes. Unfortunately, his premature death denied him the opportunity to completely elucidate all the mechanisms.

ELIMINATION OF DISLOCATIONS IN GaAsP/GaAs SUPERLATTICES

The semiconductor superlattice had been in existence only a short while at that time. The first superlattices to be grown [5] exhibited very poor electrical properties. Matthews discovered the reason for their failure. He found that the superlattice interfaces contained an extremely high density of dislocations, $\sim 10^8 \text{ cm}^{-2}$; and he recognized that the vast majority of these dislocations arose because of the misfit between the substrate and the superlattice taken as a whole and not, as was generally supposed, the misfit between the adjacent sublayers. He proposed, therefore, a two-part solution to the problem [4]: (i) misfit between adjacent layers will not produce misfit dislocations if the layer thickness is maintained less than some critical value; and (ii) there will be no misfit between the substrate and the superlattice as a whole if a carefully graded buffer layer is introduced between the substrate and the superlattice. The compositional grading must be done in such a way that the composition at the top of the graded layer is equal to the average composition of the superlattice; or, what

amounts to the same thing, that the lattice constant at the top of the grade should be equal to the average of the lattice constants of the two components of the superlattice.

This prescription worked very well on its very first trial. The threading dislocation density was reduced from $\sim 10^8$ to $\sim 10^4 \text{ cm}^{-2}$, and the result was the first strained-layer superlattice. It is important to realize that it was not the superlattice itself which reduced the number of dislocations in the multilayer; it was the graded layer which did so. And the intended purpose of the revised growth procedure was actually not to remove existing dislocations but to prevent new ones from being formed.

Nevertheless, analysis of those early layers suggested that some filtering had taken place. This was deduced from etch pit counting, which showed a decrease in threading dislocation density from 10^6 cm^{-2} below the superlattice to 10^2 above it [4]. Further proof is exhibited in Fig. 1, which shows three TEM cross-sections performed several

Fig. 1: TEM cross-sections of $\text{GaAs}_{0.5}\text{P}_{0.5}/\text{GaAs}$ superlattices: (a) without and (b,c) with graded layer.



a



b



c

years later and not heretofore published. Fig. 1a shows a GaAs_{0.5}P_{0.5}/GaAs superlattice grown without a graded compositional layer between the substrate and the superlattice. It contains dense tangles of dislocations within the superlattice and near the first interface. The specimen of Fig. 1b had a graded layer, and one can see many interfacial dislocations running horizontally in the TEM foil and two sets of truncated ones which are slightly oblique to each other and nearly normal to the $\sim (110)$ foil. All of them are misfit dislocations. It is clear in this case that there are no misfit dislocations in the upper layers, so it appears that a filtering action took place in the first dozen or so layers. Fig. 1c has no dislocations at all, which suggests that the compositional grading in the buffer layer was very precise and effective.

As to why the superlattice was a more effective dislocation blocker than the single layer arrangement, this is not completely clear. It was noted that multiplication of threading dislocations is less probable in thin layers than in thick ones [6], and that the multiple layers should enable dislocations to pass by each other on different levels, thus avoiding the extensive interactions that would occur if all of them tried to escape the crystal on the same misfit plane. Part of the reason why the single layer experiments did not succeed seems to be the fact that the epitaxial layer was in tension rather than compression. It has been found by several investigators that a compressive epi layer can confine dislocations to the interface more effectively than can a tensile one [7,8]. In the superlattice, of course, one has both compressive and tensile layers alternating with one another.

RECENT PROGRESS

In the past ten years or so a great deal of effort has been expended in using misfit strain to regulate dislocation propagation. The work has taken two basic thrusts, which are to some extent opposite in intent. The first of these is to actually produce misfit dislocations in a superlattice in order to provide a reduced density of threading dislocations at some remote point where there is an active device layer, such as a laser or a solar cell. In particular, the major application of this technique has been in trying to improve the perfection of GaAs grown on silicon. The other major thrust is to prevent the formation of misfit dislocations in an elastically stressed layer that is the site of an active device. This stressed layer is said to be pseudomorphic. A Cornell-IBM team of researchers has made many significant contributions to the understanding of pseudomorphic growth [9]. Another group at Sandia Labs has published extensively in the areas of both pseudomorphic growth and strained layer superlattices [10].

Results in dislocation filtering have been rather disappointing. Some workers have confirmed a partial filtering effect; some have reported no effect; and in some cases the superlattice actually created a greater number of dislocations than it removed. The rest of this paper deals with assessments of these conflicting results and attempts to reconcile them.

Bedair et al. succeeded in eliminating essentially all of the threading dislocations emanating from the substrate in homoepitaxially grown GaAs by using an InGaAs superlattice [11]. However, the total number of dislocations was quite low to start with. The system GaAs/Si contains far more dislocations than GaAs/GaAs and seems to be less tractable to the filtering process. Among the recent results, for example, Al-Jassim et al. observed a reduction of 10-15 times in GaAs/Si samples that contained InGaAs/GaAs superlattices and were also subjected to high-temperature anneals [12]. Similarly, the Bedair group obtained an estimated tenfold reduction with InGaAs/GaAsP superlattices combined with annealing [13].

Cao et al. also found up to 50 \times reduction in dislocation density for MOCVD growth of GaAsP/GaAs when the superlattice was combined with a so-called "growth overshoot" in the graded layer [14]. This is a bit better than the etch-pit results reported much earlier by Matthews and Blakeslee [4]. Finally, an AT&T Bell Labs group has experimented with GaAsP superlattices in complicated GaAs laser epitaxial structures grown on Si-Ge. TEM micrographs indicated that high concentrations of dislocations were trapped in the superlattice situated between the Ge and the GaAs [15].

FACTORS GOVERNING DISLOCATION BEHAVIOR

Theoretical Considerations

The theory for the elimination of threading dislocations by applying misfit stress was built upon the earlier work of Frank and van der Merwe [16]. They originated the basic concept that at some critical thickness, h_c , a mismatched epitaxial layer should develop a cross-grid of misfit dislocations. At layer thicknesses, h , less than h_c , the atoms in the epitaxial layer are strained elastically to occupy the same positions in the plane of growth as those directly beneath them in the substrate. When the critical thickness is reached it becomes energetically favorable for the misfit to be relaxed by the cross-grid of misfit dislocations.

The equilibrium theory was developed by considering a balance of forces upon a threading dislocation. These forces are due to the misfit, f , and the line tension in the dislocation. When the misfit stress builds up to the point where it slightly exceeds the line tension opposing it, a dislocation propagating into the epitaxial layer from the substrate becomes unstable and may glide, leaving a segment of misfit dislocation in the interface. The misfit force is proportional to the thickness, the misfit, f , and the magnitude of the Burgers vector of the dislocation, b . This force is

$$F_m = [2G(1+\nu)/(1-\nu)] f b h \cos \lambda \quad (1)$$

and the line tension is proportional to the square of the Burgers vector and to the logarithm of the epitaxial layer thickness.

$$F_l = [Gb^2/4\pi(1-\nu)] (1-\nu \cos^2 \alpha) [\ln(h/b) + 1] \quad (2)$$

where G is the shear modulus, ν is the Poisson ratio, and λ and α are angles depicted in Fig. 2. At the critical thickness the two forces are equal. Equating them and solving for the layer thickness gives the value of h_c , the layer thickness at which the misfit dislocation array becomes stable.

$$h_c = \frac{b(1-\nu \cos^2 \alpha) [\ln(h_c/b) + 1]}{8\pi f(1+\nu) \cos \lambda} \quad (3)$$

This is the critical thickness for a single layer. The same equation can be derived from energy balance considerations instead of a balance of forces, as shown by Matthews in Ref. 17. A plot of h_c as a function of misfit strain is given in Fig. 3. This plot can also be used for a superlattice that is unstrained with respect to its substrate, according to

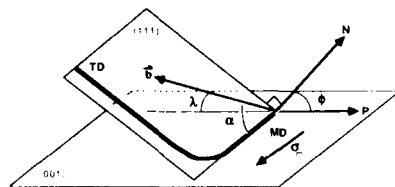


Fig. 2: Geometry of glide for 60° dislocations. MD is misfit segment; TD is threading segment. See text for explanation of other symbols.

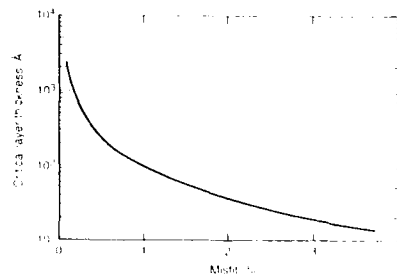


Fig. 3: Critical layer thickness vs. misfit for single mismatched layer.

Matthews [4], by multiplying the single layer thickness by 4. More recent work by van der Merwe shows that this factor is not exactly 4, but is closer to 5.4 [18].

Geometrical Factors

Implementation of the foregoing theory requires that a dislocation can glide (or slip) on its glide plane in response to the misfit stress in the overlayer. The glide plane in Group III-V and Group IV semiconductor crystals is any one of the four $\{111\}$ planes, and the dislocations that glide upon them are the so-called 60° dislocations. They have Burgers vectors inclined 45° to the (001) interface, as shown in Fig. 2. The component of the misfit stress, σ , which can act to move the dislocation is its projection upon the glide plane and is called the resolved shear stress. It is expressed as

$$\sigma_{\text{res}} = \sigma \cos \lambda \cos \phi \quad (4)$$

where the angles λ and ϕ are indicated in Fig. 2. For 60° dislocations and $[001]$ growth the maximum stress is in the (001) misfit plane, and the cosines of λ and ϕ are 0.5 and 0.816, respectively.

Justification for considering only the 60° dislocations in the theory of Matthews' was that these dislocations predominated in specimens examined by TEM [4,19,20]. One of them is illustrated in Fig. 2. It lies in a $\{111\}$ glide plane and has two components, a misfit component MD lying in the interface and a threading component TD inclined to the interface. The force which drives the threading component toward the edge of the plane and increases the length of the misfit component is the force σ_m due to the mismatch stress. It is equal to the product of σ_{res} and b .

Another hypothetical 60° dislocation is illustrated in Fig. 4a. It consists of a $[1\bar{1}0]$ misfit segment connecting two threading segments oriented along $[011]$ and $[\bar{1}12]$, respectively. Similarly oriented threading dislocations are often seen by TEM and can be moved in response to a glide force. Figure 5 shows a GaAsP superlattice with $\sim 1.4\%$ strain between the layers. A large number of 60° dislocations threading up from the

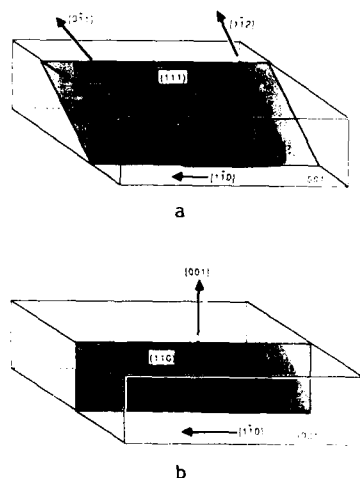


Fig. 4: Schematic of (a) 60° dislocation and (b) edge dislocation.



Fig. 5: GaAs_{0.9}P_{0.1}/GaAs_{0.5}P_{0.5} superlattice containing sessile dislocation (X), bent-over glide dislocations (Z), and stacking fault (Y).

buffer layer have been bent over into the first few superlattice layers at Z. The misfit segment of the dislocation in Fig. 4b is oriented parallel to the 60° misfit segment in Fig. 4a. It is twice as effective in relieving misfit because its Burgers vector lies totally in the misfit plane, but if, by some growth process, it becomes bent out of this plane into a threading configuration such as $\{001\}$, it cannot be moved by a superlattice. Its glide plane is $\{110\}$, and the critical resolved shear stress is too high for this dislocation to glide away. Therefore, it will propagate through all successive layers grown. Vertical sessile (immobile) dislocations similar to this are often seen in TEM studies [21]. Three of them can be seen at points labeled X in Fig. 5.

In the past it was found that most misfit dislocations in diamond or zincblende semiconductors are nucleated as half-loops on $\{111\}$ planes at surface steps and then glide down to the interface [4,21]. Lomer dislocations with $b = a/2\langle 110 \rangle$, which relieve the maximum misfit, can be formed by the pairwise interactions of these glide loops on different glide planes. Now it is also understood that pure edge misfit dislocations can be nucleated directly at the interface if the misfit stress is sufficiently high, as is the case for GaAs on Si [22-24]. It is clear, therefore, that dislocations other than the 60° type must be contended with, and methods must be found to prevent the formation of edge-type threading dislocations such as the hypothetical example of Fig. 4b.

Magnitude of the Stress

Equation 3 for the critical layer thickness has been tested experimentally, with varying results. When the experimental conditions truly produced equilibrium, the theory predicted the observations reasonably well. The equilibrium situation is not, however, what is generally seen experimentally. B. Dodson and his colleagues at Sandia Laboratories [25] have provided insight as to why the experimental "critical thicknesses" were often substantially greater than those predicted by the Matthews theory. They have shown that the layers tend to be metastable and to produce misfit dislocations in large numbers only at thicknesses that can be several times the equilibrium critical thickness. Annealing at a higher temperature will usually reduce the metastable apparent critical thickness to the true value.

Another important point that has been emphasized by Dodson et al. is that the dislocations are subject to frictional forces and kinetic barriers must be overcome in order to get them to move, so the stresses predicted by Matthews must be exceeded. They have extensively investigated the nature and magnitude of this excess stress. The equation that they derived for the excess stress is

$$\sigma_{\text{exc}} = \frac{2Gf(1+\nu)}{1-\nu} - \frac{bG(1-\nu)^2 \cos^2 \alpha}{2\pi h(1-\nu)} \ln(4h/b) \quad (5)$$

where the symbols have the same significance as in Eqs. 1-3. The first term represents the misfit stress, and the second one is the line tension. The difference between them is the excess stress, which is the driving force for strain relaxation. From this concept they have developed a model for relaxation of the strain. The relaxation is a function of the mobility of the dislocation, which in turn is a function of the excess stress and of the temperature. From this model they have calculated an apparent critical thickness that one would see under common experimental conditions as a function of misfit. Their curve fits very well the data of Bean et al. on Si/Ge [26]. It lies considerably above the equilibrium curve, especially at low values of misfit.

If the motivation is to keep the layer coherent, one must maximize all those factors which promote metastability. If, on the other hand, the intent is to filter dislocations, the equilibrium stress must be exceeded. We believe that the effects of excess stress have been manifested in results published by Bedair et al. [11] and Al-Jassim et al. [12]. These works have in common the fact that the filtering was more effective when the superlattice was not exactly matched to its substrate but rather when there was an excess overall strain. We suggest that this is a consequence of unbalanced

strain at the first and last interfaces being distributed throughout the superlattice, imparting some excess stress to each superlattice layer.

Figure 6 shows a TEM cross-section of another, less defective area of the superlattice displayed in Fig. 5, including several steps in the compositionally graded buffer layer. It shows that dislocation filtering is possible, i.e. that misfit dislocations are confined to the interfaces, for superlattices with layers considerably thicker than h_c . The critical period for this superlattice is about 400 Å, whereas the actual period of the structure is 900 Å; yet filtering has taken place without the nucleation of new dislocations. A sort of filtering has also taken place at interfaces in the step-graded buffer layer, but the confinement of the dislocations is not as good as it is in the superlattice. This lack of confinement is also evident in Fig. 7, which is a TEM cross-section of a GaAs/Si specimen grown by the Bedair group and containing three superlattices in series [13]. Even though the superlattices were carefully balanced against the GaAs on either side by alternating compressive GaInAs with tensile GaAsP in the superlattices, much of the dislocation bending takes place above and below them. This suggests, possibly, that there was too little stress within the superlattices, i.e., that the interfacial dislocations might have been confined more effectively if the sublayers had been made thicker. Both Fig. 6 and Fig. 7 show evidence of dislocation interaction and dissociation, probably yielding product dislocations that will not glide. These types of interactions need to be studied more extensively. They can be lessened to some extent by employing less abrupt compositional steps.



Fig. 6: TEM cross-section of a GaAs_{0.9}P_{0.1}/GaAs_{0.5}P_{0.5} superlattice grown on a step-graded buffer layer. Note horizontal misfit dislocations in superlattice.



Fig. 7: TEM cross section of three successive 5-cycle In_{0.2}Ga_{0.8}As/GaAs₆₈P₃₂ superlattices in GaAs/Si. (Courtesy of S. Bedair.)

It is quite possible, of course, to apply too much misfit stress and thus exceed the limit for nucleating new dislocations. This is what happened when the superlattices were grown without any graded layer (Fig. 1a). Another example of this effect apparently shows up in the report of Yamaguchi et al. [27], where the dislocation density was observed to decrease steadily with increasing layer thickness and then to increase abruptly.

Effects of Specimen Size

Even at 100% efficiency, the filtering process will have some upper limit on the number of threading dislocations that can be eliminated. A simplistic calculation

$$\rho_{\max} = \frac{4f}{bL\cos\lambda} \quad (6)$$

shows that the maximum density of dislocations that can be filtered (for a square substrate) is limited by the misfit f and is inversely proportional to the length L of one side. For a 1-cm specimen, to remove 10^4 dislocations cm^{-2} , which is a typical number for a commercial GaAs substrate, requires a very trivial misfit of 0.005%. To remove one million, typical of graded GaAsP, requires 0.5%, which is reasonable. On the other hand, to remove a density of 10^8 , such as one finds in GaAs/Si, would require a totally unachievable misfit of 50%. If one uses a superlattice instead of a single layer and makes the gross assumption that every layer in the superlattice can be fully saturated with misfit dislocations, another factor of 50 in ρ_{\max} is obtained; or, looking at it differently, the misfit necessary to eliminate 10^8 substrate dislocations per cm^2 can be reduced from 50% to 1%, a reasonable value.

The question of specimen size has been thoroughly investigated by the Cornell-IBM group, who made mesas of different sizes on their specimens and studied the density of dislocations as a function of mesa size and strain. They found that the interfacial density increased very rapidly with increasing mesa diameter. They were able to control the process such that they could activate first the bending of threading dislocations, then the generation of dislocations via multiplication, and finally, dislocation nucleation at surface steps [10].

Necessity for Two-Dimensional Growth

It is important to realize that the operation of this process depends upon the assumption that one can achieve two-dimensional layer growth, or at least a close approximation to it. Without parallel interfaces, there is little chance that the glide process can be effective at all. It is rather paradoxical that increasing the strain, which is necessary for dislocation glide, at the same time enhances the probability of 3-D nucleation. This effect is discussed in a recent paper concerned with the influence of interlayer strain on the morphology of epitaxial layers [28]. An example of it is shown in Fig. 8, which is a TEM cross-section of a highly distorted region in an MOCVD-grown GaAsP superlattice. The distortions were initiated by 3-D nucleation. Even though some dislocations were confined to the superlattice interfaces (point X), a greater number of threading dislocations were created by the distorted superlattice than were filtered by it (point Y). Reference 28 suggests some alterations in the growth procedure that can be effective in minimizing this type of 3-D layer growth.

Dislocation Interactions

When the misfit dislocations are brought close together, they may interact. Some of these interactions are harmful, producing new threading dislocations, but many of them are not harmful. Figure 9 shows a superlattice that has been etched in such a way as to remove successive superlattice layers. At X there are several dislocations that terminate at the edge of the terrace. They are obviously in the topmost layer and can cross over those below without interaction. However, at Y and Z, the orthogonal dislocations are in the same plane, and they do interact. There is a repulsive interaction at Z which does not appear to do any damage, and the attractive interaction at Y.

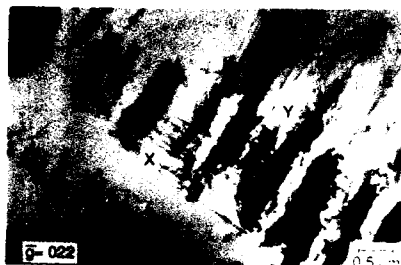


Fig.8: TEM cross-section of GaAsP superlattice with compositional distortions that generate dislocations.

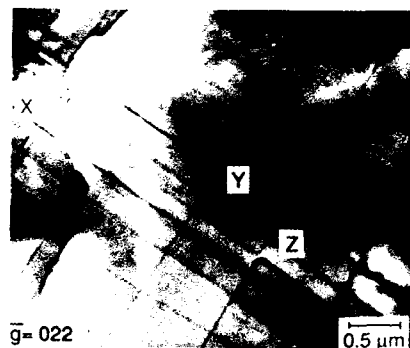


Fig.9: TEM plan view of misfit dislocations on different layers in a GaAs_{0.9}P_{0.1}/GaAs_{0.5}P_{0.5} superlattice.

produces a very short segment of a third connecting dislocation, which is perhaps not visible in the figure. Reactions such as these were first catalogued by Abrahamis et al. [20]. One way to avoid harmful interactions is to activate a or fast dislocations at a different time from the slower, orthogonal β dislocations, so that they cross each other at different levels in a strained layer. This has actually been done [29], but it is very difficult to control.

A more effective way to minimize harmful interactions is to improve the characteristics of the graded layer. Experience with very long grades, such as those common in hydride VPE growth of GaAsP/GaAs, has shown that the shallower the grade, the fewer the dislocations [30]. Olsen et al. [31] have made a comparison of step grading and continuous grading in the heteroepitaxial VPE growth of GaInP on GaP. They concluded that step grading was somewhat more effective than continuous grading, but that both types of grading effectively reduced the density of threading dislocations in the constant composition region below the detectability limit for TEM, which is about 10^6 cm^{-2} . The most effective procedure according to them was to use step grading followed by an abrupt compositional step at the end of the graded region. We favor continuous grading over stepping since it tends to lessen the kinds of interaction which produce dislocations with unfavorable Burgers vectors at abrupt steps; and we would replace the abrupt step with a properly strain-balanced superlattice, which should be even more effective.

Crystal Inhomogeneities

The final point is that crystal inhomogeneities of almost every type can be detrimental. These defects include stacking faults, twins, inclusions and precipitates. They can disrupt dislocation movement, and they can actually nucleate new and unmanageable dislocations. Dislocations in the center of Fig. 5 are bent over and are proceeding to the right at Z, in a high density, and apparently are not interacting with each other. However, those going to the left cannot penetrate the stacking fault at Y, so they are reflected and will never get out of the crystal. Reference 32 emphasizes what a strong effect foreign-phase contamination has upon dislocation behavior and shows how an otherwise orderly arrangement of misfit dislocations can be severely disrupted by an oxide particle.

CONCLUSIONS

Misfit strain can be used to remove threading dislocations. Superlattices, when properly designed, are more effective than single layers, principally because they provide many alternative paths for the dislocations to lie on, thus avoiding each other and reducing the potential for harmful interactions. One essential ingredient of the proper design is that the superlattice thickness should be considerably greater than the equilibrium critical thickness in order to provide the necessary excess stress to move the dislocation. Another important factor is that strain gradients be as gentle as possible everywhere except in the superlattice itself. In this regard, continuous grading is to be preferred over step grading. In fact, it might be that growing a linearly graded $\text{Ge}_x\text{Si}_{1-x}$ alloy on a Si substrate and then depositing GaAs upon that would reduce the defect density in GaAs/Si. Since the glide process is not very effective for dislocations other than those of the 60° type, methods such as annealing or variation of the substrate orientation should be investigated for use in conjunction with superlattices in order to better handle the dislocations of different types. And it is of the utmost importance to avoid the occurrence of harmful growth defects.

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THE "BUFFER" LAYER IN THE CVD GROWTH OF β -SiC ON (001) SILICON

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ABSTRACT

The concept of a "buffer" layer in the epitaxial growth of compound semiconductors on (001) silicon substrate is discussed on the basis of homogeneous and heterogeneous surface nucleation. Experimental results on the nucleation of β -SiC on (001) Si by Chemical Vapor Deposition (CVD) are presented and they are discussed in terms of the model for the growth of the buffer layer.

INTRODUCTION

In the growth of many compound semiconductors on (001) silicon by Molecular Beam Epitaxy (MBE) or Chemical Vapor Deposition (CVD), a thin "buffer" layer is first grown at a relatively low temperature before the substrate is raised to a higher temperature and the bulk growth is carried out. The growth of a buffer layer seems to be a necessary step to attain an epilayer which is in parallel epitaxy with respect to the substrate. Without this step, i.e. carrying out the growth at a higher temperature in one step, often results in a polycrystalline deposit with a poor morphology.

The need for a buffer layer grew out experimentally and seems to be applicable to a number of systems (e.g. β -SiC/Si [1], GaAs/Si [2], GaP/Si [3],...) with widely different film/substrate mismatches in lattice constants, coefficients of thermal expansion, and elastic constants. In each case, the buffer layer itself is basically a thin continuous layer of the deposited material which seems to be no different from the bulk epilayer except for a higher defect density [4]. It usually forms by nucleation of (three-dimensional) islands and their coalescence into a continuous film which is monocrystalline with a parallel epitaxial orientation relative to the substrate and its lattice parameters are no different from the bulk overgrowth at least within the resolution of high resolution electron microscopy (HREM) [5].

The explanation of the need for a buffer layer for good quality epitaxial growth has not received much attention. However, in a recent paper [6], the low temperature growth of a buffer layer was explained on the basis of homogeneous versus heterogeneous surface nucleation and this will now be briefly summarized for the case of CVD.

Homogeneous nucleation is considered to be the formation of supra-critical clusters of atoms on clean and defect-free areas of the substrate surface. In the present context, steps on the substrate are considered to be sites for homogeneous nucleation as long as there is no impurity segregation at the steps and they are clean and defect-free. This is despite the fact that the steps are preferential nucleation sites as compared to the flat terraces on the substrate. The unique aspect of a homogeneous nucleus is its orientation relationship with respect to the substrate. In general, a supracritical cluster of atoms forming a homogeneous nucleus will be in parallel orientation with respect to the substrate because of the directional nature of the covalent bonds at the interface. In some ways, the substrate "communicates" its orientation to the deposited atoms through the interfacial bonding forces. Hence, in clean and defect-free areas of the substrate surface, the deposited atoms are forced to sit in the correct sites such that they will follow the orientation of the substrate on which they are depositing [6]. Presumably, this would be true even for a reconstructed substrate surface in the case of MBE, because the bonds would need to "deconstruct" in order to form interfacial bonds with the deposited

atoms. It is these bonds, of course, which determine the adhesion energy of the deposited film. As a result of the parallel orientation, the interfacial bonds will be least distorted (stretched or bent) as compared to other, misoriented, nuclei and the film/ substrate interfacial energy will be at a minimum [4]. Hence, the parallel nuclei can grow laterally on the substrate surface at a faster rate as compared to other misoriented nuclei.

In general, homogeneous nucleation requires the overcoming of a large energy barrier and can only take place at lower temperatures where the "supercooling" provides a large enough driving force for the formation of such supracritical clusters. The temperature, of course, cannot be so low that the gaseous compounds in the CVD reactor do not dissociate, or the chemical reaction necessary for the formation of the compound semiconductor cannot take place. In general, the nucleation rate of homogeneous nuclei is a thermally activated process and increases exponentially with decreasing temperature [6]. Thus, in the appropriate low temperature range, the nucleation rate will be very large and the high density of homogeneous nuclei and their ease of lateral growth results in rapid coalescence to form a thin (buffer) layer having the same orientation as the substrate. Once this thin, continuous, layer forms on the substrate, further growth may be considered as homoepitaxy. Hence the mode of growth changes from three-dimensional island growth to two-dimensional, layer-by-layer, growth and thus the temperature may be safely raised to a higher value and deposition continued at a faster rate [6].

On the other hand, if the substrate is raised to a high temperature from the beginning of growth, the driving force for homogeneous nucleation is low and the density of homogeneous nuclei will be very small. There is, however, a very low energy barrier for "heterogeneous" nucleation, i.e. nucleation at "contaminated" or "defective" sites on the substrate surface. The number of these sites is limited and depends on the state of the substrate surface preparation (e.g. polish) and surface cleaning. In general, heterogeneous nucleation requires a small driving force and a slight "supercooling" is sufficient for this purpose; thus it can take place even at relatively high temperatures. In fact, at sufficiently high temperatures, this is practically the only type of nucleation that takes place. Now, at a contaminated site, the "communication" between the substrate and the deposited atoms (through the interfacial bonding forces) is broken down, and the supracritical atom clusters that form heterogeneous nuclei will not be forced to have the same orientation as the substrate but can have any arbitrary orientation. Since, at high temperatures, the growth rate is high, the heterogeneous nuclei will grow rapidly and, in the absence of homogeneous nuclei, will coalesce to form a polycrystalline layer.

In brief then, the buffer layer is grown at a temperature sufficiently low that homogeneous nucleation completely dominates over heterogeneous nucleation. According to this model, on an ideally clean and defect-free substrate surface, where no heterogeneous nucleation sites are present, there should be no need for growing a buffer layer and growth can be carried out in one step.

In the present work, some preliminary nucleation studies have been made on the growth of β -SiC on (001) Si by CVD in order to get a better understanding of the buffer layer. It should be mentioned that in the growth of SiC, in contrast to other compound semiconductors, the buffer layer is grown during the "ramping" period when the carbon-containing gas (e.g. propane) is introduced in the chamber at room temperature and the substrate is ramped up to the growth temperature [1]. During this ramping process, a thin (buffer) layer of SiC forms on the substrate where the necessary silicon for the formation of SiC is provided by the substrate. However, the minimum temperature at which the gas dissociates and the SiC molecules form stable nuclei on the substrate is not known exactly. Thus, a series of experiments on the nucleation of SiC were performed in the CVD reactor used for growing this material. The deposited material was subsequently studied by Nomarski optical microscopy and Transmission Electron Microscopy (TEM). This work is briefly discussed below and the results are shown to be basically consistent with the above discussion of the buffer layer formation.

EXPERIMENTAL

(001) silicon wafers were heated in a CVD reactor to different initial growth temperatures (1000, 1070, and 1170°C). Following this, propane gas was introduced into the reactor for various times (5, 10, 15, 20, and 30 s). The resulting layers were then characterized using Nomarski differential interference contrast microscopy, plan-view TEM, and cross-sectional High Resolution Electron Microscopy (HREM).

RESULTS

The results of the initial growth experiments performed in this work are summarized in Table 1:

Table 1

Time (s)	1000°C	1070°C	1170°C
5	—	No trace of SiC	—
10	No trace of SiC	$4 \times 10^{10} \text{ m}^{-2}$	$3 \times 10^8 \text{ m}^{-2}$
15	—	Continuous SiC film	—
20	—	—	$4-5 \times 10^9 \text{ m}^{-2}$
30	No trace of SiC	—	—

The island densities in Table 1 were measured from optical micrographs. As seen in this table, there appears to be an incubation time for the nucleation of SiC. This is, however, only within the resolution of optical microscopy which detects island nuclei which are larger than a certain size. In some cases, it is possible that nucleation has in fact taken place but that the size of the island nuclei is too small for them to be detected.

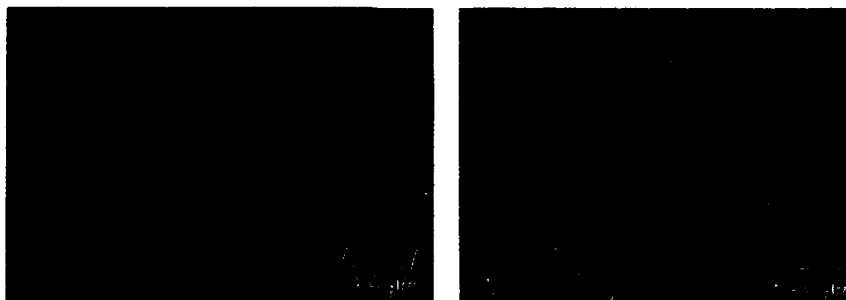


Fig. 1) Nomarski micrographs of SiC islands grown at 1170°C for (a) 10 s, (b) 20 s. Note the dark central feature at the center of islands.

We start with the growth experiments at 1170°C. After 10 s of growth at this temperature, a small number of disc-like islands ($\sim 3 \times 10^8 \text{ m}^{-2}$) were

observed which had an average diameter of 5-10 μm (Fig. 1a). After 20 s, the island density was higher ($\sim 4-5 \times 10^9 \text{ m}^{-2}$) and the average island size was larger indicating that they had grown. Some islands in fact had already started to coalesce (Fig. 1b). Practically all the islands had a distinct feature at their center showing dark contrast under Nomarski illumination. Each island appeared to grow radially from this central dark feature. This may indicate that nucleation had taken place at some impurity/defect (i.e. heterogeneous) site and then grown radially outward. A high density of pits on the substrate were also observed under each island. Each pit forms by the agglomeration of silicon vacancies that are generated in the substrate when Si atoms diffuse to the SiC nucleus to react with the C atoms and form SiC molecules. The pits are faceted and come either in the shape of an inverted pyramid with a square base at the substrate surface (Fig. 2), or in the form of an octahedron (two pyramids, base-to-base) just below the substrate surface (Fig. 3). In general, the SiC islands in the vicinity of the pits are misoriented and highly faulted. An example may be seen in Fig. 3. Away from the pits, however, the SiC deposit has a lower density of faults and is often in parallel orientation with respect to the substrate. This is shown in the HREM micrograph of Fig. 4.



Fig. 2) Cross-sectional HREM micrograph of an inverted pyramidal pit on the substrate surface (15 s at 1070°C).



Fig. 3) Cross-sectional HREM micrograph of a SiC deposit on the Si substrate above an octahedral pit (20 s at 1170°C).

At 1070°C, after 10 s, the density of islands was $\sim 4 \times 10^{10} \text{ m}^{-2}$, i.e. two orders of magnitude higher than the equivalent time at 1170°C. This is a minimum value because the size of the nuclei is smaller at the lower temperature and so a larger fraction of them may be beyond the resolution of Nomarski microscope. The average diameter of the islands was about 1-2 μm (Fig. 5a). The islands do not appear to have any distinct central feature; rather they look uniform throughout. This may indicate that the dominant form of nucleation at this temperature is by a homogeneous process. After 15 s of growth, the SiC film was continuous and completely covered the

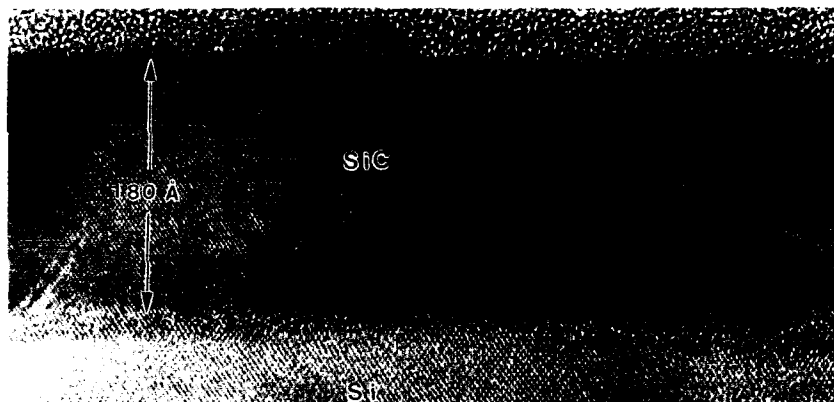


Fig. 4) Cross-sectional HREM micrograph of SiC/Si away from a pit center (20 s at 1170°C).

substrate surface, i.e. a buffer layer had been produced (Fig. 5b). Fig. 6 is a HREM micrograph of the continuous film which shows that it is in parallel epitaxy with respect to the substrate. Again a high density of pits could be observed under the islands (10 s) or under the continuous film

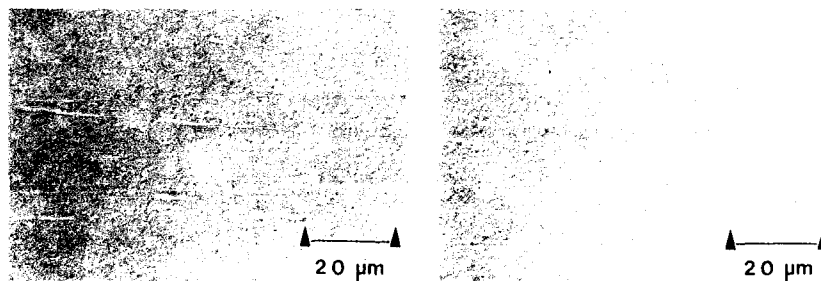


Fig. 5) Nomarski micrograph of SiC grown at 1070°:
(a) islands after 10 s, (b) continuous film after 15 s.



Fig. 6) Cross-sectional HREM micrograph of the continuous SiC epilayer shown in Fig. 5(b).

(15 s; Fig. 2).

At 1000°C no trace of SiC could be detected up to a time of 30 s. A number of possibilities could account for this, e.g. (a) the incubation time at this temperature may be higher than 30 s, (b) the nuclei may be too small to be detected even after 30 s of growth, (c) the temperature may be too low for propane to dissociate or for SiC molecules to form.

CONCLUSION

The present work discusses the necessity of growing a buffer layer at a relatively low temperature on the basis of homogeneous and heterogeneous nucleation on the substrate surface. Heterogeneous nuclei forming at contaminated/defective areas of the substrate surface do not necessarily follow the orientation of the substrate. They form rather easily at any temperature, but their number is limited depending on the perfection and cleanliness of the substrate surface. On the other hand, clusters on clean and defect-free areas of the substrate surface, forming the homogeneous nuclei, are forced to follow the orientation of the substrate through the interfacial bonding forces. Such homogeneous nuclei are much more difficult to form and require a substantial amount of supercooling as the driving force. Their number, however, is not limited but rather increases exponentially as the temperature is lowered. Hence, below a certain growth temperature, the density of homogeneous nuclei completely dominates the heterogeneous ones and their growth and coalescence results in a buffer layer with the same orientation as the substrate. Preliminary experiments on the nucleation of β -SiC on (001) silicon have been carried out which support this model. However, much more experimental and theoretical work is required to get a more complete understanding of the role of the buffer layer.

ACKNOWLEDGMENT

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EFFECTS OF GROWTH TEMPERATURE ON MOCVD-GROWN GaAs-ON-Si

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ABSTRACT

Effects of growth temperature on crystallinity and surface morphology of MOCVD-grown GaAs-on-Si were studied. The FWHM of the (400) x-ray peak in the rocking curve of GaAs-on-Si reduces from 340 to 230 arcs with increasing growth temperature from 650 to 700°C, but further increase of growth temperature does not significantly decrease the FWHM. The surface morphology of GaAs-on-Si grown at higher temperature is scaly and rough. Lower growth temperature is desirable to obtain GaAs-on-Si with good surface morphology. In order to eliminate the trade-off between crystallinity and surface morphology, the three-step growth process is proposed.

INTRODUCTION

The advantages of GaAs-on-Si material are well recognized. The GaAs-on-Si technology will allow integration of GaAs and Si circuits on the same chip, which can take advantages of the high-density Si technology and the high-speed or optoelectronic GaAs technology. This combination is particularly attractive for optical interconnections in the Si VLSI.

There are, however, expected heteroepitaxial problems created by 4 % lattice mismatch, large thermal expansion coefficient mismatch and polar/non-polar interface with antiphase domain formation and cross-doping.

Surface morphology, crystallinity and background carrier concentration greatly affect fabrication of GaAs devices and their characteristics. Good control of the material and electrical properties of GaAs-on-Si is a key to the successful GaAs-on-Si technology, which enjoys assets of both the Si and GaAs technologies.

Growth temperature influences the material and electrical properties of MOCVD-grown GaAs-on-Si. The GaAs layer grown on Si by the two-step growth process [1] at higher temperature shows good crystallinity but poor surface morphology. In order to obtain both good crystallinity and surface morphology of GaAs-on-Si, the three-step growth process is proposed in this paper.

EXPERIMENTAL

GaAs layers were grown in an atmospheric-pressure, horizontal MOCVD reactor on n(100) Si substrates 2 degrees off toward [011] at various temperatures, 650, 700, 750 and 800°C. The source materials are TMG (trimethylgallium) and arsine (100 %).

Before the growth, a susceptor was heated in H₂ at 1020°C for 30 min. Si substrate was chemically cleaned to remove

metallic contaminants and native oxide prior to loading into a reactor. Following a high-temperature heat treatment of the Si substrate at 1000°C for 10 min in H₂, the two-step growth process was employed. Arsine was introduced into the reactor at 900°C on lowering temperature to 400°C. A 12.5 nm-thick low-temperature nucleation layer of GaAs was deposited at 400°C, and then 3 μm-thick GaAs layers were grown at various temperatures. For comparison, 3 μm-thick GaAs layers were also grown on GaAs substrates without a low-temperature nucleation layer at various temperatures.

Surface morphology of the GaAs top layer was examined under a Nomarski optical microscope, and crystallinity was assessed using double-crystal x-ray diffraction. The FWHM of the (400) x-ray reflection peak in the rocking curve was studied as a function of growth temperature. Cross-section TEM was carried out to provide an insight picture of dislocations. RHEED and Raman spectroscopy were also used to probe the surface structure. It should be also noted that all characterization results discussed in this paper are averaged over several runs with the same growth conditions and reproducible.

RESULTS AND DISCUSSIONS

Surface morphology of the GaAs layers grown on Si at various temperatures is shown in Fig. 1. The surfaces are all

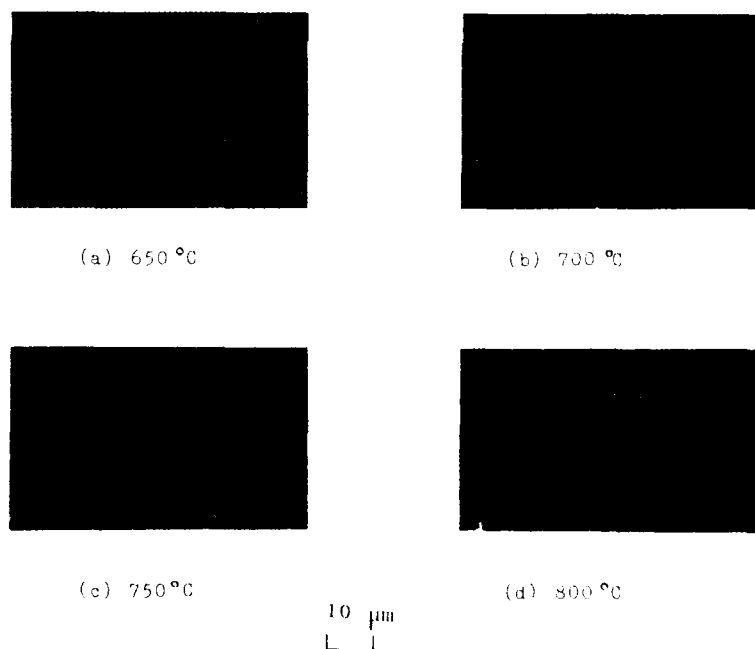


Fig. 1 Surface morphology of GaAs layers grown on Si at various temperatures.

mirror-like. The surface morphology becomes scaly and the surface becomes "rough" with periodic "tread and riser" [2] as growth temperature is increased. The GaAs layer grown at 750°C shows nonuniformity in the surface morphology, and a portion with a slightly hazy surface contains many scattered small islands under a Nomarski microscope, although both specular and hazy portions show the same texture of the morphology as seen in Fig. 1. A reason for this nonuniformity reproducibly observed only with the growth temperature of 750°C is not clear at present.

Raman spectroscopy is used to further probe the surface structure of the GaAs layers grown on Si at 750°C. In Fig. 2 the peak at 292 cm^{-1} is associated with the allowed scattering by

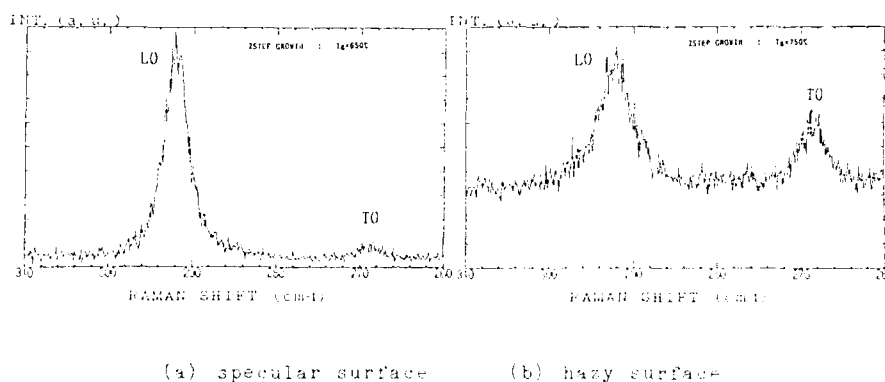


Fig. 2 Raman spectra of GaAs layers grown on Si at 750°C.

the longitudinal optical (LO) phonon, whereas the peak at 260 cm^{-1} corresponds to a forbidden scattering by transverse optical (TO) modes. The enhancement of the forbidden TO phonon scattering suggests poor crystallinity or presence of a crystal orientation other than (100) in the GaAs layer with a hazy surface, while the TO peak is suppressed in the GaAs layer with a specular surface. Weak rings superposed on the streak RHEED pattern as seen in Fig. 3 indicate presence of misoriented

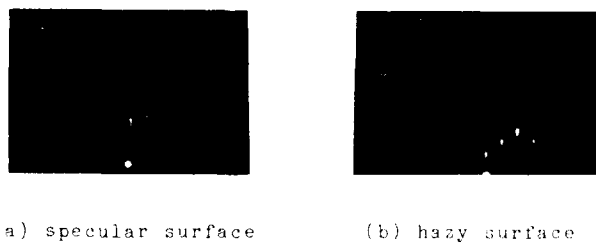


Fig. 3 RHEED patterns of GaAs layers grown on Si at 750°C.

grains in addition to the (100) crystal orientation in the GaAs layer grown on Si at 750°C. All the above results from Raman

spectroscopy and RHEED conclusively support presence of polycrystalline microstructures in the hazy-surface GaAs layer grown at 750°C but not in the specular-surface GaAs layer grown at 750°C and the entire area of the GaAs layer grown at 650°C.

Fig. 4 shows the FWHM of the x-ray rocking curve for the (400) reflection as a function of growth temperature. For GaAs-on-GaAs increase of growth temperature from 650 to 750°C slightly reduces the FWHM but further increase of temperature increases the FWHM. For GaAs-on-Si, a significant reduction of the FWHM is seen with increasing growth temperature from 650 to 700°C. The overall crystallinity of the GaAs layer on Si improves with increasing growth temperature in the range from 650 to 800°C.

A cross-section TEM micrograph in Fig. 5 reveals more threading dislocations reaching the surface of the GaAs layer grown on Si at 750°C, while the dislocations near the surface of the GaAs layer grown on Si at 800°C have been apparently annealed during the growth. Stacking faults and microtwins are also observed in the GaAs layers grown at 650, 700 and 750°C but very few or none in the GaAs layer grown at 800°C. Since the cleaning procedure is the same for all the samples, stacking faults and microtwins are not caused by poor surface cleaning. Some stacking faults and microtwins in the GaAs layer grown at 750°C extend from the GaAs/Si interface to the surface as seen in the TEM micrograph. In general the observations from the TEM micrographs agree with those from the x-ray FWHM.

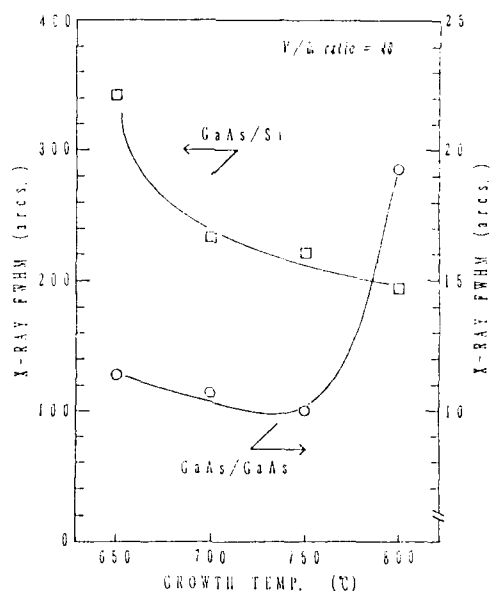
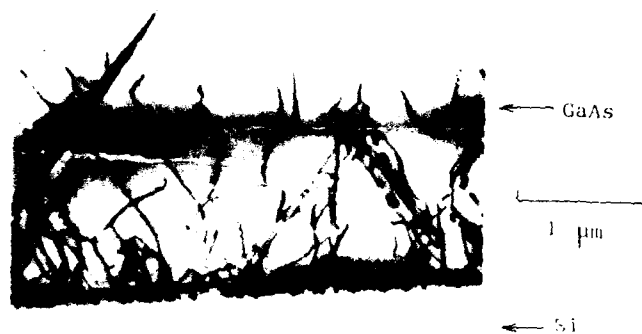
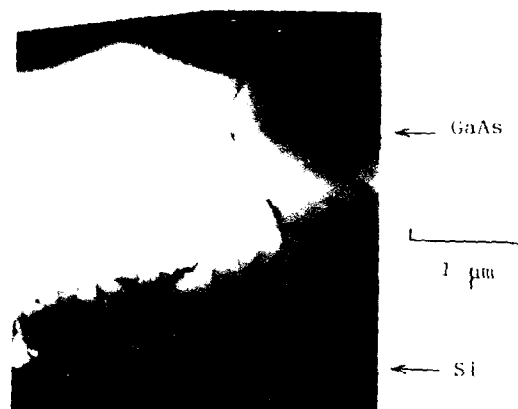


Fig. 4 X-ray rocking curve FWHM of GaAs-on-Si vs. growth temperature.



(a) 750°C



(b) 800°C

Fig. 5 TEM cross-section of GaAs layers grown on Si at 750 and 800°C.

THREE-STEP GROWTH

As discussed, lowering growth temperature improves surface morphology but degrades crystallinity of MOCVD-grown GaAs-on-Si, while growth temperature does not significantly affect surface morphology of GaAs-on-GaAs. This suggests that the GaAs layer on the low-temperature nucleation layer on Si must be grown at relatively low temperature to obtain good surface morphology. The three-step growth process is proposed for this purpose. A 1 μm-thick GaAs layer is grown at 650°C on the low-temperature nucleation layer and then a 2 μm-thick GaAs layer is grown at

750°C. These thicknesses of the GaAs layers grown at 650 and 750°C are those optimized for the crystallinity and the surface morphology. The process avoids a direct contact of the GaAs layer grown at 750°C with the nucleation layer and brings a GaAs top layer grown at higher temperature. As a result, the GaAs layer grown on Si by this process has a low x-ray FWHM, 180 arcs and good morphology (Fig. 6) uniformly.



Fig. 6 Surface morphology of GaAs-on-Si grown by the three-step growth process.

CONCLUSIONS

Effects of growth temperature on MOCVD-grown GaAs-on-Si have been studied. Crystallinity improves but surface morphology degrades with increasing growth temperature. The trade-off between crystallinity and surface morphology has been eliminated by the proposed three-step growth process. The GaAs-on-Si grown by the three-step growth process has good surface morphology and crystallinity.

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CHARACTERIZATION OF GaAs/Si/GaAs HETEROINTERFACES

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ABSTRACT

Transmission electron microscopy of GaAs grown on Si for metal-semiconductor-metal photodetectors is presented in this paper. Two kinds of samples are compared: GaAs grown on a 15 Å Si epilayer grown on GaAs, and GaAs grown at low temperature (300°C) on Si substrates. It is shown that the GaAs epitaxial layer grown on thin Si layer has reverse polarity to the substrate (antiphase relation). Higher defect density is observed for GaAs grown on Si substrate. This higher defect density correlates with an increased device speed, but with reduced sensitivity.

INTRODUCTION

The motivation for this work was the desire to fabricate ultra-high-speed metal-semiconductor-metal (MSM) photodetectors. Optimum performance of such detectors requires a combination of high sensitivity with short minority carrier lifetime. In earlier work, neutron-damaged GaAs has been used in MSM devices [1,2], with sensitivity sacrificed for increased speed. Our approach was to use molecular beam epitaxy (MBE) to grow GaAs on Si substrates. The planar thin film geometry, in principle, allows good carrier mobility parallel to the GaAs/Si interface, while the expected high density of crystal defects at this interface should reduce carrier lifetime.

EXPERIMENTAL

Two different types of samples were grown in a Varian molecular beam epitaxy (MBE) system. In the first type of samples, a thin layer (15 Å) of Si was grown on a GaAs buffer layer grown on GaAs substrate, followed by a 1 µm thick layer of GaAs. The thin Si epilayer was grown using a Si doping cell at a nominal temperature of 600°C, with a substrate temperature of 600°C. Growth of the final 1 µm GaAs epilayer was initiated at 425°C at approximately 0.1 µm/hr and slowly ramped up to 1 µm/hr at 600°C. The second types of samples were prepared by growing low temperature (LT) GaAs epilayers on Si substrate at 300°C. All substrates were at nominal (001) orientation.

Cross-section samples of both types of material were studied using a JEOL 200CX electron microscope with a point-to-point resolution of 2.4 Å and the Atomic Resolution Microscope (ARM) at Berkeley with a resolution of 1.7 Å. In each case, cross-sections were examined with [110] and [100] parallel to the electron beam.

RESULTS

Transmission electron microscopy revealed many defects in the first type of samples, GaAs grown on Si (15 Å) deposited on epi-GaAs substrate (Figs. 1-3). Defect types and their density were similar to that in GaAs grown directly on Si substrates, e.g. misfit dislocations, stacking faults, microtwins and threading dislocations [3,4]. The number of stacking faults in the GaAs epilayer was much higher than in typical two-step growth GaAs layers grown on bulk Si, with typical spacings between stacking faults of 15nm.

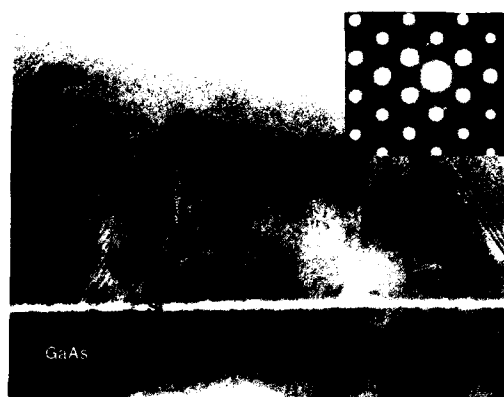


Fig. 1: High resolution image of the GaAs/Si/GaAs interface taken in $\langle 110 \rangle$ projection. Note high density of microtwins and stacking faults present in the GaAs epilayer.

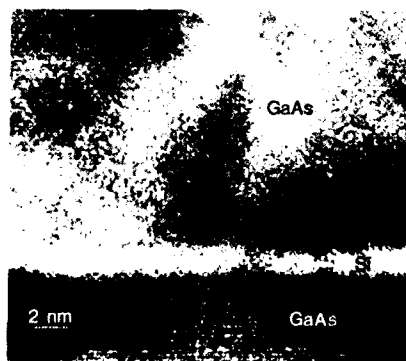


Fig. 2: High resolution image of the GaAs/Si/GaAs interface taken in $\langle 100 \rangle$ projection. Steps at both interfaces are visible.

Many antiphase boundaries were observed in these layers as well. To ensure that the observed contrast was associated with antiphase boundaries the sample was placed in a Phillips 400T electron microscope where convergent beam electron diffraction (CBED) patterns were taken in particular domains. The sample was tilted to fulfill the condition of coupling two odd reflections with the (200) reflection in order to observe the black (or white) cross in the (200) disc.

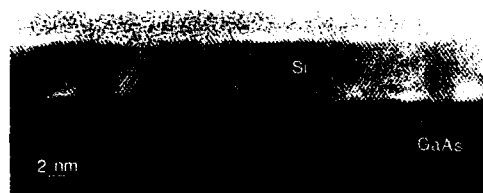


Fig. 3: High resolution image of the Si/GaAs interface taken in $\langle 110 \rangle$ projection. Thickness of the Si layer is ~ 6 nm. Note high density of stacking faults present in the Si epilayer and lack of pure edge type of misfit dislocations at the interface.

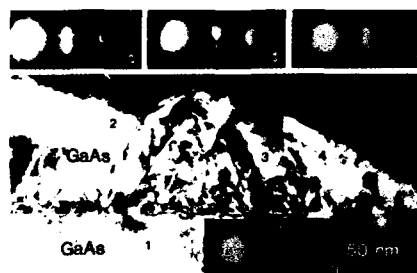


Fig. 4: Dark field image of the GaAs/Si/GaAs interface. Numbers 1, 2, 3 and 4 indicate the position of the electron beam where convergent beam diffraction pattern was taken in order to determine the polarity of the crystal. CBED patterns show the reverse polarity (see the crosses in the (200) disc) of the GaAs epilayer. Only the grain 3 has the same polarity as the underlying epi-GaAs.

This CBED method was previously successfully applied to check the crystal polarity [5,6]. A black cross was observed in the (200) disc in the GaAs buffer layer (Fig. 4 - beam position 1), which changed to white when the beam was placed in the GaAs epilayer above the Si layer (Fig. 4- beam positions 2 and 4). Only in a few places (beam position 3) was the polarity of the domain identical with that of the substrate. This observation shows a preferred GaAs-Si interface orientation which is consistent with preferential bonding of As to Si [7], although some domains have the same polarity as the underlying GaAs buffer layer. The defects in the final GaAs epilayer appeared to originate at the upper GaAs-Si interface. TEM revealed steps at both the GaAs-Si and Si-GaAs interfaces.

It is very difficult without image processing to decide if some misorientation of this thin Si layer took place, because the Si layer is visible in most cases only as a white band. This white band may be associated with impurities during growth or contamination during TEM sample preparation. When a 60 Å thick Si layer was grown, lattice imaging of the layer was very easy, and no white band was observed (Fig.3). This 60 Å thick Si layer was highly defective. Stacking faults with one partial dislocation at each interface were observed. This study shows that even when only a few monolayers of Si are grown, the differences in lattice constant and thermal expansion coefficient of Si and GaAs cause a high defect density in the top GaAs epilayer.

This GaAs-Si-GaAs structure was compared to low-temperature epitaxial GaAs heteroepilayers grown on Si. The latter had a high density of defects, mostly stacking faults, dislocations and antiphase domains (Figs. 5, 6). It was observed that any irregularities at the interface, such as surface contamination, could lead to the formation of small grains (polycrystalline material) and stacking faults (Figs. 6 and 7).



Fig. 5: Bright field image of GaAs deposited at 300°C (LT) on Si substrate. Note high density of microtwins, stacking faults and dislocations present in the GaAs epilayer.



Fig. 6: High-resolution image of the GaAs (LT) on Si interface taken in <110> projection. Note that interface contamination is the source of polycrystallinity and other defects.



Fig. 7: High-resolution image of the GaAs (LT) on Si interface taken in $\langle 110 \rangle$ projection. Note lack of pure edge type of misfit dislocations at the interface.

Annealing of the LT-GaAs structures at 600°C did not reduce dislocation density significantly but drastically reduced stacking fault density (Figs. 8 and 9). It was observed that dislocations in postannealed samples were more tangled than in as-grown samples.



Fig. 8: Bright field image of the GaAs deposited on Si substrate at 300°C (LT) and annealed at 600°C with As overpressure. Note that density of microtwins and stacking faults drastically decreased, but many tangled dislocations are present in the GaAs epilayer.

Comparing these two types of materials, a higher defect density, especially close to the interface was observed for the LT GaAs grown on Si substrate. This correlated with an increased device speed but with very low sensitivity. MSM detectors on these epilayers showed autocorrelation response times under 50 ps [8]. The annealing step did not significantly effect the response time, but the relative sensitivity of the photoconductors increased significantly after annealing.



Fig. 9: High-resolution image of the GaAs (LT) on Si interface taken in $\langle 110 \rangle$ projection. Microtwins and stacking faults found at the interface only in some areas.

CONCLUSIONS

A study of the GaAs/Si/GaAs structures used for MSM detectors shows that the GaAs epilayer grown on 15 Å thick Si deposited on epi-GaAs substrate has reverse polarity to the substrate (*antiphase relation*), which is consistent with preferential bonding of As to Si. The number of defects formed in GaAs grown directly on a (001) Si substrate is high compared to the GaAs/Si/GaAs(001) structure, and this correlates with increased device speed.

Annealing at 600° C with As overpressure does not significantly reduce dislocation density or change the device speed, although it does increase the overall device quantum efficiency, which can probably be related to a decrease in the density of stacking faults.

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GROWTH OF GaAs ON Si USING AlGaP INTERMEDIATE LAYER

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ABSTRACT

We have studied heteroepitaxial growth of GaAs on Si using an $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer in an atmospheric-pressure metal organic chemical vapor deposition (MOCVD) reactor. The crystallinity of the GaAs layer depends on AlP composition(x) of the intermediate layer. The best crystal quality of GaAs layer is obtained when the AlP composition(x) of the intermediate layer is close to 0.5. The X-ray FWHM of 180 arcs and the etch pit density (EPD) of $2.5 \times 10^7 \text{ cm}^{-2}$ were obtained in this GaAs/AlGaP/Si structure.

INTRODUCTION

GaAs-on-Si has been of a great interest for its application to combine optical and high-speed GaAs devices with Si large scale integrated circuits. Si substrate has many advantages of large area, high quality, low cost, mechanical strength and high thermal conduction as compared with LEC GaAs substrate. Even though Salerno et al.[1] reported successful growth of GaAs-on-Si with large area (6 inch diameter) and high uniformity, the quality of GaAs layer grown on Si substrate is not satisfactory yet for practical applications. Difficult problems to be solved are tensile stress and high dislocation density in the GaAs layer which are due to the difference of thermal expansion coefficient and the large lattice mismatch, respectively. The density of dislocations in GaAs layer is more than 10^8 cm^{-2} by the conventional two-step-growth. The order of 10^6 cm^{-2} can be achieved by use of strained layer superlattice (SLS) and/or by use of thermal cycle.[2,3]

Soga et al. first proposed AlGaP(or GaP) and SLS intermediate layers for GaAs-on-Si, and high quality GaAs layer was grown on Si.[4,5] In this study we have grown GaAs on Si substrate using an $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer and discuss effects of the intermediate layer on crystallinity of GaAs layer.

EXPERIMENTAL

All layers were grown by metal organic chemical vapor deposition (MOCVD). The MOCVD apparatus consists of horizontal reactor with an RF heated susceptor at atmospheric pressure. The Ga, Al, As, and P sources were trimethylgallium (TMG), trimethylaluminum (TMA), AsH₃(100%), and PH₃(100%), respectively. The carrier gas was palladium-diffused H₂ with a flow rate of 6 slm. Si substrates used in this study were n-type (100) surface tilted towards [011] by 2 degrees. The Si substrate was degreased in organic solvents and then cleaned using 4H₂SO₄ + H₂O₂ and HF + H₂O solutions. Before the growth, the substrate was heated in H₂ atmosphere at 1000°C for 10 min to remove native oxide on the substrate. After the substrate heat treatment, the susceptor was cooled down to 900°C and a 50nm-thick Al_xGa_{1-x}P layer was grown on Si substrate with V/III ratio of 100. For the Al_xGa_{1-x}P growth, total mole fraction of group III element sources ([TMA]+[TMG]) was maintained at 1.4×10^{-4} and the ternary alloys of Al_xGa_{1-x}P were grown from x=0 to 1 by changing their mole ratio ([TMA]/[TMG]). A 3 μm-thick GaAs layer was grown on the Al_xGa_{1-x}P/Si at 700°C with V/III ratio of 40. The growth rate of GaAs layer was 50 nm/min.

The crystallinity of GaAs layers were characterized by Nomarski microscope, double crystal X-ray diffraction (400) rocking curve measurement, low temperature photoluminescence (PL) measurement, and etch pit density (EPD) revealed by molten KOH. The intermediate layers were studied by transmission electron microscopy (TEM). To evaluate the growth rate of the Al_xGa_{1-x}P on Si, we have grown about 1 μm-thick of Al_xGa_{1-x}P layer on Si substrate with various AlP compositions. Solid compositions of Al_xGa_{1-x}P ternary alloys were determined by Auger Electron Microscopy (AES).

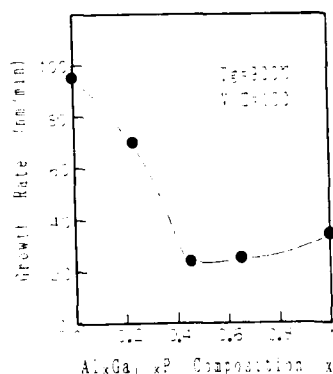


Fig.1 Growth rate of Al_xGa_{1-x}P layer grown on Si substrate as a function of AlP composition x.

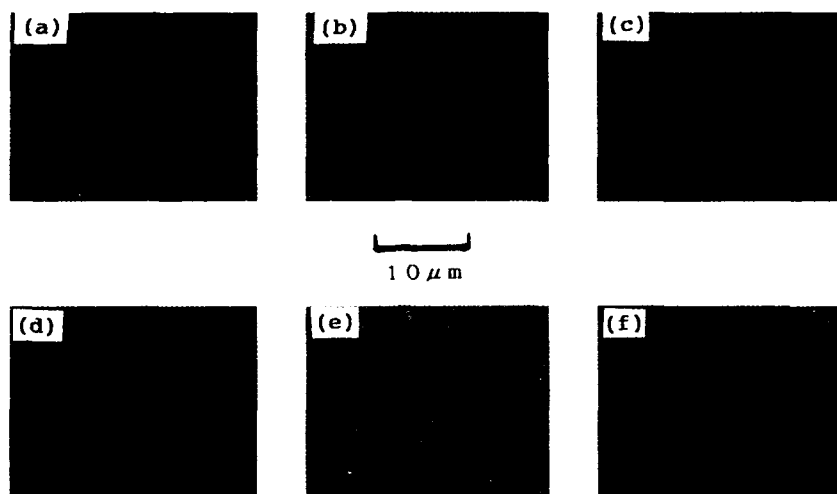


Fig.2 Photographs of GaAs layers grown on Si with various $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers. The AlP composition(x) of the intermediate layers are as follows. (a) $x=0$, (b) $x=0.23$, (c) $x=0.45$, (d) $x=0.65$, (e) $x=0.84$, (f) $x=1$

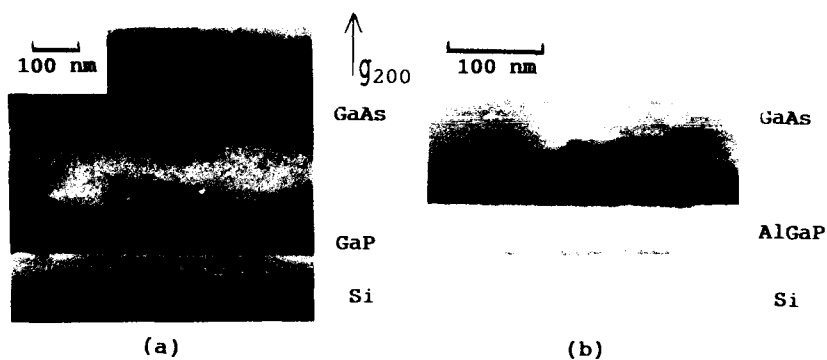


Fig.3 Cross-section TEM micrographs of GaAs on Si with GaP intermediate layer, and $\text{Al}_x\text{Ga}_{1-x}\text{P}$ ($x=0.55$) intermediate layer.
(a) GaAs/GaP/Si (b) GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{P}$ /Si ($x=0.55$)

RESULTS AND DISCUSSION

Fig.1 shows the growth rate of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ on Si substrate. The growth rate gradually decreases with decreasing AlP composition(x) from AlP and it drastically increases when x reaches to 0.45. Fig.2 shows the surface

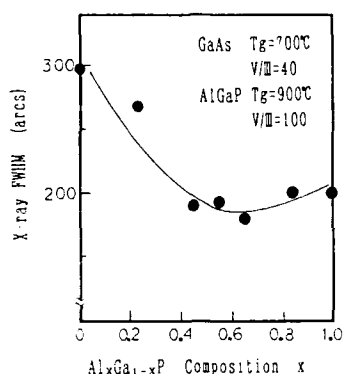


Fig.4

The FWHM of double crystal x-ray rocking curve as a function of AlP composition in $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer.

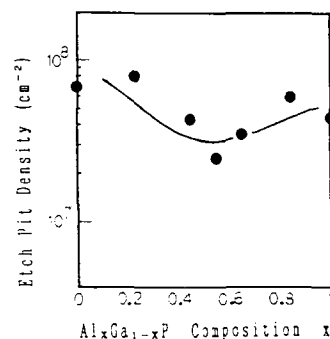


Fig.5

Etch pit density of GaAs layer on Si as a function of AlP composition(x) in $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer.

morphology of GaAs on Si using the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers of various AlP composition(x) from $x=0$ (i.e. GaP) to $x=1$ (i.e. AlP). With the GaP intermediate layer, surface of the GaAs layer shows scaly morphology with "treads and risers". When x is greater than or equal to 0.45, surface morphology becomes very smooth.

To understand the above results, the samples were analyzed by cross-section TEM. The TEM micrographs in Fig.3 represent GaAs on Si with $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer ($x=0$ (GaP) and 0.55). It is clearly seen that the growth of GaP layer on Si is island-like, whereas the growth of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ ($x=0.55$) layer is planar. The growth of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer with the AlP composition(x) greater than 0.45 is planar and it does not change drastically with x . The dependence of both the growth rate of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ on Si and surface morphology of GaAs layer on AlP composition(x) well corresponds to the change of growth mode of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ on Si. The $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layer with low AlP composition(x) grows three-dimensionally. When AlP composition(x) exceeds 0.45, $\text{Al}_x\text{Ga}_{1-x}\text{P}$ growth mode changes into quasi-two-dimensional. The initial stage of nucleation is not clear yet from this observation, but we hypothesize that $\text{Al}_x\text{Ga}_{1-x}\text{P}$ grows at very large number of nucleation sites on Si and covers the Si surface very rapidly. As a result, the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layer grows quasi-two-dimensionally. On the other hand the growth of GaP is three-dimensional even when its thickness reaches to 50 nm. George et al.[6] discussed detail understandings for the above results.

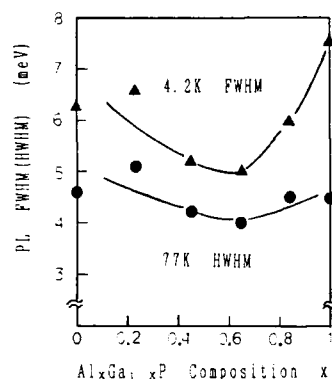


Fig.6

FWHM(4.2K) and HWHM(77K) of PL emission peak from GaAs on Si as a function of AlP composition(x) in $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer.

(HWHM : half width at half maximum)

Fig.4 shows the FWHM double crystal X-ray of the (400) reflection peak from the rocking curve of GaAs on Si as a function of AlP composition(x) in $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer. The FWHM is greatly affected by the composition(x) of the intermediate layer. As the minimum value of 180 arcs is obtained when x is close to 0.5, the crystal quality improves when composition(x) approaches to 0.5. Fig.5 shows dependence on etch pit density (EPD) of GaAs layer of AlP composition(x) in the intermediate layer revealed by molten KOH etching. The EPD has dependence on the composition(x) similar to that seen in Fig.4, and the value of $2.5 \times 10^7 \text{ cm}^{-2}$ is obtained when x is 0.55. We also studied optical properties of GaAs on Si by low temperature photoluminescence(PL) measurements at 77 K and 4.2 K. In the 77 K PL, it is difficult to evaluate the FWHM of band edge emission peak because the peak is splitted into two peaks which are due to the split of hole bands by tensile stress in the GaAs layer. The crystallinity was assessed by the HWHM (half width at half maximum) of the band-emission peak in 77 K PL and by the FWHM of the exciton-related peak in 4.2 K PL. The carrier concentration of GaAs layer, $1 \times 10^{17} \text{ cm}^{-3}$ by C-V measurements, dose not change with the composition(x). The HWHM and FWHM are shown in Fig.6. It suggests that the crystallinity improves when x approaches to 0.5. As shown in Ref.[7], characteristics of Schottky barrier diodes also show similar dependence on the composition(x). The ideal factor of I-V characteristics is 1.06 when x is close to 0.5.

All the above results indicate that crystallinity of GaAs layer is strongly affected by the composition(x) of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer. The best crystallinity is obtained when x is around 0.5. From the study of GaAs/AlGaP/Si structure, the ternary alloy is found to be appropriate as an intermediate layer than GaP or AlP.

CONCLUSIONS

GaAs was successfully grown on Si substrate using an $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer by atmospheric-pressure MOCVD. The growth mode of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layer grown on Si substrate changes from three-dimensional island growth to quasi-two-dimensional planar growth with increasing AlP composition(x). The dependence of both surface morphology of a GaAs layer and the growth rate of an $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layer on Si substrate with AlP composition(x) well corresponds to the change of the growth mode of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layer on Si revealed by TEM study. Crystallinity of the GaAs layer is greatly affected by the composition(x) of the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layer. When AlP composition(x) is close to 0.5, the crystallinity of GaAs is the best in the GaAs/AlGaP/Si structure as observed by X-ray, EPD, and PL measurements. The X-ray FWHM of 180 arcs and the EPD of $2.5 \times 10^7 \text{ cm}^{-2}$ were obtained. Further improvement is expected with SLS and thermal annealing.

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NUCLEATION STUDIES OF LATTICE MATCHED AND MIS-MATCHED HETEROEPITAXIAL LAYERS USING THE $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{P}/\text{Si}$ SYSTEM.

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ABSTRACT

Heteroepitaxial growth of GaAs on Silicon substrates is being actively pursued, since this technology offers numerous potential benefits in terms of optoelectronic and high speed devices. However a complete understanding of the fundamental causes for film properties such as surface morphology and crystal quality is still lacking at the present time. We present here the results of a study of GaAs grown on Silicon substrates using $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers. This system offers the advantage of studying the effects of surface properties and bulk properties of heteroepitaxial films separately. Surface and interface properties are shown to be the dominant factors in the growth of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ on Si, where the lattice match between the two materials is very good. For low Al mole fractions the layers tend to form islands indicative of 3D growth, whereas for $x > 0.4$, the layers are planar indicative of 2D growth. Bulk properties such as the lattice constant mismatch are presumed to play a key role in the growth of GaAs on $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers, where it is shown that the GaAs still has an island type nucleation phase, even though surface and interface factors such as contamination and polar-on-nonpolar growth are avoided. In addition the nucleation of the GaAs on the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers appears to be modified by the nature of the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layer i.e. whether the intermediate layer is in the form of islands or a planar layer. The final surface morphology and the crystalline quality of $3\mu\text{m}$ GaAs films grown on $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers can be correlated to the initial nucleation.

INTRODUCTION

Gallium Arsenide on Silicon heteroepitaxy is being actively pursued [1,2,3] because of the many potential benefits of incorporating specialised GaAs high speed and optical devices on Silicon VLSI chips. However problems such as high defect densities, tensile stress and poor surface morphology still exist and a complete understanding of the fundamental causes of these problems is still lacking.

The growth of good quality Gallium Arsenide on Silicon substrates is complicated by several problems. These problems can be divided into two broad classes. Those relating to surface or interfacial properties and those related to bulk properties. Among surface and interface properties, we can include such factors as: the difference in free surface energy densities for GaAs and Silicon, substrate surface modification (either by contamination or by some form of pre-coating), growth of polar material on non polar substrates and interfacial Ga-Si or As-Si bonds versus Ga-As bonds. As for bulk properties, we can consider bulk free energy considerations which determine the concentration of nuclei at a given temperature and also the large difference in lattice parameters giving rise to high compressive stresses in the growing nuclei. An understanding of the initial nucleation and growth is crucial to the control of film properties such as surface morphology, defect densities, doping and stress.

In this study, the growth of Gallium Arsenide on Silicon using $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate layers is investigated. The $\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{P}/\text{Si}$ system offers the unique opportunity of examining both lattice matched ($\text{Al}_x\text{Ga}_{1-x}\text{P}/\text{Si}$) and lattice mismatched

systems ($\text{GaAs}/\text{Al}_x\text{Ga}_{1-x}\text{P}$) simultaneously. In the first instance, the role of surface and interface properties in the growth of a lattice matched heteroepitaxial layer can be studied. In the second case, purely bulk effects such as those listed above, are expected to influence the growth process, since the growth of GaAs occurs on a clean polar substrate, grown in situ. Prior work done by Soga et al [4] has shown that good quality GaAs films can be grown on Si using GaP intermediate layers. Noto et al [5] have shown that by using a ternary compound of $\text{Al}_x\text{Ga}_{1-x}\text{P}$, as the intermediate layer, the surface morphology of the GaAs films can be improved considerably.

EXPERIMENTAL

The heteroepitaxial layers were grown by an MOCVD process. The Si substrates used were miscut 2 degrees off from the [100] normal towards [011]. Substrates were degreased, oxidized using a mixture of $\text{H}_2\text{SO}_4 + \text{H}_2\text{O}_2$ for 4 min to remove carbon contamination and then dipped in a $\text{HF} + \text{H}_2\text{O}$ solution, prior to introduction into the growth chamber. The substrates were heated at 1000°C for 10 min in a reducing ambient to remove surface oxide. The temperature was then lowered to 900°C where 500\AA of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ was then deposited. The mole fraction of Al (x) was varied from $x=0$ to $x=1.0$ to study the role of Al content in the intermediate layers. The temperature was subsequently lowered to 700°C where GaAs growth was initiated. The GaAs was grown to a thickness of $3\mu\text{m}$.

For the initial nucleation studies, the same procedure, as listed above was followed except that the thickness of the Gallium Arsenide was reduced to 100\AA and two compositions were chosen for the intermediate layers, namely GaP and $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$.

The surface morphology of the $2\mu\text{m}$ layers was examined using Nomarski microscopy and the crystal quality was evaluated by cross-section TEM. The initial nucleation samples were studied using both plan view and cross-section TEM.

RESULTS AND DISCUSSION

Nomarski micrographs of the surface morphology of the $3\mu\text{m}$ GaAs layers grown on $\text{Al}_x\text{Ga}_{1-x}\text{P}$ intermediate buffer layers (Fig 1) shows an improvement in the surface morphology with increasing Al content in the intermediate layers.

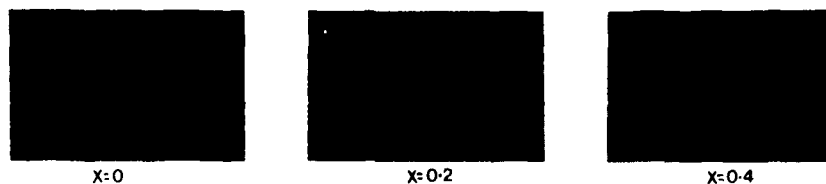


Fig 1. Surface morphology of $3\mu\text{m}$ GaAs layers grown on $\text{Al}_x\text{Ga}_{1-x}\text{P}$ buffer layers

Cross-section TEM micrographs of the $3\mu\text{m}$ GaAs layers are shown in Figs 2a-c. Fig 2a shows the GaAs film grown on a GaP intermediate layer. The GaP appears to form islands on the Silicon surface. The addition of Al to the GaP appears to reduce the island forming tendency (Fig 2b), and tends to promote more two dimensional growth. For layers with $x > 0.2$ in the ternary $\text{Al}_x\text{Ga}_{1-x}\text{P}$ (Fig 2c) the intermediate layers are planar, without

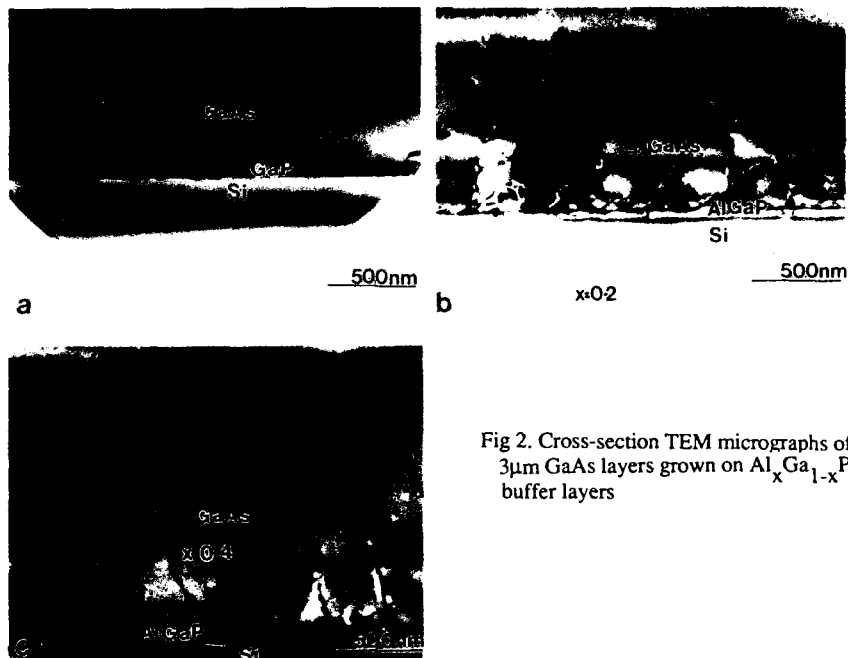


Fig 2. Cross-section TEM micrographs of $3\mu\text{m}$ GaAs layers grown on $\text{Al}_x\text{Ga}_{1-x}\text{P}$ buffer layers

any evidence of island formation. The Si substrate interfaces for all the intermediate layers appear to be free from misfit dislocations and no threading dislocations are to be seen within the intermediate layers. However misfit dislocations are generated between the intermediate layers and the overgrown GaAs. In fact some loops appear to move down from the GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{P}$ interface into the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layers. The average crystal quality has been evaluated by Noto et al [5], using X-Ray diffraction and has been shown to improve with the Al content of the intermediate buffer layers.

Plan view and cross-section TEM were performed on the buffer layers grown for the nucleation study. The plan view micrographs (Figs 3a,b) show the GaAs as dark

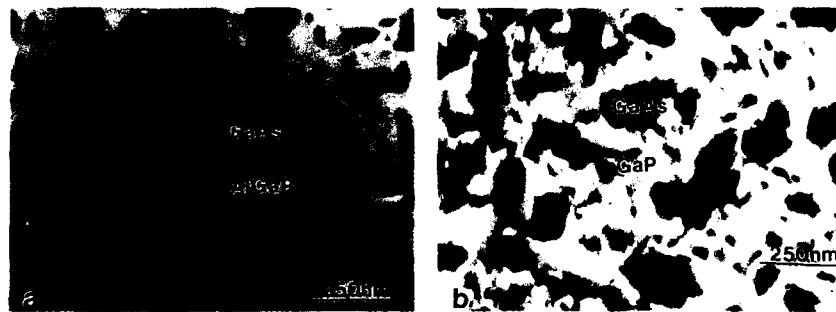


Fig 3. Plan view TEM micrographs showing nucleation of GaAs layers on AlGaP (a) and GaP (b) buffer layers

islands sitting on a bright background. Moire fringes are seen within the islands due to the double diffraction effects from the GaAs and the $\text{Al}_x\text{Ga}_{1-x}\text{P}/\text{Si}$ layers. The shapes of the GaAs islands grown on the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ layer (Fig 3a) exhibit a definite relationship to the substrate orientation, and appear to form long rectangular needles along the two $\langle 011 \rangle$ directions on the surface. There does not appear to be a preference for either one of the $\langle 011 \rangle$ directions as one might expect since the Silicon substrate is tilted towards a $\langle 011 \rangle$ direction. There is a distribution both in the size and the spacing between the islands with many closely spaced small islands being present in between the large islands. On the GaP intermediate layer (Fig 3b) the islands are more equiaxed, larger and further apart from each other than those on the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ intermediate layer. Table I compares the island densities obtained for the two types of buffer layers.

Table I

Island distribution for AlGaP and GaP intermediate layers

	Large island density ($\#/\mu\text{m}^2$)	Small island density ($\#/\mu\text{m}^2$)
GaAs/AlGaP/Si	29	102
GaAs/GaP/Si	17	19

Large islands: $> 500\text{\AA} \times 1000\text{\AA}$

Cross-section TEM pictures of the nucleation study samples show that on the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ (Fig 4a), intermediate layer, the GaAs islands grow with well defined (111) facets inclined at 45 degrees to the substrate surface. The islands exhibit dark contrast in comparison with the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ intermediate layer due to the high concentration of defects present within them. Misfit dislocations are formed at the GaAs/ $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ interface with some loops propagating into the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ intermediate layer. The interface between the $\text{Al}_{0.4}\text{Ga}_{0.6}\text{P}$ and the Silicon substrate appears to be dislocation free. On the GaP intermediate buffer layers (Fig 4b) however, the GaAs nucleation appears to be modified by the nature of the GaP surface. The GaAs prefers to nucleate in the wells created at the junctions of the GaP islands behaving very much like a liquid, that has been poured over a rough surface.



Fig 4. Cross-Section TEM micrographs showing nucleation of GaAs layers on AlGaP (a) and GaP (b) buffer layers

Thus, this study allows one to learn more about the modes of nucleation and growth that are possible in lattice matched and lattice mismatched systems.

In the case of $\text{Al}_x\text{Ga}_{1-x}\text{P}/\text{Si}$, since the layers have a close lattice match to the substrate, the main factors affecting the growth of the epilayers should be surface and interface related. The absence of Al causes severe island formation, suggesting that nucleation occurs at certain preferential sites on the substrate. The addition of Aluminum appears to induce more homogeneous nucleation, leading to planar growth. A possible explanation for this behaviour assuming we neglect sheet charge formation due to polar/non polar effects, can be the following. The native oxide of Silicon is not completely removed by the preclean procedure and results instead in localized areas where the oxide has broken, exposing fresh Si surface. The ambient during the growth of GaP is not able, to reduce this native oxide and since the surface mobilities are high enough, at the growth temperature, growth proceeds at these isolated nucleation sites. By increasing the Al content of the layer, the nucleation becomes more uniform since Al is a strong getter for oxygen and is capable of reducing SiO_2 at the growth temperature (ref thermodynamical data such as the well known Ellingham diagram). Hence the residual contamination of the Si surface, is not very critical for the growth of $\text{Al}_x\text{Ga}_{1-x}\text{P}$, for $x > 0.2$.

The growth modes of GaAs on $\text{Al}_x\text{Ga}_{1-x}\text{P}$ surfaces are interesting, as well. Since the growth occurs in situ on a compound semiconductor it is possible to exclude many variables such as the effects of polar/non polar growth and contamination and concentrate instead on the role of bulk properties, namely the large lattice constant mismatch (~4%). The TEM observations indicate the growth mode of GaAs on planar layers of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ to be 3d (island formation) rather than a 2d layer by layer growth. Thus the coherent strain energy is high enough, to shift the equilibrium energy balance for nucleation in the direction of increased surface energy. The strong orientation relationship of the shape of the GaAs islands on the planar $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layers can probably be explained by the fact that on (001) surfaces of Si and perhaps $\text{Al}_x\text{Ga}_{1-x}\text{P}$, atomic steps occur along the two $\langle 110 \rangle$ directions. These steps could then provide the preferential nucleation sites for the growing GaAs layers. From this one can conclude that the usual 3d nucleation of GaAs/Si is not due to the polar/non polar growth, but rather due to the high strain energy.

In the case of the growth of GaAs on GaP intermediate buffer layers, the nucleation mode is modified by the nature of the GaP surface. Since the GaP exists as islands, on the Silicon surface, the surface of the GaP layer is very rough, having many "hills and valleys". Since we have shown already, that the GaAs prefers an island type 3d nucleation mode, even on clean polar substrates, the preferential nucleation sites on the GaP layer appear to be the valleys in between the GaP islands. The minimum free energy condition in this case, includes the reduction of the GaP surface energy as well.

The correlation between the initial nucleation modes of the GaAs and the final film properties is very clear. When the GaAs islands are on average larger and further apart, one can expect that, at coalescence the film surface will be more rough and faceted, than in the case where the islands are smaller and more numerous. This expectation is supported by the surface morphology observations.

Cross-section TEM observations indicate that misfit and threading dislocations are generated mainly at the GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{P}$ interface. With this information, one can then deduce that the threading dislocation density of the GaAs grown on the GaP intermediate layers should be higher than in the case of the planar $\text{Al}_x\text{Ga}_{1-x}\text{P}$ layers. This is not only because of the increased interfacial area, but also because misfit dislocations formed on the side walls of the GaP islands may not be as sessile as the pure edge dislocations generated on the (001) interfaces. In addition, the GaAs nuclei, being larger and farther apart on the GaP layer may tend to form low surface energy facets, resulting in more defects being generated at the island boundaries at coalescence. Thus, the above could be a possible explanation for the improvement in crystallinity as measured by X-Ray diffraction.

CONCLUSIONS

Lattice matched nucleation in the $\text{Al}_x\text{Ga}_{1-x}\text{P}/\text{Si}$ system appears to be strongly modified by the nature of the substrate surface, with nucleation modes changing from island type to planar, with increasing Al content.

Lattice mismatched nucleation on the other hand, is always 3 dimensional for large mismatch (~4%) and the nucleation can be modified by the nature of the surface.

Thick film properties such as surface morphology and defect density are shown to be dependent on the initial nucleation mode.

The use of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ buffer layers appears to be a promising approach towards the development of low defect GaAs/Si heteroepitaxy.

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PART VI

Heteroepitaxy on Silicon II

ANTIPHASE DEFECT REDUCTION MECHANISM IN MBE GROWN GaAs ON Si

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ABSTRACT

It is shown that antiphase boundary (APB) is annihilated during the growth, by monitoring the surface with reflection high energy electron diffraction (RHEED). The RHEED observation indicates that double domain GaAs changes to single domain within a thickness of 100 nm, while the transition region is estimated to exist within 200 nm from GaAs-Si interface by scanning electron microscope (SEM) observation of etch pits on vicinally polished surface. The self-annihilation mechanism of APB is discussed from these results.

1. INTRODUCTION

Single domain GaAs can be grown on double domain Si(100) substrates by both MBE and metalorganic chemical vapor deposition (MOCVD)[1,2]. The annihilation of double domain has been explained by several models[2-6], but there are few experimental results supporting the model. One of them is that the growth of single domain starts at the initial stage of the epitaxy, within a few monolayers from the substrate[3-5]. In this model atomic steps on the surface play an important role. Ideally there are two types of steps, for which the direction of dangling bonds at the step edge is perpendicular to each other. GaAs preferentially nucleates at one type of step and not at the other type of step. Therefore, in this model, there grows a single domain GaAs at the beginning of epitaxy on the two domain Si substrate. In the other model, APB annihilates gradually with the epitaxial growth[2]. Recently Akiyama et al. reported for MOCVD that a single domain GaAs is obtained by an annealing (600°C, 5 min) of thin (40 nm) buffer layer grown at 500°C and 2 nm/min[7]. The as-grown buffer layer consists of small islands aligned along two directions which are perpendicular to each other. After the annealing, these small islands coalesce and turn to unidirectional islands. The succeeding epitaxy on this buffer layer results in a single domain. This result clearly indicates that in the coalescing process the antiphase boundaries between contacting two islands are moving during annealing at 600°C and they turn to a single domain island. In MBE growth the annihilation mechanism of APB may be different from MOCVD because the growth mechanism itself is different each other. In this paper it is shown that APB is annihilated during the growth, by monitoring the surface with RHEED. SEM observation of etch pits on vicinally polished surface also shows that a double domain changes to a single domain at a thickness within about 200 nm from GaAs-Si interface. A model for the self-annihilation of APB is proposed on the basis of these results.

2. EXPERIMENT

Single domain GaAs has been grown on double domain Si(100) tilted 4° toward [011]. The double domain Si surface is obtained by incomplete annealing at 850°C for 1 min. The amorphous GaAs of 5 nm thick is deposited and then annealed at 350°C for 40 min. By this treatment single crystal GaAs with smooth surface is obtained, and therefore a streak RHEED pattern is observed. The evaluation of the surface superstructure becomes possible by this technique. In the normal two step growth, the RHEED pattern becomes

spotty after the first buffer layer deposition (25 nm, 250°C, 100 nm/min). Therefore detailed evaluation of surface superstructure is impossible. After solid-phase epitaxy of the GaAs, migration enhanced epitaxy (MEE)⁸ at 350°C is employed for growing succeeding 100-nm of GaAs in order to prevent island growth of GaAs. The normal MBE growth at 580°C is used for succeeding growth. The change of double domain structure to single domain is monitored by the RHEED observation during the growth. SEM observation of etch pit on vicinally polished surface is also utilized. The vicinal angle is 0.5°. For the pit observation, molten KOH etching at 350°C is used.

3. RESULTS

Figure 1 shows RHEED patterns at each growth steps. Si surface structure after thermal cleaning (850°C, 1 min) is 2x2 pattern (Fig. 1(a) and (b)), showing that the surface structure is double domain, namely superposition of 1x2 and 2x1. After deposition of 5-nm of amorphous GaAs, RHEED pattern changes to diffusive hollow ones. Succeeding annealing at 350°C for 40 min causes the film to crystallize as shown in Fig. 1(c) and (d)

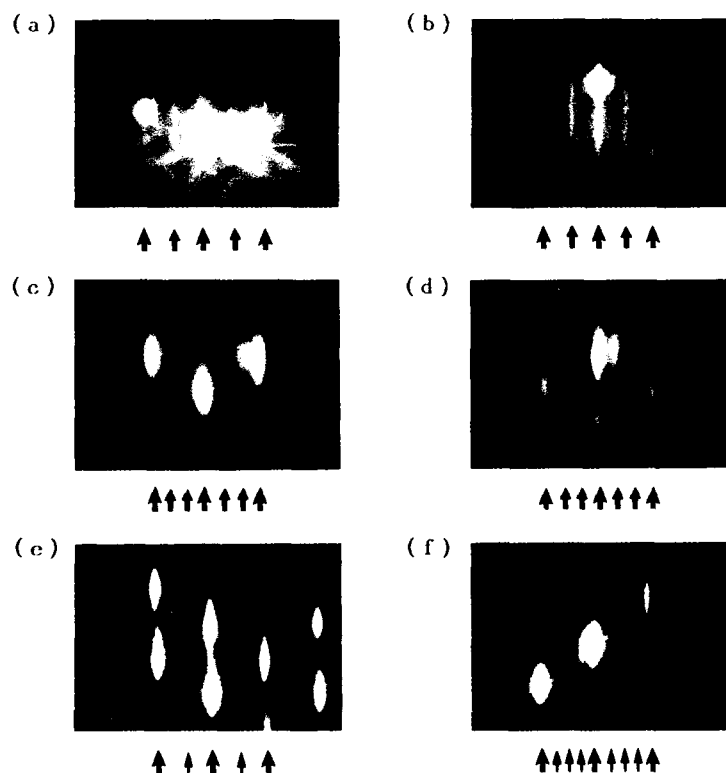
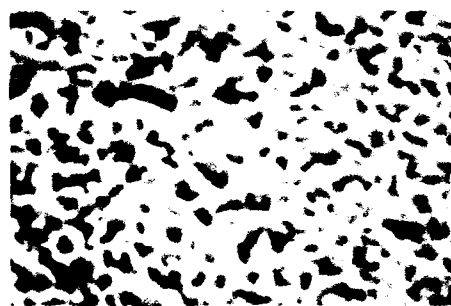


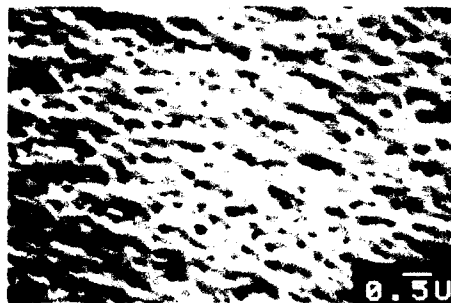
Fig. 1 RHEED patterns at various growth steps. Left row is $[0\bar{1}1]$ azimuth and right row is $[01\bar{1}]$ azimuth. (a) and (b), Si(100) which has two domains. (c) and (d), GaAs crystallized by solid-phase epitaxy of 5-nm amorphous GaAs at 350°C for 40 min. (e) and (f), GaAs grown on (c) and (d) to the thickness of 1.1 μm .

in which streak pattern of 3×3 superstructure is observed. The 3×3 pattern is a mixture of 3×1 and 1×3 , which shows double domain structure. Single domain 3×1 pattern is observed for GaAs grown on GaAs substrate at a particular growth temperature and As/Ga flux ratio.⁹⁾ It is noted that GaAs with thickness of 5 nm grown on double domain Si surface does not change to single domain by this annealing. To prevent island growth, MEE at 350°C is used for the following 100 nm GaAs growth. Then the substrate temperature is raised to 580°C , and $1\ \mu\text{m}$ of GaAs is grown by ordinary MBE method. The RHEED pattern changes from 3×3 to 2×4 single domain pattern with increasing the film thickness. The transition thickness from double to single domain is not clear but is in between 80 and 120 nm. After growth of $1.1\ \mu\text{m}$ GaAs, a clear 2×4 single domain pattern is observed (Fig. 1(e) and (f)). These results show that the APB is self-annihilated during the growth of GaAs, being different from the result of MOCVD[7] in which single domain is obtained by the annealing of the first buffer GaAs layer.

SEM observation of etch pit on vicinally polished surface shows that double domain changes to single domain at a thickness within 200 nm from GaAs-Si interface. Figure 2 shows SEM photographs of etch pits in the region of (a) 0–80 nm and (b) 200–300 nm from the GaAs-Si interface. The left side of the photograph is near the GaAs-Si interface. The etch pits has random direction in Fig. 2(a), showing double domain. On the other hand, in Fig. 2(b) the etch pits align in the same direction, which indicates that



(a) 0 ~ 80 nm



(b) 200 ~ 300 nm

Fig. 2 SEM photographs of etch pit on vicinally (0.5°) polished surface of the sample shown in Fig. 1.

the region more than 200 nm away from the interface is single domain. The APB is annihilated within the film thickness of 200 nm.

4. DISCUSSIONS

4.1 Origin of APB and Si/GaAs interface

APB is generated when there are single atomic height steps on the Si(100) surfaces. Another case is that when atomic arrangement at the Si-GaAs interface is different from place to place, APB is generated even though the Si substrate has single domain surface. The possible orientations of GaAs on Si(001) depend on the atomic arrangement at the Si-GaAs interface. They are GaAs[$\bar{1}10$]/Si[110] and GaAs[110]/Si[$\bar{1}10$]. The interface atomic arrangement is not understood clearly[10]. For As prelayer mode, stable Si-As bonds are formed at the high growth temperature[11], while at the low growth temperature less than 500°C one probable arrangement is that Si is bound to Ga since Si-Ga-As-Ga... stacking agrees with the GaAs orientation grown at the low temperature[12]. However, the actual arrangement seems to be not so simple because XPS results indicate the existence of Si-Ga bonds as well as Si-As bonds[11,13]. Another important factor for the interface atomic arrangement is charge neutrality[14]. Figure 3 shows the probable atomic arrangement which may explain the above experimental results, that is, the dependence of the orientation of GaAs on the growth temperature, coexistence of Si-As and Si-Ga bonds. This atomic re-arrangement model has already been proposed by Harrison et al.[14] and discussed by Kroemer[15] from view point of charge neutrality.

4.2 Self-annihilation mechanism of APB

It is clear that the APB is annihilated during the growth of GaAs from

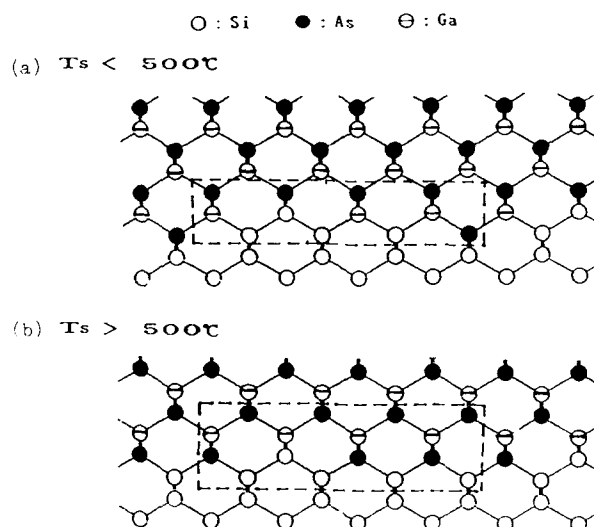


Fig. 3 The atomic re-arrangement which achieve charge neutrality at the interface and can explain the experimental results of the GaAs orientation to Si and coexistence of Si-As bonds and Si-Ga bonds. (a) Low temperature mode. (b) High temperature mode.

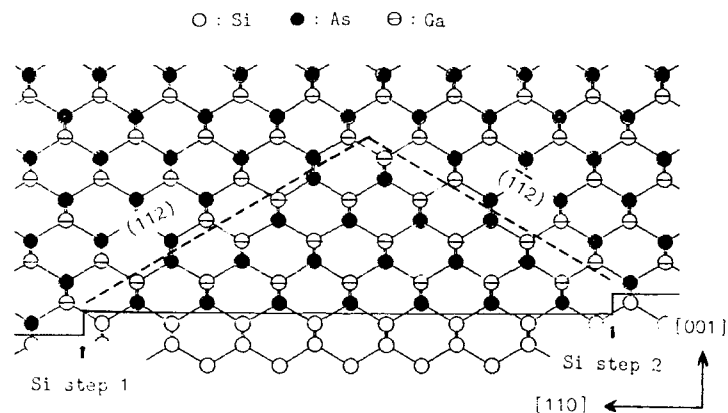


Fig. 4 A model of self-annihilation of APB.

the results in the previous section. For MOCVD, a single domain GaAs is obtained by the annealing of the buffer GaAs layer[7]. It is very important to form very small islands during the initial growth. Once large islands are formed, it requires so large energy to align in the same direction that single domain GaAs can not be obtained. On the other hand, in our experiment the annealing of amorphous GaAs layer (5 nm) at 350°C for 40 min does not change the film to single domain. This must be due to the low annealing temperature. Single domain GaAs can be grown on this double domain layer at a temperature less than 500°C, at which the film does not change to single domain by annealing only. This shows that there is a self-annihilation mechanism during epitaxial growth.

Figure 4 shows the annihilation model of APB. It is reported that the APB surface with low index number such as (110) and (100) preferably appears in GaAs[16]. The APB in (110) surface is electrically neutral because there are same number of Ga-Ga and As-As bonds in the APB and also stoichiometry is maintained. The excess energy calculation of APB has indicated that (112) and (110) APB are more likely to form than (111) and (100)[17]. Experimental observation of APB in GaAs on Ge has shown that {110}APB is more numerous than {112}[16].

In order to annihilate the APB in the GaAs(100) during the growth, APB must exist in the plane, not perpendicular to the surface. The APB planes of {111}, {112}, {113}... are the candidates for the self-annihilation. Among them only {111} and {112} planes are suitable for the self-annihilation, because the antiphase domain gradually shrinks assuming the preferential occupation of Ga or As atom at the antisite in the APB²⁾. In the case of {111} APB, the annihilation is most simply explained by assuming that APB consists of Ga-Ga bonds. The APB generated at the step 1 in Fig. 4 goes up along (111) plane and the APB generated at the step 2 goes up along (111) plane, so that the two APB's meet at a particular thickness. However, in this case the electric charge is accumulated at the APB because the bonds in APB are only Ga-Ga bonds, resulting in the increase in the interface energy[17]. To neutralize it, As-As bonds are introduced in the new model, in which the APB facet generates in {112} plane as shown in Fig. 4. The two kinds of APB's ((112) and (112-bar)) generated at the corresponding steps meet each other in proceeding the growth, and then the APB disappears. Assuming that Ga-Ga bonds are more likely to generate than As-As bonds

(physical basis of this assumption is not clear at this stage), the domain direction of GaAs grown on Si is consistent with the experimental results. Recently Ueda et al. observed the triangular APB[18] as shown in Fig. 4. In their observation, the inclination is smaller than (111) and close to (112). These results strongly support the annihilation mechanism stated above.

CONCLUSION

It is shown that the APB is annihilated during the epitaxial growth by MBE. The APB annihilation model has been proposed. The experimental results involving domain direction are reasonably explained by this model. The condition of charge neutrality requires some modification of atomic arrangement at the interface. Our model is very simplified one, and deeper understanding of the annihilation mechanism including the interface atomic re-arrangement should be done.

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EVALUATION OF ANTI-PHASE-BOUNDARIES IN GaAs/Si HETEROSTRUCTURES BY TRANSMISSION ELECTRON MICROSCOPY

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ABSTRACT

The nature and behavior of anti-phase-boundaries in GaAs/Si heterostructures using GaP, GaP/GaAsP and GaAsP/GaAs strained layer superlattices as intermediate buffer layers, have been investigated by transmission electron microscopy. It has been found that anti-phase-domains are very complicated three dimensional polygons consisting of several sub-boundaries in different orientations. Self annihilation of anti-phase-domains during crystal growth of GaAs on (001) just or (001) 2° off Si substrates is directly observed for the first time through planview and cross-sectional observations. Based on these findings, a mechanism of annihilation of these domains is proposed.

INTRODUCTION

Recently, much effort has been put into the investigation of defects generated in highly mis-matched (HM 2) hetero-epitaxy such as GaAs/Si(Ge)[1-5], GaP/Si[6] etc. Major problems in these systems are 1) introduction of a high density of defects, i. e., dislocations, stacking faults, and microtwins, and 2) accumulation of internal stress due to difference in thermal expansion coefficients between the epitaxial layer and the substrate during the cooling process after growth. The current best data for dislocation density evaluated by plan-view TEM observation is known to be in the low 10^6 cm^{-2} , achieved by the combination of standard low-high two-step growth technique and thermal annealing during growth[7], or using strained layer superlattice(SLS) as an intermediate buffer layers[8,9]. However, for the second problem, the situation has not been drastically changed yet[10].

The problem of anti-phase-domains(APD's)[11], has received considerable attention in the past; it is now recognized that they can be practically controlled by using (001) more than 2° off Si as a substrate[12]. However, the exact nature and mechanism for their generation(and annihilation, if any) can not be fully understood yet. Etch-pitting with molten KOH is the most commonly used method for revealing APD's[13]; one can identify anti-phase-boundaries(APB's) by the presence of two kinds of etch-pits elongating in equivalent $\langle 110 \rangle$ orientations on both sides of the boundary. Since the typical diameter of these etch-pit is in a range 1-3 μm , sub-micron size APD's are not detected by this method. The most powerful method for microscopic identification of APD's is transmission electron microscopy(TEM). At present, two unique techniques can be employed for surveying APD's. One is the convergent beam electron diffraction(CBED) approach which was originally demonstrated by Taftø and Spence[14]. The other is the ± 002 dark field imaging technique proposed by Kuan[15]. The latter method is a very simple one; thus we have also employed this method in our experiments. The technique enables us to produce distinct dark and bright contrast on both sides of the APB, although the contrast is strongly related to the foil thickness.

In this paper, we describe for the first time a detailed structural investigation of APD's by transmission electron microscopy(TEM) and present direct evidence for their self-annihilation.

EXPERIMENTAL PROCEDURES

Crystals were grown by metalorganic chemical vapor deposition(MOCVD). The heterostructure consists of a GaP buffer layer(0.1 μm), followed by SLS's of GaP/GaAs_{0.5}P_{0.5} and GaAs_{0.5}P_{0.5}/GaAs(5 period for each SLS and 20 nm for each layer), and finally a thick GaAs layer(4 μm). The growth temperatures for the GaP, SLS's, and GaAs were 900°C, 750°C, and 750°C, respectively. TMG, AsH₃, and PH₃ were used as reactants(the detailed growth procedure is described elsewhere)[16,17]. Two types of heterostructures were examined; Type-I was grown on (001) $\pm 0.5^\circ$ Si substrates and Type-II on (001) 2° off toward [110] substrate.

Both plan-view and cross-section TEM observations were carried out; in both cases, specimen preparation was performed by ion thinning. TEM observations were carried out in an Akashi ultra-high resolution analytical electron microscope EM-002B operated at 200 kV.

RESULTS AND DISCUSSION

First of all, plan-view and cross-section TEM observations were performed for Type-I structures. From the plan-view observations, we have found uniformly distributed domain-like regions of the type shown in Fig. 1. It is concluded that these regions correspond to anti-phase-domains(APD's) for the following reasons:

- (1) No extra spots for small-angle tilt boundaries are found in the electron diffraction pattern from the area containing the domain-like regions.
- (2) Some part of the boundary has fringe-contrast, but this is not due to a stacking fault since the fringe is not asymmetric in the dark-field image.
- (3) In the electron diffraction pattern from areas including the domain-like regions in the (110) and the (1 $\bar{1}$ 0) cross-sections, no twin-related spots are observed.
- (4) From cross-section observations, the contrast of the domain itself in a dark field image is reversed when the reflection vector is changed from 002 to 00 $\bar{2}$ as illustrated in Fig. 2(details for Fig. 2 are described later).



Fig. 1. A typical plan-view bright-field TEM image illustrating APD's in the GaAs top layer of the GaAs/SLS's/GaP/Si heterostructure grown on a (001) $\pm 0.5^\circ$ Si substrate, taken under the $\langle 001 \rangle$ zone-axis illumination.

The domain size is found to be in the range $0.5 - 2.0 \mu\text{m}$; thus, the etch-pitting technique would not be expected to detect these small APD's, since etch-pits are larger than $1 \mu\text{m}$ in most cases. Each APD has a different geometry; they are found to be three-dimensional extended polygon-shaped structures consisting of many different sub-boundaries. These sub-boundaries are classified into two types; those nearly normal to the (001) plane and those inclined to the (001) plane. Fig. 2 shows a typical plan-view bright-field TEM image of an APD taken under the 220 reflection. Since the sub-boundaries denoted by A-B and D-E do not display fringe contrast, they are expected to be normal to the (001) plane. From the directions of their elongation, they are possibly (110)- and (100)-oriented boundaries, respectively. From plan-view observations it is found that most of the APB's normal to the (001) plane are $\{110\}$ or $\{100\}$ boundaries. The other boundaries denoted by B-C-D-C'-B and A-F'-E-F are curved and exhibit fringe contrast. This may be due to the phase-shift of the electron beam when the electrons re-enter from the matrix crystal to the APD. Thus, they are inclined to the (001) plane and are perhaps a mixture of tilted APB's indexed as $(11n)$ (such as (111) and (112)) and $(10n)$ (such as (101) and (102)).

In each boundary, a number of dislocations can be seen. In this case, these boundary-dislocations are invisible under the reflection of 400 or 040. Since most of the APB's are not lying on the $\{111\}$ plane, these boundary-dislocations can not glide. Also in the case where stacking faults and micro-twin are generated in the APD, they cannot be expected to extend to the region outside the APD, since there is a clear difference in atomic arrangement between the APD and matrix crystal. From stereoscopic observations, it is found that the circuit denoted by A-B-C-D-E-F-A in Fig. 2 is lying below the top surface and that the circuit denoted by A-B-C'-D-E-F'-A is lying on the top surface. This finding strongly suggests that the domain size becomes smaller during the sequence of crystal growth, with self-annihilation occurring as a final stage.

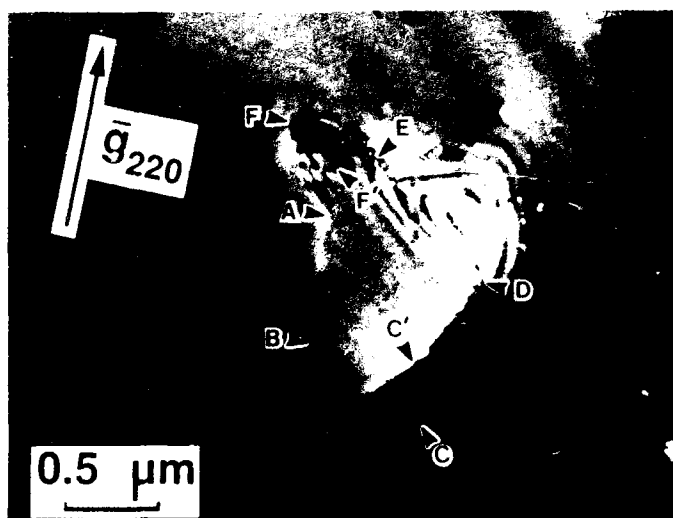


Fig. 2. A typical plan-view bright-field TEM image of a anti-phase-domain in the GaAs top layer of the GaAs/SLSi's/GaP/Si heterostructure grown on a (001) $\pm 0.5^\circ$ Si substrate, taken under the 220 reflection.

Surprisingly, we have discovered direct evidence for this speculation in the cross-section TEM image shown in Fig. 3. Figures 2(a) and 3(b) are dark field images taken by weak 002 and 00 $\bar{2}$ reflections obtained from the (110) cross-section specimen of Type-I. A high density of defects (mostly dislocations) is present in both the GaP buffer layer and the SLS's, since the crystal is grown on (001) $\pm 0.5^\circ$ Si. In both figures, a domain extending from the interface between the Si substrate and the GaP buffer layer into the GaAs layer is observed (see the domain denoted by APD), although the contrast of the boundary in the region below the SLS's is not clear due to the high defect density. It should be noted that in Fig. 3(a) the domain contrast is bright whereas that of the matrix region is dark. On the other hand, the opposite result is obtained in Fig. 3(b). Since the crystal structures on both sides of an APB are related to each other by a 180° rotation along the $\langle 110 \rangle$ direction, the 002 reflection from the crystal on one side of an APB should be equivalent to that of the 00 $\bar{2}$ reflection from the other side of the APB. We have calculated the amplitude of transmitted beam and the 002 and 00 $\bar{2}$ beams in an (110) diffraction pattern from perfect GaP and GaAs crystals as a function of foil thickness (see Fig. 4). It is found that due to the lack of twofold axes along the $\langle 110 \rangle$ direction in the zinc-blende structure the amplitudes of the 002 and the 00 $\bar{2}$

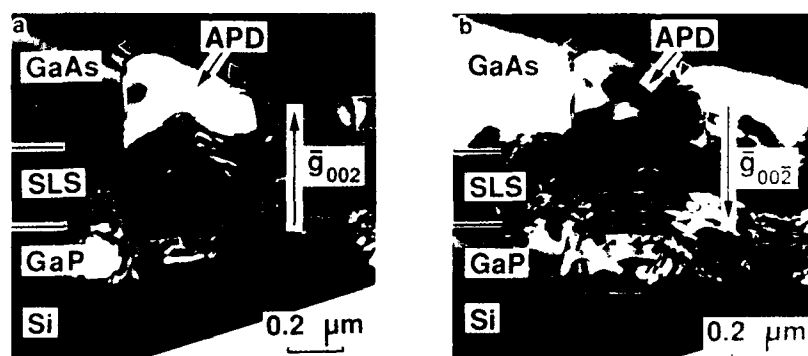


Fig. 3. Cross-section dark field images of the GaAs/SLS's/GaP/Si heterostructure obtained by the weak 002 and 00 $\bar{2}$ reflections. An anti-phase-domain (see the region denoted by APD) self-annihilating in the intermediate layer of GaAs is observed. (a) $\bar{g}=002$; (b) $\bar{g}=00\bar{2}$.

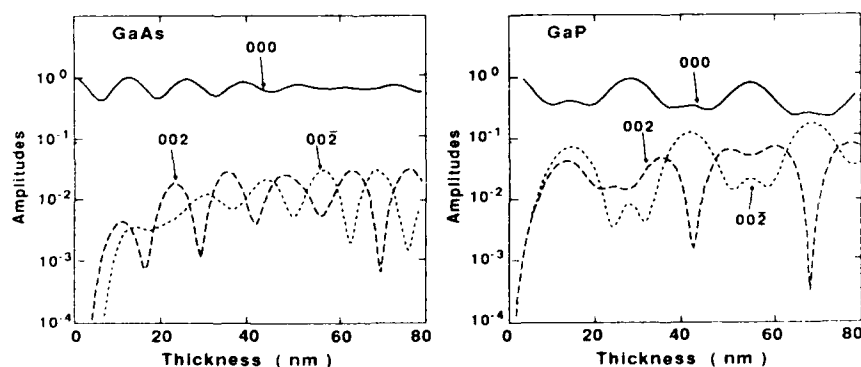


Fig. 4. Calculated thickness dependence of the amplitude of the 000, 002, and 00 $\bar{2}$ reflections from GaP and GaAs crystals.

reflections are not equal for most crystal thicknesses. Thus, one can conclude that the image intensities from both sides of the APB must be different except for certain foil thickness. In Figs. 3(a) and 3(b), the upper part of the figure correspond to the edge of the TEM specimen. The thickness is almost constant in the direction parallel to the interface and gradually increases from the upper part (edge of the foil) to the lower part. The estimated thickness of the major part of the image where APD is clearly observed (see the region denoted by APD) is roughly in the range 30–50 nm. Based on this consideration, the domain observed in Figs. 3(a) and 3(b) is identified to be an APD similar to that shown in Fig. 2. As can be seen in Figs. 3(a) and 3(b), the APD annihilates in the intermediate layer of GaAs by changing the orientation of sub-boundaries from normal to (001) to higher-index-planes (see also the region denoted by arrows).

On the basis of these results, the following scenarios are derived for the self-annihilation mechanism of APD's during crystal growth:

(a) At the initial stage of crystal growth, three-dimensional island growth proceeds at the step-edges. By the coalescence of islands with two different phases (i. e., matrix-phase and anti-phase), APD's are structurally introduced. The APD's may be originally columnar-shaped consisting of several sub-boundaries predominantly nearly normal to the (001) plane such as (110) and (100). Alternately, the sub-boundaries may be inclined to the (001) plane from an early stage of crystal growth, in which case step (c) takes place immediately;

(b) When the thickness of the APD reaches a critical value, these sub-boundaries change their orientation to the higher-index-plane inclined to the (001) plane (such as the (112) plane which is the orientation with lowest energy [17]), so as to minimize the total energy in the system;

(c) By the coalescence of APB's with opposite orientation, the APD finally annihilates itself at the intermediate layer.

At this moment, the reason for the existence of e.g. (100) APB's, which have a higher generation energy than (110) and (112) APB's, at the initial stage of crystal growth is not clear. Since not all of the APD's annihilate, it is also difficult to estimate the critical thickness for the step (b).

Next, Type-II samples are examined. From plan-view observations, APD's which are similar to those shown in Figs. 1 and 2 are not detected in the surface region of the GaAs layer. Figures 5(a) and 5(b) are 002 and 002 dark field TEM images from the (110) cross-section, illustrating the interface between the GaP buffer layer and Si substrate. Hillock-like micro-domains are observed in the GaP buffer layer near the interface (see arrows). The variation of the diffraction contrast of these micro-domains is very similar to that of the APD's shown in Fig. 3. Moreover, in this case, conditions (1)–(3) described previously (see the beginning of this section),

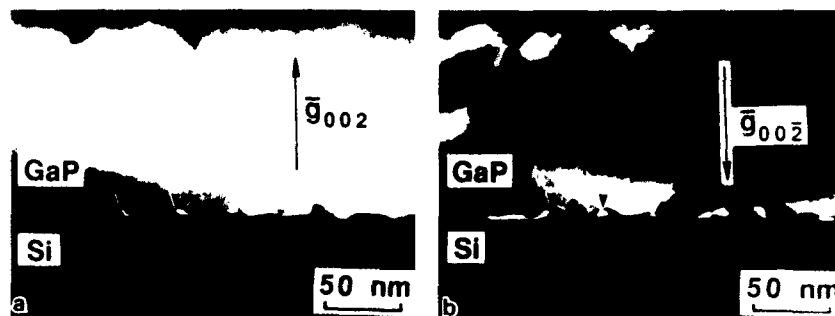


Fig. 5. Cross-section dark field images illustrating the GaP/Si interface in the GaAs/SLS's/GaP/Si heterostructure grown on a (001) 2° off Si substrate, obtained by the weak 002 and 002 reflections. (a) $\bar{g}=002$; (b) $\bar{g}=002$.

are satisfied. Therefore, it is concluded that they are also APD's, although very small, with diameters of 10-20 nm. Provided that there are a certain number of monolayer steps on the surface of a (001) 2° off Si substrate (there is still controversy about the existence of double-layer steps on the vicinal surface of Si), the frequent presence of APD's is well explained by the average spacing between monolayer steps, i. e., approximately 4 nm.

CONCLUSIONS

In conclusion, we have investigated the nature and behavior of APB's in GaAs/Si hetero-structures with GaP, GaP/GaAsP, and GaAsP/GaAs SLS's as intermediate buffer layers grown by MOCVD via TEM. It has been found that the size of the APD's depends on the offset angle of the Si-substrate. The APD's observed are very complicated three dimensional polygons and consist of several sub-boundaries in different orientations. We have also discovered APD's self-annihilating at the intermediate layer as a result of a change in the orientations of the sub-boundaries. Finally, a simple model for the generation of APD's has been presented.

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CORRELATION BETWEEN CRYSTALLINITY AND SCHOTTKY DIODE CHARACTERISTICS OF GaAs GROWN ON Si BY MOCVD

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ABSTRACT

We have studied the crystallinity and Schottky diode characteristics of GaAs/Si grown by MOCVD. In comparison with two-step growth and GaP/strained layer superlattice techniques, the crystallinity and the Schottky diode characteristics are superior for the GaAs/Si with $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ as an intermediate layer. The GaAs/Si grown with the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ intermediate layer shows mirror-like surface morphology and an X-ray FWHM of 188 arcs. The ideality factor of the Schottky diode fabricated on the GaAs/Si grown with the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ intermediate layer is 1.06, but its forward current-voltage characteristic shows a significant leakage current at small forward bias. It is also found that the composition of Al affects strongly the crystallinity and the Schottky characteristics of GaAs/Si.

INTRODUCTION

Serious problems with the growth of GaAs/Si are formation of antiphase domains in the GaAs epitaxial layer and differences of thermal expansion and lattice constants between GaAs and Si. Therefore, a high density of dislocations originating at the GaAs/Si interface propagate through the GaAs epitaxial layer. The high density of dislocations may degrade device performance on GaAs/Si. In order to overcome these problems, it has been reported that GaAs can be successfully grown on Si by the two-step growth and GaP/strained layer superlattice (SLS) techniques, using metal organic chemical vapor deposition (MOCVD)[1-4]. In this paper, we discuss the crystallinity and the Schottky diode characteristics of MOCVD-grown GaAs/Si by the two-step growth and by using the GaP/SLS and $\text{Al}_x\text{Ga}_{1-x}\text{P}$ as intermediate layers.

EXPERIMENT

Growth of GaAs/Si by MOCVD

GaAs epitaxial layers were grown on Si substrates oriented (100) off (110) towards (011) in an RF-heated horizontal MOCVD reactor at atmospheric pressure by the two-step growth technique and using $\text{Al}_x\text{Ga}_{1-x}\text{P}$ and GaP/SLS as intermediate layers. The two-step growth technique is as follows. The first GaAs layer with a thickness of 14.5 nm was deposited at 500°C, followed by the GaAs epitaxial layer doped with Se. In the technique with the $\text{Al}_x\text{Ga}_{1-x}\text{P}$ as an intermediate layer, 5 nm of $\text{Al}_x\text{Ga}_{1-x}\text{P}$ was grown on Si at 500°C, followed by growth of the GaAs epitaxial layer doped with Se. In the GaP/SLS technique, a 0.1 µm thick GaP film was grown on a Si substrate at 500°C, followed by five periods of 20 nm GaP/20 nm GaAs, 20 nm GaAs/10 nm and five periods of 20 nm $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ /20 nm GaAs at 500°C. Then, a GaAs epitaxial layer doped with Se was grown. In all cases, a 0.1 µm thick GaAs epitaxial layer doped with Se to $1 \times 10^{18} \text{ cm}^{-3}$ were grown at 500°C.

700 and 750 °C. The crystallinity of the GaAs epitaxial layers were studied by double-crystal X-ray rocking curve measurements.

Fabrication of Au-GaAs/Si Schottky diode

AuGe/Ni/Au ohmic electrodes were formed by vacuum evaporation. Schottky contacts to Se-doped GaAs were then made by the lift-off technique using Au as the Schottky contact metal. The area of the Schottky contact is $7.85 \times 10^{-3} \text{ cm}^2$. Current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the Schottky diodes were measured, and the ideality factor and the Schottky barrier height (ϕ^{1-V}) were calculated.

RESULTS AND DISCUSSION

Crystallinity of GaAs/Si grown by MOCVD

Figure 1 shows the FWHM of the (400) reflection peak of the X-ray double-crystal rocking curve as a function of growth temperature. In all samples, the FWHM decreases with increase in the growth temperature. This result suggests that the crystallinity of GaAs/Si improves at higher temperatures. At 750 °C, the FWHM's of the GaAs/Si grown by the two-step growth, $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ and GaP/SLS techniques are 210, 188 and 152 arcs, respectively.

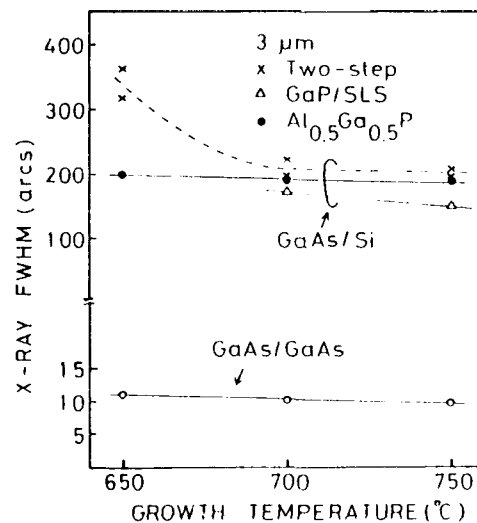


Fig. 1. Growth-temperature dependence of X-ray FWHM of GaAs/GaAs and GaAs/Si.

The surface morphology of the three types of GaAs/Si samples are shown in Fig. 2. The morphology of the GaAs/Si grown with the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ intermediate layer shows more specular than that of the GaAs/Si grown by

the two-step growth or GaP/SLS techniques.

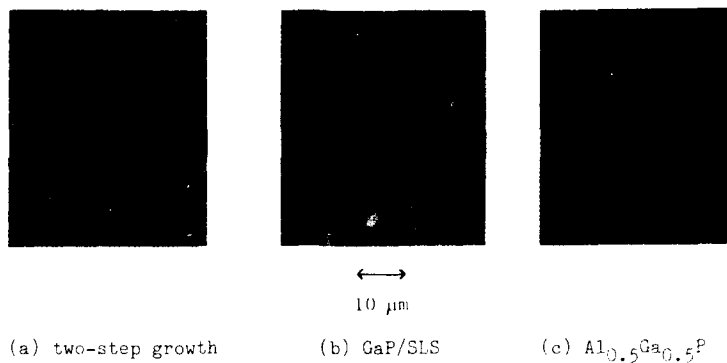


Fig. 2. Surface morphology of GaAs/Si grown by (a) two-step growth, (b) GaP/SLS and (c) $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ techniques.

We have also studied the effect of the intermediate layer on the crystallinity of GaAs/Si. Figure 3 shows the X-ray FWHM of the GaAs/Si grown with $\text{Al}_x\text{Ga}_{1-x}\text{P}$ as an intermediate layer. The X-ray FWHM depends on the composition of Al (x) and the minimum FWHM has been obtained at about 0.5. The dependence of X-ray FWHM on the composition of Al coincides with the crystallinity studied by the other measurement, such as etch pit density and surface morphology[5]. From these results, it is clear that the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ is suitable material as an intermediate layer.

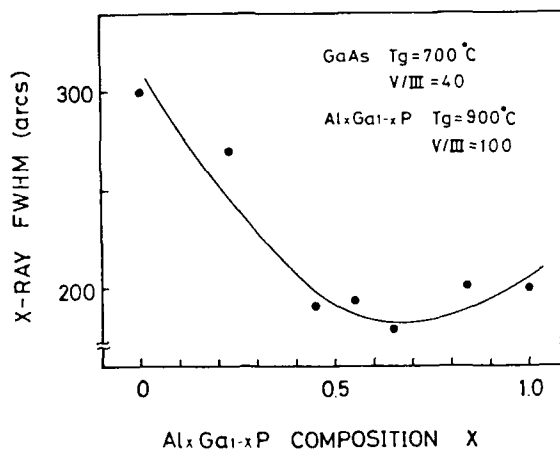


Fig. 3. Al-composition dependence of X-ray FWHM of GaAs/Si grown with $\text{Al}_x\text{Ga}_{1-x}\text{P}$ as an intermediate layer.

Characteristics of Au-GaAs/Si Schottky diode

Next, we have studied the characteristics of Schottky diodes fabricated on the GaAs/Si grown by the two-step growth, $\text{Al}_x\text{Ga}_{1-x}\text{P}$ and

GaP/SLS techniques. Figure 4 shows the ideality factor calculated from the forward I-V characteristics of Schottky diodes on GaAs/Si as a function of the growth temperature. For comparison, that for a Schottky diode fabricated on n-type GaAs substrate is also shown in the figure. With increase in the growth temperature, the ideality factor approaches 1. This result indicates that the crystallinity and Schottky diode characteristics of GaAs/Si improve at higher growth temperature. At 750 °C, the ideality factors for the GaAs/Si grown by the two-step growth, GaP/SLS and $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ are 1.11, 1.09 and 1.06, respectively.

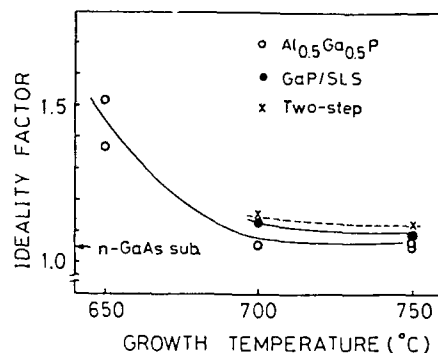


Fig. 4. Growth-temperature dependence of ideality factor of Au-GaAs/Si Schottky diode.

Figure 5 shows the dependence of the ideality factor on the composition of Al used as an intermediate layer. The ideality factor depends strongly on the composition of Al and the ideality factor of 1.06 is obtained by using $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ as an intermediate layer. This dependence of the Schottky diode characteristics on the composition of Al reflects the results of X-ray FWHM discussed earlier. The Schottky diode characteristic of GaAs/Si with $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ is as good as on n-type GaAs substrate.

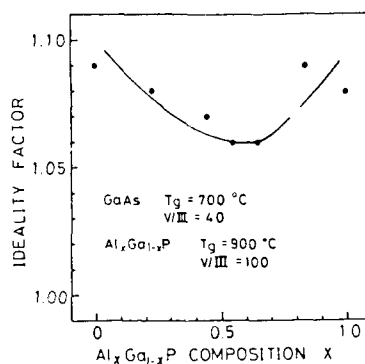


Fig. 5. Al-composition dependence of ideality factor of a Schottky diode on GaAs/Si grown with $\text{Al}_x\text{Ga}_{1-x}\text{P}$ as an intermediate layer.

Assuming the Richardson constant A^{**} is $8.6 \text{ Acm}^{-2}\text{K}^{-2}$ and that the characteristic I_0 follows the thermionic emission model[6], the Schottky barrier height ϕ_{B0} was calculated from the current extrapolated to 0 V in

the forward I-V characteristic. The ϕ^{I-V} is between 0.86 eV and 0.9 eV in all samples. The plots of C^{-2} vs. V are linear from the measurement of the C-V characteristics.

The forward I-V characteristics measured as a function of temperature are shown in Fig. 6. Note that significant leakage current is seen at small forward bias for Schottky diodes on GaAs/Si. This leakage current, which is not explained by the thermionic emission current, increases at the lower temperature.

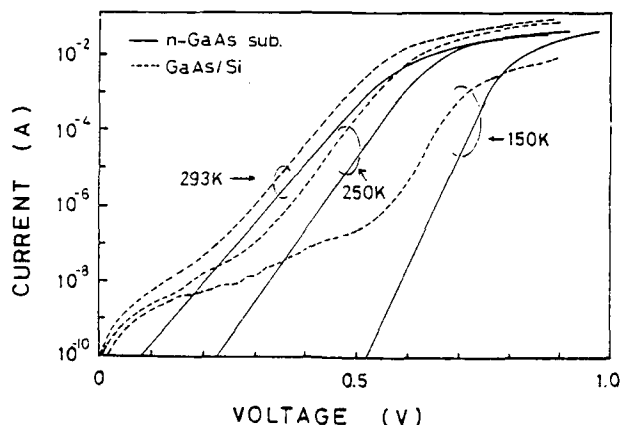


Fig. 6. Forward I-V characteristics of a Schottky diode on n-GaAs substrate and GaAs/Si grown with an $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ intermediate layer as a function of temperature.

Figure 7 shows the dependence of the ideality factor and the ϕ^{I-V} on temperature. Normally, the ϕ^{I-V} is a decreasing function of temperature[7]. The ϕ^{I-V} for n-type GaAs substrate is almost unchanged, while the ϕ^{I-V} for GaAs/Si is an increasing function of temperature. The fact that the ϕ^{I-V} for GaAs/Si is an increasing function of temperature may be related to material and electrical properties unique to GaAs/Si.

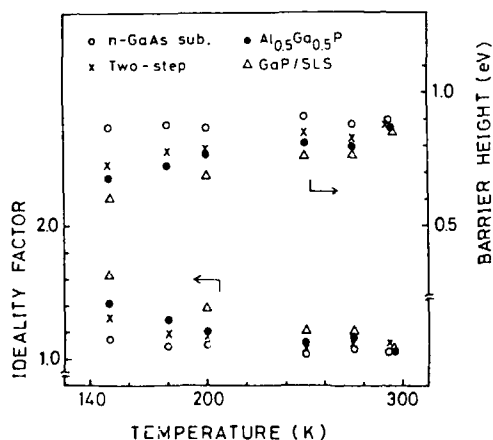


Fig. 7. Temperature dependence of the ideality factor and the Schottky barrier height of n-GaAs substrate and GaAs/Si.

CONCLUSIONS

We have studied the crystallinity of MOCVD-grown GaAs/Si and characteristics of Schottky diodes fabricated on the GaAs/Si. In comparison with the two-step growth and GaP/SLS techniques, the crystallinity and the Schottky diode characteristics are superior for GaAs/Si with $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ as an intermediate layer. From the study of the effect of an intermediate layer on the crystallinity of GaAs/Si, it is clear that the intermediate layer plays an important role in improving crystallinity and the Schottky diode characteristics of GaAs/Si. The $\text{Al}_{0.5}\text{Ga}_{0.5}\text{P}$ is found to be suitable as an intermediate layer for GaAs/Si.

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SILICON SURFACE PASSIVATION FOR HETEROEPITAXY BY HYDROGEN TERMINATION

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ABSTRACT

Results are reported for XPS and LEED evaluations of Si(100) wafers cleaned, etched, and hydrogen terminated by various low-temperature, wet-chemical techniques. We have obtained especially promising results with the JPL spin-etch technique. Under quite practical tolerances for the spin etch, our XPS measurements indicate about 1×10^{-2} monolayer (ML) of total residue. The LEED showed sharp spots in a (1x1) pattern. We review our experimental results and suggest an interpretation in terms of both the chemistry of silicon surfaces in contact with HF in a polar solvent, and the hydrodynamics of liquids on spinning surfaces.

INTRODUCTION

In heteroepitaxy, the use of low temperatures would provide numerous advantages. However, new methods of preparing silicon substrates are needed which will avoid the brief high-temperature oxide-desorption process step commonly used just before epitaxial growth is begun. Contrary to the lore surrounding the silicon-fluorine bond strength, it was recently reported that silicon surfaces immersed in an HF etchant are not bound up with F or its compounds and show remarkably ideal electronic properties [1]. It has developed that the Si(100) surface under these wet-chemistry conditions is free of residue and has its dangling Si bonds terminated with a layer of hydrogen [2]. When dry, this H-terminated surface was also found to show considerable resistance to reoxidation and contamination, i.e., passivation.

The Grunthaners and their coworkers at the Jet Propulsion Lab have done much of the initial phase of process development and characterization of H-terminated silicon for introduction into UHV [3]. Their spin-etch technique is that of using an HF-in-ethanol etchant pipetted onto the Si/oxide surface while it is being spun in a glove box with a flowing nitrogen atmosphere. In the present study we have made an effort to simplify this technique with a systematic study of the science of the various processing steps. We have made extensive use of the proof-plate technique by which the very clean surfaces can be used to sample various substances used in the process. We have also made comparative evaluations of this technique with other more conventional methods of substrate surface preparation for UHV and epitaxial growth. These results are reported at length elsewhere [4].

EXPERIMENTAL

Our most successful method of H-termination of silicon is basically that of the JPL group [3]. The initial degreasing of the Si is done with detergent followed by a sequence of solvents and finally a soak in chromic-sulfuric acid. This acid is an especially effective oxidizer of organic material. We normally do the etch of the Si samples in a stainless-steel glove box with a moderate flow of N_2 gas from liquid boiloff. Recently, we have had promising results doing the spin etch under a stream of N_2 gas in a hood (five-sided box). A pipette is always used to dispense the etchant so as to avoid transferring to the sample the organic and particulate matter which is concentrated at the free surface of the liquid reagents. Our etchant is $HF + H_2O + \text{ethanol}$ at 1:1:10, and the water and ethanol are commercial "HPLC-grade" purity, which has a very low level of nonvolatile residue.

A port on our glove box provides direct entry into a VG ESCALAB where XPS, scanning small-spot AES, and LEED surface-analysis techniques are available. The XPS provides quantitative surface residue analysis down to coverages of the order of 5×10^{-4} ML. This is accomplished by counting the total photoelectron emission from core levels of C, N, O, F, and Si.

RESULTS

In Fig. 1 is a typical high-resolution XPS spectrum of the Si 2p core level for a spin-etch prepared surface. A monochromated Al K_{α} source was used. The dotted curves are a simulation of the spin-orbit split lines using parameters from the literature [4]. There was no indication of any contribution other than the simulated Si 2p doublet.

Samples were tilted to analyze only electrons from a glancing takeoff angle (6°). The XPS was then highly surface sensitive with an effective electron escape depth of about 1 ML of Si. In Fig. 2 are shown surface sensitive spectra using the bright, unmonochromated Mg K_{α} source; one sample was prepared by a conventional UV-ozone cleaning [5] followed by a dip in $HF + H_2O$ (1:10), and the other by the spin-etch technique. A substantial component of the Si 2p line shifted to lower kinetic energies by binding to oxygen is seen for the dip-etch sample, but there is none within the noise for the spin-etch sample.

The two samples just described and many others were evaluated with XPS to determine the emission from core levels of specific residue elements, e.g., C, N, O, and F. Figure 3 shows results for O and C 1s core-level emission for Si(100) with various processes and proof-plate exposures. The highest intensity line shown in the figure is for the dip-etched sample. The curve with the least residue is from a freshly spin-etched sample processed entirely in the glove box. Other curves indicate the increase in residue for this sample exposed to either air, evaporation of a large drop of HPLC-grade ethanol, or dipping into HPLC-grade water. Note the very effective

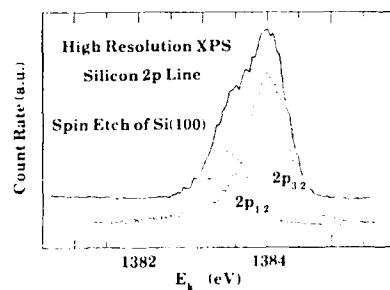


Fig. 1. Silicon 2p core-level spectra as a function of electron kinetic energy E_k . The source photons are 1486.6 eV. The solid line was measured for a spin-etch prepared surface, and the dotted lines are simulated components of the spin-orbit doublet.

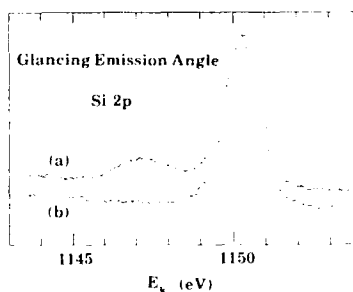


Fig. 2. Silicon 2p core-level spectra for 1253.6 eV photons. The photoelectrons are collected from a glancing angle. Curve (a) is a UV-ozone cleaned and dip etched sample. Curve (b) is immediately after a spin-etch preparation.

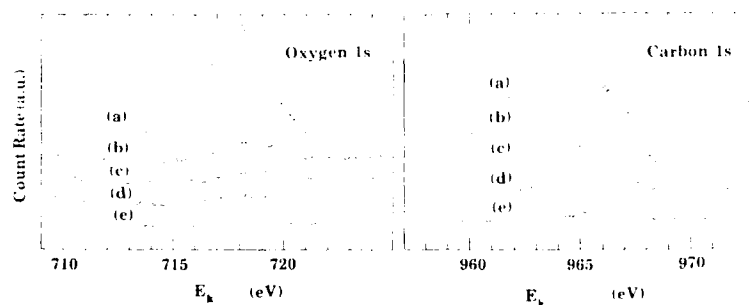


Fig. 3. Oxygen and carbon 1s core-level spectra for 1253.6 eV photons collected from Si surfaces with various preparations: (a) UV-ozone cleaned and dip etched, (b) to (e) spin-etching with subsequent exposures to (b) dipping in water, (c) evaporation of ethanol on the surface, (d) exposure to room air for 1 min, and (e) inspected immediately after the spin-etch. The XPS instrument operating conditions were held constant, and the curves are offset for clarity.

passivation against reoxidation and contamination upon (room) air exposure, the evaporation residue left by the ethanol, and the much worse contamination caused by dipping in the ultrahigh purity water. In the latter case the sample has surely swept up contamination from the liquid water surface.

Table I summarizes the residue coverages found for various samples including a freshly cleaved Si(111) surface and an Ar⁺ ion sputtered Si(100) surface. The cleavage results are a measure of the ultimate cleanliness of our diffusion-pumped UHV environment. These samples had initially rapid increases in their C and O coverages. Comparing the cleaved and spin-etch sample uptake rates, we conclude that H-terminated surfaces are between 10 and 14 orders of magnitude more passive than unterminated silicon [4].

TABLE I. Surface residue coverages from XPS measurements of silicon with various preparations. 1 ML (one monolayer) corresponds with $6.8 \times 10^{14} \text{ cm}^{-2}$.

Sample	C (ML)	O (ML)	F (ML)
Cleave Si(111) in UHV (10 min after)	0.007	0.0008	—
Chromic Acid & Spin Etch Si(100)			
in nitrogen glove box	0.025	0.005	0.010
in nitrogen hood	0.042	0.012	0.016
<i>Subsequent proof-plate tests</i>			
1 atm air for 1 min	0.064	0.010	0.012
water evaporation	0.069	0.023	0.005
dip in water	0.15	0.022	0.003
Ar ⁺ ion sputtering (while at 600°C)	0.16	0.11	—
UV-Ozone & Dip Etch	0.19	0.16	0.01
Degrease and Dip Etch	0.25	0.13	0.10

Our initial results for a sample prepared by spin etching without a glove box (i.e., in a hood) are very similar to the results for samples spin etched in the glove box and then exposed to air for 1 min. Both of these samples show remarkably little residue, and we are currently seeking improvements to this promising simplification.

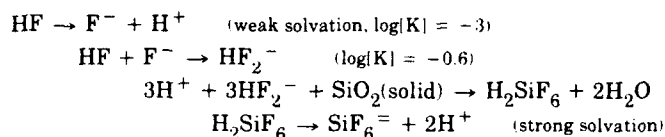
LEED patterns for the H-terminated surfaces were unreconstructed, i.e., 1x1, with spots as sharp as we observed for our cleaved surfaces. The dip-etched samples were nominally 1x1 also, but the spots were not as sharp and varied in definition as the sample was translated laterally under the LEED beam.

DISCUSSION

The success of the spin-etch technique in producing H-terminated surfaces and the remarkable passivation that results are a consequence of several factors

The uniformity of the solid/liquid interface is greatly enhanced by the use of ethanol since it has a small contact angle (good wetting) even with etched Si surfaces. Interface segregation of ethanol from solutions with water occurs due to differential adsorption [6] onto Si. This increases the solvation of trace hydrocarbon residue at the Si surface. The electrolyte solution of ethanol, water, and HF acid induces an electric double layer at the liquid/solid interface which enhances the H^+ ion concentration near the surface and encourages diffusion of negative ions away from the surface [6].

The chemistry of the etch reaction is influenced by the polar solvent, and differs considerably from gas phase reactions.



The H^+ ion reaction products near the etching surface are available to terminate the Si surface.

The larger thermochemical bond energy for Si–F relative to Si–H bonds can be misleading since the former have a much higher bond ionicity (electronegativity difference). Thus, Si–F bonds are more easily attacked (lower free-energy barrier, ΔG) than their bond energy might imply [7]. The reaction rate constant $k = k_0 \exp(\Delta G/k_B T)$ depends on equilibrium parameters, ΔG , and dynamic factors, k_0 . In polar solvents the solvation relaxation time t and the self diffusion D are the main dynamic factors [8], and typical values are shown in Table II.

TABLE II. Dynamic effects in typical polar solvents (Ref.8).

Solvent	t (ps)	D (cm ² /s)
water	0.5	2.5×10^{-5}
methanol	9.2	2.3×10^{-5}
n-propanol	77	0.7×10^{-5}

Clearly the addition of water to the etchant used in the present study has several beneficial effects, including enhancement of the rate of solvation of ionic reactants during the etch. Indeed, we found a larger amount of F residue on spin-etched Si when the etchant had no additional water, i.e., HF + ethanol (1:10).

The hydrodynamics of spinning ethanol onto Si surfaces has three important regimes: The centrifuge regime, during which the drop flattens and spreads centrifugally and excess liquid is spun off. The gas/liquid shear-stress regime, when the rotating table acts as a centrifugal gas pump causing a radial shear stress

that further thins the liquid. It is expected that this thinning mechanism will eventually dominate the centrifugal one and that the thinning rate will slow down, following a power law in time [9]. For high vapor-pressure solvents, such as ethanol, an evaporation regime is reached when the evaporation rate becomes proportionally high for very thin liquid films. Also, nonzero contact-angle solvents in the thinning limit will be in very small, stable surface droplets, which then evaporate. All such evaporation of fluids on the freshly etched surface will deposit nonvolatile residue. This is evident in Fig. 3, spectrum (c).

The passivation chemistry of H-terminated silicon is likely due to the hydrophobic nature of such surfaces, the low Si-H bond ionicity, and its relative strength. These leave the H-terminated surface resistant to attack by F^- and OH^- ions at the liquid/solid interface and to chemisorption by H_2O , CO, etc. in the vacuum. Physisorption and electrostatic binding of adventitious contamination and particulate matter is still quite possible but can be minimized by careful sample handling.

CONCLUSIONS

We have advanced the development of a simple low-temperature process that leads reliably to very passive H-terminated Si surfaces. The critical steps and their physical basis have been identified. These techniques and framework for analysis can be used to explore further simplifications and to anticipate the routine use of spin-etch prepared Si in epitaxial growth processes.

ACKNOWLEDGMENTS

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PHOTOEMISSION STUDY OF Si (001) SURFACES EXPOSED TO As FLUX

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ABSTRACT

Photoemission spectra (XPS and UPS) of As-covered Si (001) surfaces prepared at high ($>600^{\circ}\text{C}$) and low ($<450^{\circ}\text{C}$) temperatures and GaAs epilayers subsequently grown on them were measured without exposing to air. It was found that the surface electronic structures of As/Si prepared at the low temperature are different from those of the high temperature sample, the spectra of which can be interpreted as a symmetric dimer model. Differences were also observed between the GaAs epilayers on the As-covered Si surfaces prepared at the high and low temperatures. The temperature dependence of the surface and interface structures are discussed.

1. INTRODUCTION

The heteroepitaxy of GaAs on Si has attracted much interest from the viewpoint of the combination of the merit of compound semiconductor and Si technology[1,2]. To obtain high quality GaAs/Si structures, the understanding of the initial stage of GaAs growth on Si and its interface structure is necessary, including the structure of Si surfaces exposed to As. From RHEED studies, it has been reported by Kawabe et al. that the surface structure of As-covered Si (001) surfaces (As/Si) depends on the substrate temperature at which clean Si surfaces are exposed to As flux[3]. That is; (2x1) reconstruction of a Si (001) surface changes to (1x2) when the surface is exposed to As flux at high temperature ($>600^{\circ}\text{C}$), though the reconstruction does not change under the low temperature ($<450^{\circ}\text{C}$) As exposure. For the (001) surface of zincblende (or diamond) structure, epitaxial growth of one monatomic layer brings about 90 degrees rotation of reconstruction structure. Kawabe's result seemingly implies that the amount of deposited As layers is different between the high and low temperature exposure. While, chemical bonding and composition of the surfaces can not be revealed by RHEED studies. Photoemission spectra are very sensitive to surfaces conditions, and provide us

chemical information of surfaces. Several photoemission studies of As/Si systems have been reported up to now[4]. However, the temperature dependence of the surface structure of As/Si surfaces has not been discussed based on the photoemission spectra. In this paper, we report the results of *in-situ* photoemission measurements (XPS and UPS) of Si (001) surfaces exposed to As₄ flux at various temperatures and GaAs epilayers grown on them subsequently. The temperature dependence of the surface structures is discussed in relation to the initial growth of GaAs on Si.

2. EXPERIMENTS

The As-covered Si samples were prepared by molecular beam epitaxy. The preparation chamber is connected to the analysis chamber for photoemission measurements through ultra-high vacuum. The base pressures of the preparation and analysis system were less than 2×10^{-10} Torr. Clean Si surfaces were obtained by heating chemically etched Si wafers under Si beam in vacuum. During this cleaning process, The temperature of As effusion cell was kept below 100°C to suppress the ambient As pressure. Subsequently, the Si surfaces were exposed to As₄ flux at various substrate temperatures between 200 and 750°C. The flux intensity of As₄ was $1-1.5 \times 10^{-6}$ Torr, and the exposure time was around 10 sec. After that, several monolayers of GaAs were grown on these As-covered Si substrates at 400°C. At each stage of the processes described above, the samples were transferred to the analysis chamber without exposure to air and photoemission spectra were measured excited by MgK α and HeI lines for XPS and UPS, respectively. Si2p peaks of Si substrates were adopted as the energy reference. The apparent atomic ratios were obtained from the XPS peak intensities and the photoemission cross sections reported by Scofield[5].

3. RESULTS AND DISCUSSION

At first, we show the results for As/Si surfaces. In Fig.1, the XPS spectra of As3d core levels for Si surfaces exposed to As₄ flux at 300°C (low temp.) and 680°C (high temp.) are shown. The binding energies of As3d levels are located between those for bulk

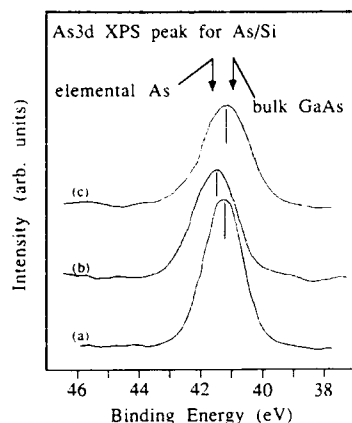


Fig.1 XPS spectra of As3d core levels for the Si surfaces exposed to As at (a) 680°C, and (b) 300°C. The spectrum for the sample (b) after heating up to 800°C is also shown as (c).

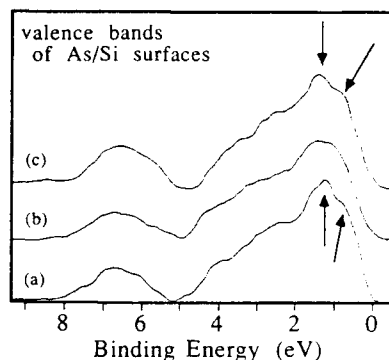


Fig.2 UPS spectra of the valence bands for the Si surfaces exposed to As at (a) 680°C, and (b) 300°C. Spectrum (c) is that for the sample (b) after heating up to 800°C. Surface states are observed just below the band edge for (a) and (c), as shown by arrows.

GaAs and elemental As. However, the binding energy for the low temp. sample is 0.3eV higher than that of the high temp. sample. Besides, the low temp. sample exhibits larger peak width than that of the high temp. sample. In GaAs/Si system, the valence of As is negative. The obtained XPS spectra indicate that the As atoms of the high temp. As/Si sample attract more electrons and the valence condition of the As atoms is more negative, compared with the low temp. sample. The wider peak of the low temp. sample suggests that there exist As atoms with different chemical bonding. The spectra c) in Fig.1 is for the low temp. sample after heated up to 800°C. The binding energy is almost the same as spectrum a). Therefore, the difference between spectra a) and b) can be attributed to the heating effect during the exposure to As₄ flux. In Fig.2, the UPS valence band spectra are shown. The measured samples and the notations of spectra are the same as in Fig.1. Only spectra a) and c) show shoulder-like fine structures just below the valence band edge. These structures are considered to be due to surface states. The fact that spectra a) and c) show the similar feature is quite identical to Fig.1. For As-terminated Si surfaces, the symmetric dimer model is proposed by Uhrberg *et al.*[4]. They insisted that the dangling bonds at the surfaces make As-dimers and doubly occupied lone-pair states, and these

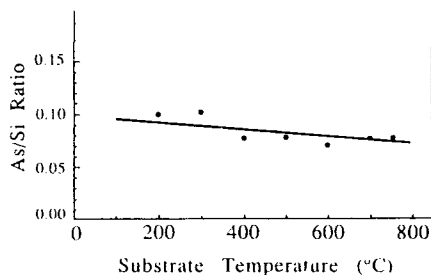


Fig.3 Apparent atomic ratios between As and Si against the substrate temperatures at which Si surfaces are exposed to As_4 flux. The observed ratios correspond to approximately 1 monatomic layer of As on Si.

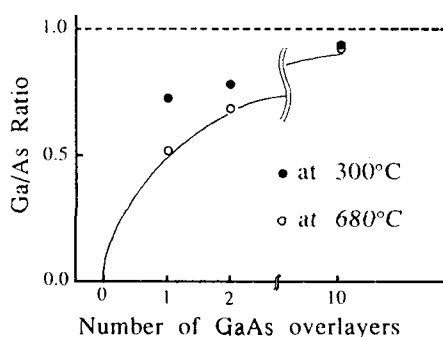


Fig.4 Apparent Ga/As atomic ratios for the GaAs epilayers grown on Si exposed to As_4 flux. Open circles denote the case of the Si exposed to As at 680°C and closed circles denote the case of 300°C. The solid line shows the expected values from the alternate stacking of Ga and As layers initiated by an As layer.

almost constant at around 1 monatomic layer through the whole temperature. More than 2 monatomic layers of As is not observed. Kawabe *et al.* also reported the similar result by Auger electron spectroscopy [3]. These results indicate the difference of the surface structures between the high and low temp. samples can not be attributed to the amount of As but results from the chemical bonding difference.

Next, we show the photoemission results for GaAs epilayers on As/Si surfaces. For both the high and low temp. samples, the binding energy of As3d levels shifts to that of bulk GaAs as the

lone-pair states result in the surface states. According to them, the observation of surface states indicates that the As-dimers are formed on the surfaces. The surface of the high temp. sample is considered to be identical to what Uhrberg *et al.* observed. On the contrary, the surface of the low temp. sample does not show structures which can be attributed to surface states. Its surface structure can not be explained by the As-dimer model. However, thermal treatment makes the surface identical to that of the high temp. sample.

Figure 3 shows the apparent As/Si atomic ratio for Si surfaces exposed to As_4 flux at various temperatures. Although a slight increase is observed with the decrease of the temperature, the amount of As on Si surfaces is found to be

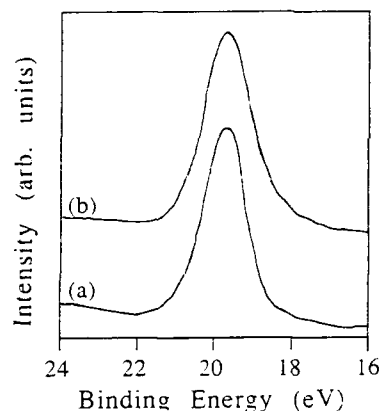


Fig.5 XPS spectra of Ga3d core levels for 2 monolayers of GaAs epilayers grown on Si exposed to As flux (a) at 680°C and (b) 300°C.

number of GaAs overlayers increases. In Fig.4, the apparent atomic ratios of Ga/As are plotted against the number of GaAs overlayers. The top layer of the grown surface is the As layer under the As-stabilized condition.

Assuming simultaneous growth of Ga and As and their alternate stacking initiated by an As layer, the observed atomic ratio should be $N/(N+1)$, where N is the number of (GaAs) layers. The ratios in the case of the high temp. sample correspond with $N/(N+1)$ quite well. However, the observed Ga/As

ratios observed for the low temp. sample are higher, which means the existence of excess Ga or As deficiency. In Fig.5, the XPS spectra of Ga3d core levels for GaAs grown on the high and low As-covered Si surfaces are shown. Although GaAs on the high temp. sample exhibits a clear single peak, the peak of the low temp. sample is a little wider and has a tail at the low energy side. Judging from the binding energy, the tail corresponds to elemental Ga atoms. Considering these results, the interface between GaAs epilayers and the Si substrate for the low temp. sample is not the ideal stacking of Ga and As layers initiated by an As layer. It is suggested that there is an elemental Ga phase at the interface, and it may bring about some kind of disorder. The difference of this GaAs/Si interface structure should result from the initial As/Si surface structure.

Based on the As-dimer model, which can explain the surface structure of the high temp. sample, each As atom is bonded to 2 Si atoms and 1 another As atom. While, each As atom is bonded to 3 As atoms and the valence is zero in As_4 species. The chemical environment of As atoms of the low temp. sample is between those of these 2 kinds of As. Therefore, in the case of the low temp. sample, it is considered that more than 1 As atoms are bonded to As atoms or the number of Si atoms bonded to As atoms is less than 2. Arsenic atoms of the low temp. sample may be As_4 atoms which are not fully decomposed. Further heating may then cause

decomposition consistent with the heating effect seen in Figs.1 and 2. While, Figs. 4 and 5 indicate that there is some structural deviation from the alternate stacking of atomic layers, such as in zincblende, at the As/Si interfaces of the low temp. sample. The structural deviation suggests that the initial structure of As/Si surfaces is not uniform. If Si surfaces are covered by As and As atoms are bonded to Si uniformly, the ideal stacking of Ga and As layers is expected. However, the experiments show the results against the uniform surface structure. There are some kinds of defects in the As overlayer, and these defects may actually induce the structural deviation at the initial stage of subsequent GaAs growth, when Si surfaces are at first exposed to As₄ at the low temperature.

4. CONCLUSION

Si (001) surfaces exposed to As₄ flux at various temperatures were investigated by *in-situ* photoemission spectroscopy. It was found that surface chemical bonding depends on the temperature at which Si surfaces are exposed to As. In the case of low temperature exposure around at 300°C, the valence of As atoms are lower than that of high temperature exposure, and the As overlayer is not uniform, and the surface structure can not be explained by As-dimer model. Also, the structure of GaAs epilayers just on As/Si surfaces is not ideal stacking of Ga and As layers, when Si surfaces are initially exposed to As at the low temperature. Some thermal energy is necessary for the formation of the As/Si surface structure described by As-dimer model.

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ELECTRICAL PROPERTIES OF THIN INTERMETALLIC PLATINUM-GALLIUM FILMS GROWN BY MBE ON GALLIUM ARSENIDE AND SILICON.

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ABSTRACT

Thin films of the platinum-gallium (Pt-Ga) family have been grown on gallium arsenide (GaAs) and silicon (Si) by molecular beam epitaxy (MBE). A partial list of potential uses for these and similar structures is high temperature stable photodetectors, Schottky and Ohmic contacts, epitaxial buried contacts, and field effect transistors. In this work the electrical properties of Pt_2Ga , PtGa , and PtGa_2 on both GaAs and Si will be presented. The resistivity of these thin films has been found to depend on the crystal quality and phase of the material.

Introduction

Recently there has been a significant amount of interest in intermetallic compounds grown on GaAs [1,2,3]. Excellent properties have been obtained for CoGa grown on GaAs by Palmstrom et.al. [2]. In this work we present the results of resistivity versus temperature for thin (~ 1000 to 2000 Angstrom) films of single phase Pt-Ga intermetallics grown at or near room temperature on GaAs(100) and Si(100). The resistivity versus temperature data was obtained using the van der Pauw method. A block diagram of the experimental setup is illustrated in Fig 1.

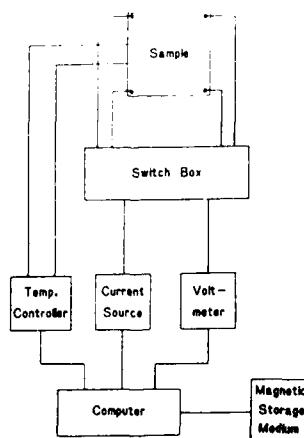


Fig. 1 Measurement setup.

Crystal quality and stoichiometry were determined by two-theta x-ray diffraction (XRD) and transmission electron microscopy (TEM). Pt_2Ga has been determined to be lattice-matched to GaAs while both PtGa and PtGa_2 , although not single crystal, show a high degree of epitaxial quality.

Resistivity versus Temperature of Pt-Ga Intermetallics on GaAs

For the work performed in this study all the thin intermetallic films were grown on either semi-insulating or very low doped GaAs(100). As these films were metals or semi-metallic in nature, the substrate did not contribute a parasitic current shunt path for the resistivity measurements. At each temperature point, the resistivity values reported consisted of an average of 5 (five) measurements in both the forward and reverse current directions, all results reported were reproducible and were not signal processed in any way.

The graphical results of the resistivity versus temperature of the Pt-Ga intermetallic single phase thin films are shown in Fig. 2 through Fig. 7. As can be seen from Fig. 2, the resistivity of PtGa_2 on GaAs is relatively low for a metal on GaAs. The liquid nitrogen temperature resistivity is $11 \mu\Omega\text{-cm}$ and the room temperature resistivity is $18 \mu\Omega\text{-cm}$. These values are in excellent agreement with the values obtained for bulk single crystal PtGa_2 [4].

For the case of PtGa on GaAs the resistivity values are considerably higher than those of PtGa_2 as can be seen from Fig. 3. The resistivity at liquid nitrogen temperature (77°K) for PtGa on GaAs is $215 \mu\Omega\text{-cm}$ and the room temperature (300°K) resistivity value is $362 \mu\Omega\text{-cm}$.

As shown in Fig. 4, the resistivity of Pt_2Ga -GaAs was extremely temperature insensitive, changing from $114.8 \mu\Omega\text{-cm}$ to $119 \mu\Omega\text{-cm}$ as the temperature was varied from 77°K to 300°K . The delta change in resistance of less than 5% corresponds to a resistivity temperature coefficient of approximately a factor of 20 times smaller than the temperature coefficients of the most common semi-metal and metallic materials [5,6]. At present, no simple theory exists to explain the almost temperature independent resistivity of Pt_2Ga on GaAs.

Resistivity versus Temperature of Pt-Ga Intermetallics on Silicon

As can be seen from Fig. 5 through Fig. 7 and Table I, the results of the resistivity versus temperature data indicate that the nature and structural properties of the host substrate play a major role in the measured resistivity values. Near-intrinsic ($>1000 \Omega\text{-cm}$) Si was used as the host substrate for all the films studied in this paper.

For the case of PtGa_2 on Si the resistivity at a given temperature was approximately a factor of three higher than those obtained on GaAs. This result is consistent with the increased host-substrate lattice mismatch producing a higher degree of mosaic nature in the film. This would suggest an increased scattering at grain boundaries, producing increased resistivity. Fig. 5 shows a typical resistivity versus temperature plot of PtGa_2 on Si. The liquid nitrogen and room temperature resistivity values are $32 \mu\Omega\text{-cm}$ and $62 \mu\Omega\text{-cm}$, respectively.

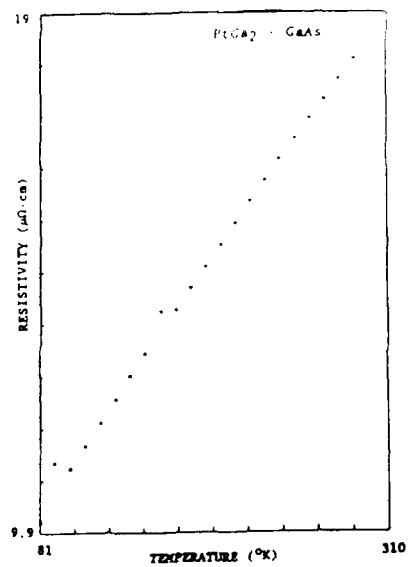
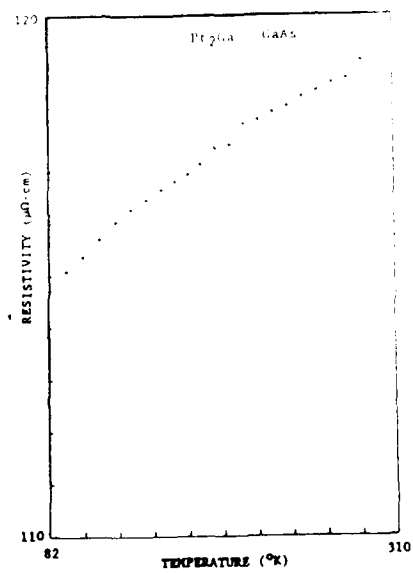
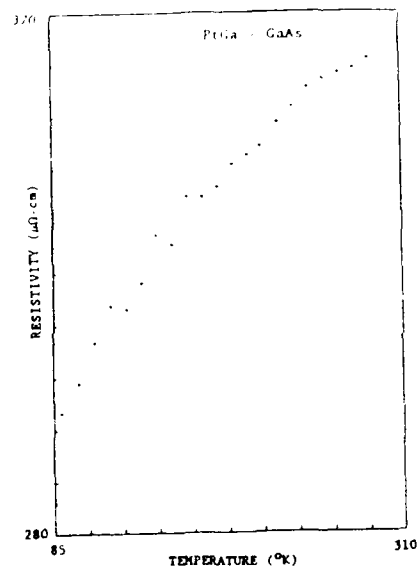
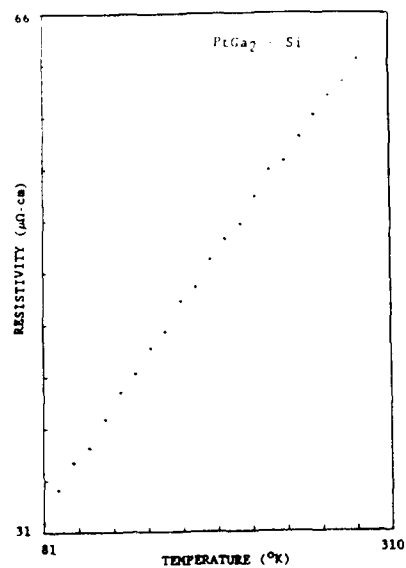
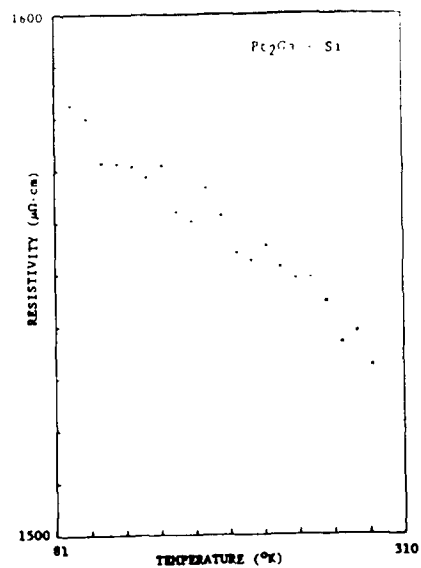
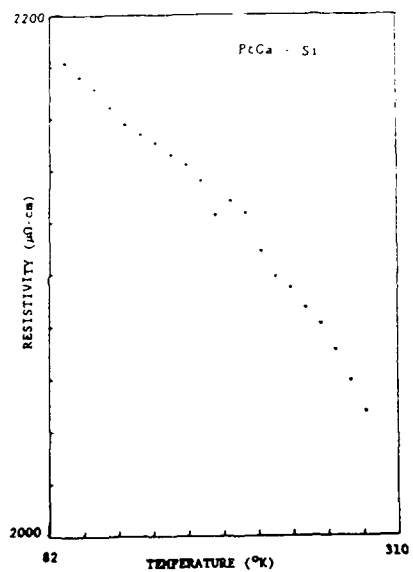
Fig. 2 PtGa₂ on GaAs.Fig. 4 Pt₂Ga on GaAs.

Fig. 3 PtGa on GaAs.

Fig. 5 PtGa_2 on Si.Fig. 7 Pt_2Ga on Si.Fig. 6 PtGa on Si.

PtGa on Si had resistivity values almost a decade higher than those of PtGa on GaAs. Referring to Fig. 6, it can be clearly observed that the resistivity decreases with temperature. Usually an inverse-law temperature dependent resistivity is indicative of semiconducting-like material. The liquid nitrogen and room temperature resistivity values are $2190 \mu\Omega\text{-cm}$ and $2045 \mu\Omega\text{-cm}$, respectively.

As can be seen from Fig. 7, Pt_2Ga on Si also exhibits a monotonically decreasing resistivity value as a function of temperature as observed for PtGa on Si. The resistivity of Pt_2Ga on Si is over a factor of 10 times greater than that of Pt_2Ga on GaAs. The liquid nitrogen and room temperature resistivity values are $1592 \mu\Omega\text{-cm}$ and $1533 \mu\Omega\text{-cm}$, respectively. Pt_2Ga on Si, although having a negative temperature coefficient of resistivity, also has a relatively temperature independent characteristic, changing by only 3.75 % in going from liquid nitrogen to room temperature.

TEM Results

Fig. 8 shows a TEM planar view of a Pt_2Ga film on Si(100). The image clearly shows the film to be composed of small grains. A similar film grown on GaAs was determined to be single crystal. The grain size in the shown film is on the order of 100 Angstroms which is comparable to the mean free path for most metals [5]. This corroborates the difference in the measured resistivities for these two films. A more detailed analysis of the correlation between crystal quality and resistivity will be presented elsewhere.

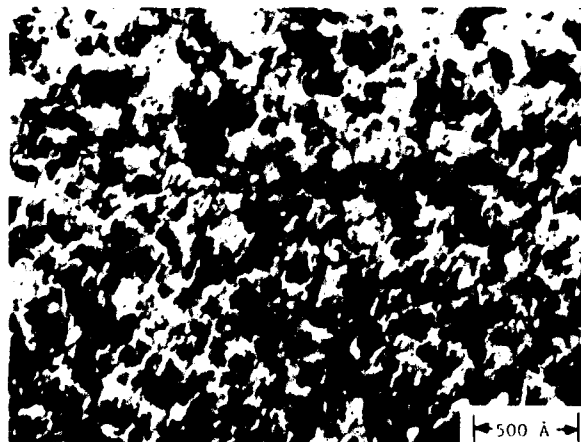


Fig. 8 TEM planar view of Pt_2Ga on Si.

Discussion

The results of Fig. 2 through Fig. 7 are summarized in Tables I and II. Table I lists the Pt-Ga intermetallic phase resistivity values at 77 °K and 300 °K and the appropriate host substrate used. Table II lists the temperature absolute resistivity coefficient (TARC) defined as:

$$\text{TARC} = R_{300} - R_{77} \quad (1)$$

and the temperature relative resistivity coefficient (TRRC) defined as:

$$\text{TRRC} = (R_{300} - R_{77}) / (300 - 77) / ((R_{300} + R_{77}) / 2) \times 10^6 \quad (2)$$

Resistivity ($\mu\Omega\text{-cm}$)			Resistivity Coefficients of the Pt-Ga Phases		
Table I			TABLE II		
Pt-Ga Phase	77 °K	300 °K	Pt-Ga Phase	TARC ($\mu\Omega/^\circ\text{C}$)	TRRC (ppm/ $^\circ\text{C}$)
PtGa ₂ -GaAs	11	18	PtGa ₂ -GaAs	0.012	2165
PtGa-GaAs	285	362	PtGa-GaAs	0.345	1967
Pt ₂ Ga-GaAs	114.8	119	Pt ₂ Ga-GaAs	0.019	141
PtGa ₂ -Si	32	62	PtGa ₂ -Si	0.145	1862
PtGa-Si	2190	2045	PtGa-Si	-0.650	-1307
Pt ₂ Ga-Si	1592	1533	Pt ₂ Ga-Si	0.265	1119

As can be seen from Table I, the Pt-Ga intermetallic phase and host substrate strongly influence and determine the transport properties. In particular, resistivity behavior ranging from highly metallic to virtually semiconducting has been observed. Very little is known about the bulk properties of PtGa or Pt₂Ga from either a fundamental or practical standpoint. It is difficult to develop a comprehensive model or theory to explain the electrical transport properties of these materials. Future work will focus on the determination of the band structure and the density of states calculation of these materials.

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GROWTH AND CHARACTERIZATIONS OF GaAs ON InP WITH DIFFERENT BUFFER STRUCTURES BY MOLECULAR BEAM EPITAXY

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ABSTRACT

We report the growth and characterizations of 3 μ m thick GaAs films grown on (100) InP substrates by MBE employing different buffer layer structures during the initial deposition. The buffer layer structures under study are: 1) GaAs layer grown at low temperature; 2) GaAs layer grown at low temperature plus two sets of In_{0.08}Ga_{0.92}As/GaAs strained layer superlattices (SLS) and 3) a transitional compositionally graded In_xGa_{1-x}As layer between the InP substrate and the GaAs film. After the buffer layer deposition, the growth was continued by conventional MBE to a total thickness of 3 μ m for all samples. From the 77K photoluminescence (PL) measurement, it was found that the sample with SLS layers has the highest PL intensity and the narrowest PL linewidth. Cross-sectional transmission electron microscopy (TEM) studies showed that the SLS is effective in reducing the propagation of threading dislocations and explains the observed superior optical quality from the PL measurement.

INTRODUCTION

Recently, there has been an increasing interest in GaAs on InP heteroepitaxy as a means to combine the better developed GaAs electronic devices with InP based optical devices for monolithic optoelectronic integration at 1.3 to 1.5 μ m range. Successful fabrications of GaAs on InP waveguides[1], MESFETs[2] and quantum well lasers[3] have been demonstrated by both MOCVD and MBE. These results showed that despite the large difference in the lattice constants (3.7%) and thermal expansion coefficients ($\alpha_{GaAs}=6.63 \times 10^{-6} \text{C}^{-1}$ $\alpha_{InP}=4.56 \times 10^{-6} \text{C}^{-1}$)[4] between the two materials, device quality GaAs films on InP substrate can be grown easily. Even so, there

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have been almost no effort made to study the effect of initial buffer layer deposition on the film quality. In this paper, we investigate the growth and characterizations of GaAs on InP with different buffer layer structures using MBE. It is expected that with further investigation of the growth method, the crystalline quality of GaAs films on InP can be improved significantly. The buffer layer structures under study are: 1) a low temperature grown GaAs layer; 2) a low temperature grown GaAs buffer layer plus two sets of $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}/\text{GaAs}$ strained layer superlattices (SLS) and 3) a transitional compositionally graded $\text{In}_x\text{Ga}_{1-x}\text{As}$ buffer layer ($x=0.53$ to 0.08) between the InP substrate and GaAs film. The optical and structural qualities of these films were evaluated by 77K photoluminescence (PL) and cross sectional transmission electron microscopy (TEM) respectively.

EXPERIMENTAL

The substrates used for all experiments described here were exact (100) oriented S-doped n^+ InP substrates. After regular degreasing steps, the InP wafers were etched in 4:1:1 $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ and Bromine-methanol sequentially before loading into the MBE chamber. The thin oxide layer was desorbed by heating the substrates to 470°C for 7 minutes in the growth chamber under an As overpressure. After oxide desorption, $3\mu\text{m}$ thick regular undoped GaAs films were grown on different buffer structures as shown in Fig.1(a) through (c). In sample (a), the initial 900\AA buffer layer was grown at 300°C at a growth rate of $0.33\mu\text{m}/\text{hour}$. The growth was then interrupted and the substrate temperature was raised to 560°C for 5 minutes under As flux before resuming regular growth. Sample (b) was grown under identical conditions as sample (a) except that 2 sets of 5-period $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}/\text{GaAs}$ SLS were incorporated. The SLS layers were grown at 460°C followed by growth interruption and annealing at 640°C for 5 minutes. The sublayer thicknesses were 100\AA for $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}$ layers and 92\AA for GaAs layers respectively. The first set of SLS was grown after the low temperature GaAs buffer layer and the second set of SLS was grown after $1\mu\text{m}$ of regular deposition. In sample (c), the growth was initiated by depositing a 500\AA thick $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer which was designed to be lattice matched to the InP substrate, followed by grading the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer from $x=0.53$ to $x=0.08$ over a thickness of 1000\AA . This was done by lowering the In oven temperature manually. Subsequently two sets of SLS followed by growth interruption and annealing were also included as in sample (b). The growth

temperature and growth rates for the rest of the films were kept at 560°C and 1 $\mu\text{m}/\text{hour}$ respectively. The total thickness was 3 μm for all samples. The morphology of all samples was good. The 5145 Å line of an Ar⁺ laser was used as the excitation source at a power density of 30 W/cm² in the PL measurement. The cross sectional TEM were taken on JEOL TEM 200CX electron microscopy with a point to point resolution of 2.9 Å.

RESULTS AND DISCUSSIONS

The PL spectra of all samples are shown in figure 2. The PL spectrum of an undoped GaAs on GaAs sample is also included for comparison. The peaks of GaAs on InP samples are about 3 meV lower than that of GaAs peak, indicating that the film is under tensile stress. The magnitude of the stress is however smaller than that is expected from a simple estimate of $(\alpha_{\text{GaAs}} - \alpha_{\text{InP}})\Delta T$. No double peaks were observed in all PL spectra obtained from all samples. As can be seen from Fig.2, the PL intensity of sample (b) grown with two sets of SLS is significantly higher than sample (a). The linewidth of sample (b) is also the narrowest among the three samples.

The results of cross sectional TEM are shown in Fig.3(a) through (d). Due to the large mismatch in the lattice constants between the two materials, a very high density of threading dislocations arising from the interface (10^8 – $10^9/\text{cm}^2$) are observed for sample (a) and (b). For sample (b), however, significant bending of the threading dislocations by the second set of SLS about 1 μm away from the heterointerface can be seen. Although the bending of dislocations is not clear for the first set of SLS near the interface due to the high dislocation density, it is observed that the dislocation density is reduced substantially after the growth of SLS. The effect of InGaAs/GaAs SLS in bending threading dislocations is thus applicable for GaAs/InP heteroepitaxy as in the case of other heteroepitaxial systems such as GaAs/Si[5], although the average lattice constant of SLS is not matched with either the films or the substrates. In sample (c), an extremely high dislocation density near the interface is observed. Careful examination shows that the threading dislocations are not generated at the initial $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ layer which is lattice matched to the InP substrate as shown in Fig.3 (d), but in the graded transitional InGaAs region. Since the graded layer is rather thin, it is possible that the strain in this layer has exceeded the critical value for the generation of dislocations. Even though this may be the case, the much higher threading dislocation density found here suggest that there may be other mechanisms responsible for the propagation of

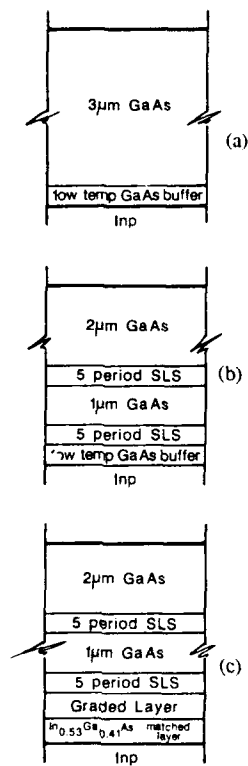


Fig.1 Schematics of different buffer structures: (a) Low temperature grown GaAs buffer layer; (b) 2 sets of $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}/\text{GaAs}$ SLS; (c) Transitional graded $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer plus 2 sets of $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}/\text{GaAs}$ SLS.

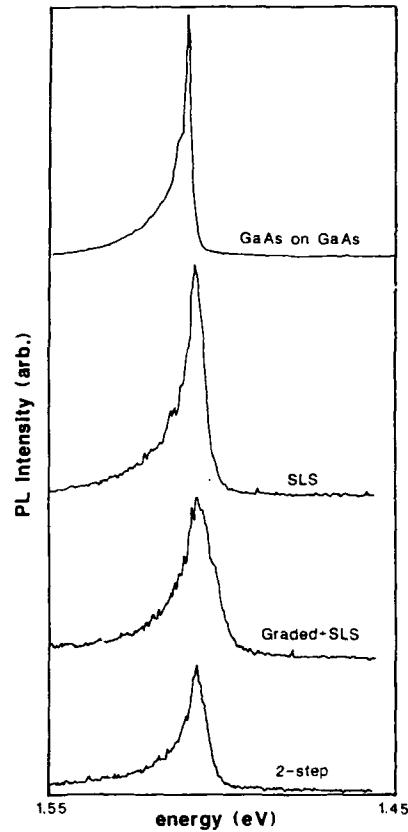


Fig.2 77K photoluminescence spectra from GaAs on InP and GaAs on GaAs films. The spectrum from GaAs on GaAs film is in different scale.

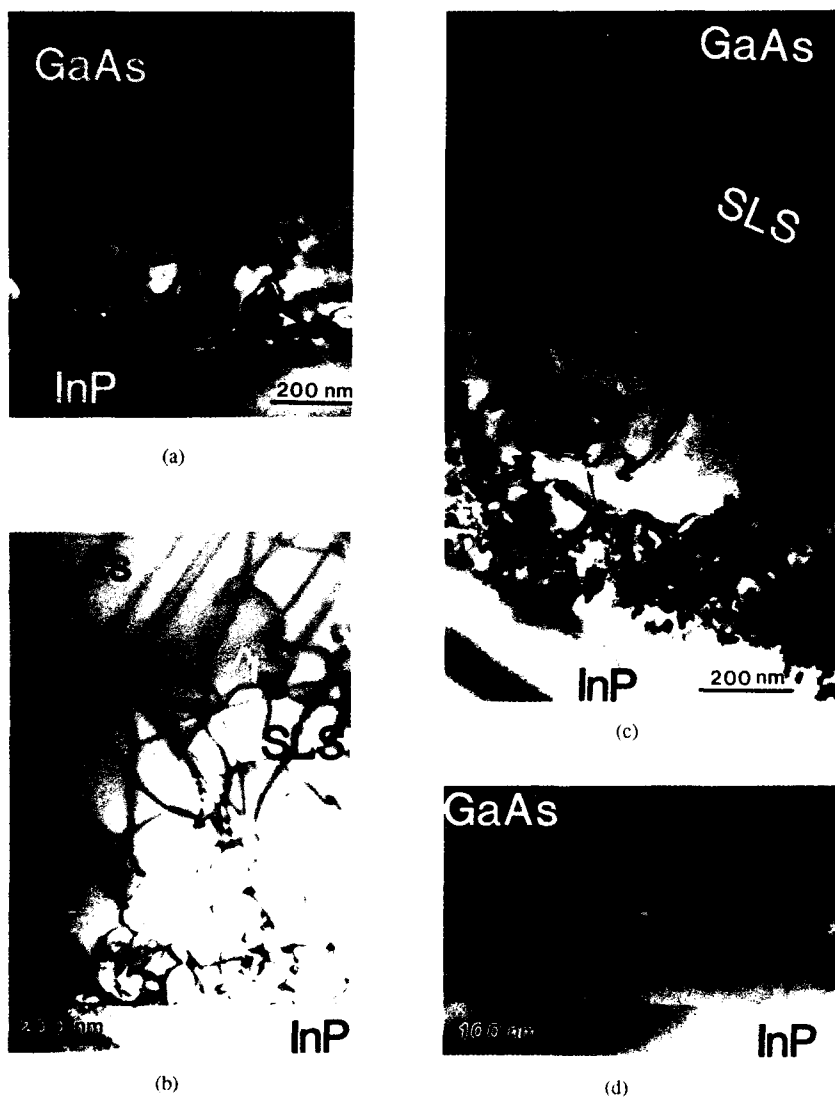


Fig.3 Cross sectional TEM micrograph from: (a) The film with low temperature grown GaAs buffer layer; (b) The film with low temperature GaAs buffer layer and 2 sets of $\text{In}_{0.08}\text{Ga}_{0.92}\text{As}/\text{GaAs}$ SLS; (c) The film with transitional graded $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer and 2 sets of SLS; (d) the interface of same sample as (c).

these misfit dislocations. The strain field generated by this compositionally graded layer may have aided the propagation of the misfit dislocations generated in the graded layer during the growth. In sample (c), the effect of SLS in bending dislocations is clearly visible as indicated by the "SLS" in Fig.3(c), thus proving that InGaAs/GaAs SLS is effective in reducing the propagation of threading dislocations in heteroepitaxial GaAs on InP films.

SUMMARY

In summary, we have reported the characterizations of GaAs films grown on InP substrates by MBE using different buffer structures during the initial growth. From both 77K PL measurement and cross-sectional TEM studies, we conclude that the incorporation of InGaAs/GaAs SLS improved the optical and structural quality of the heteroepitaxial films.

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INTERFACIAL MICROSTRUCTURES IN $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ STRAINED LAYER STRUCTURES

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ABSTRACT

The interfacial microstructures of lattice strained $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ multiple layer structures, that were grown by molecular beam epitaxy (MBE) on GaAs (100) substrates, have been investigated and characterised by transmission electron microscopy (TEM). A g_{311} weak beam imaging technique has been used to study structural imperfections at the heterointerfaces. The morphology of rough heterointerfaces, which resulted from the growth of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers (strained layer) either in a two dimensional (2D) or in a three dimensional (3D) growth mode via island formation, was imaged using this technique. A transition from 2D to 3D growth was found to occur at a certain critical layer thickness which decreased with increasing indium fraction. In thicker layers, dislocation complexes, which may have been caused by the formation of islands, were also observed. These complexes were primarily composed of stacking faults bounded by partial dislocations.

INTRODUCTION

The structural quality of $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterostructures is of importance for their electronic and opto-electronic properties. Defect structures, such as misfit dislocations, lead to degradation of their transport and optical properties. A number of experiments have been made on strained layer structures to determine the critical layer thickness (t_c), below which the lattice mismatch between the epitaxial layers can be totally accommodated by homogeneous layer strain [1-3]. At thicknesses above t_c , misfit dislocations are generated to relieve some of the strain energy. Experimental measurements of t_c are often in agreement with the Matthews and Blakeslee theory for t_c [4].

A number of structural imperfections other than misfit dislocations have been observed in $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterostructures with indium fractions (x) higher than 0.3. It has been found, by reflection high energy electron diffraction, that a transition from a 2D growth to a 3D growth mode can occur during fabrication by MBE [6-10]. Defect structures, such as local strain variations, non-planar interfaces, dislocation complexes as well as misfit dislocations, have all been observed by TEM [5, 7, 11, 12]. It is important for the fabrication of high quality strained heterostructures that the dependence of these defect structures on fabrication variables be determined.

In this investigation TEM has been used to investigate the development of interfacial microstructures in lattice strained $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ multiple layers. In addition to conventional TEM imaging techniques [13], including the g_{200} dark field imaging technique [14 - 16] with which sharp contrast across the heterointerfaces can be obtained, a recently developed weak beam imaging technique [17] has been employed to image non-planar interfaces. In this technique, a g_{311} reflection is used to form the image.

Fig. 1 shows the diffraction conditions under which this weak beam imaging is carried out. A (100)-type $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ single strained layer structure is tilted to obtain the diffraction conditions for g_{311} weak beam imaging. Each reciprocal lattice point is split because of the homogeneous layer strain in the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer. This strain only occurs in the (100) growth direction. The specimen is oriented so that the Ewald sphere cuts between the split reciprocal lattice points at 311 . The 933 reciprocal lattice point of GaAs is at the exact Bragg condition, i. e. there is a $g(3g)$ weak beam condition for g_{311} . Compared to the two beam condition, the contribution to the intensity of the g_{311} diffracted beam from GaAs is decreased since its recip-

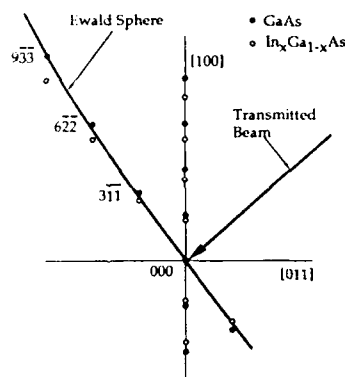


Fig. 1. Schematic diagram showing split reflections in the reciprocal lattice of a homogeneously strained $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ single strained layer structure. The Ewald sphere is drawn for the $g(3g)$ diffraction condition for g_{311} weak beam imaging. The foil is tilted so that the strained layers are inclined at an angle of $\sim 25^\circ$ to the beam direction.

cal lattice point is off the Bragg condition. By contrast the contribution from the strained layer is increased since its reciprocal lattice point lies closer to the Ewald sphere than it would be in the GaAs g_{311} two beam condition. In this imaging condition, the contrast is very sensitive to the detailed microstructure of the layer [17].

For (011)-type cross-sectional TEM specimens prepared from strained $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ multiple layer structures grown on (100) type substrates, fringes that are parallel to the intersection of the heterointerface with the surface of the specimen can be observed. These have a periodicity that is the same as that of thickness fringes. The intensity of these strained layer fringes increases with increasing strained layer thicknesses up to a certain value [17], which is in a similar range as the t_c given by the Matthews-Blakeslee theory [2].

EXPERIMENTAL

A set of multiple strained layer structures were grown on GaAs (100) in a Varian MBE-360 system. The thin $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers were separated by thick GaAs layers (100 - 200 nm) and the thickness of each successive $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer was increased by nominally one monolayer (ML) (2.82\AA for GaAs). The indium fraction, x , in each strained layer was constant for each multiple layered sample and was selected to be some value in the range 0.5 to 1.0. The strained layer thickness, t , and its indium fraction, x , were predetermined by means of the beam flux calibration. The substrate temperature was $530 - 550^\circ\text{C}$ during growth of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers. A $1\text{-}\mu\text{m}$ -thick GaAs buffer layer was grown on the substrate before the strained layer structures were grown.

Cross-section thin specimens were prepared from these MBE samples for investigation by TEM. The normal of the specimen foil was parallel to the [011] direction. After conventional mechanical thinning, the specimen slice was thinned by a modified ion beam thinning technique, in which the specimen was sputtered by argon ions at 3 - 5 keV, at an incidental angle of $\sim 15^\circ$, from one side of the specimen at a time without the specimen stage being rotated [18]. The resulting thin foils were investigated in a Jeol 2000FX instrument operated at 200 kV.

RESULTS AND DISCUSSION

2D growth

Fig. 2 is a g_{311} weak beam image, taken at a $g(3g)$ diffraction condition, showing the first



Fig. 2. A g_{311} weak beam image of a set of $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$ multiple layers taken at the $g(3g)$ diffraction condition. The domain-like contrast pattern on the 2-ML-thick layer reveals interfacial roughness resulting from growth in a 2D mode.

three strained layers in an $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$ multiple layered structure. The thicknesses of the individual strained are given in ML. The 1-ML-thick layer has uniform strained layer fringes and is thus homogeneously strained. The 2-ML-thick layer has a domain-like pattern in the intensity of these fringes and this variation in contrast is consistent with a difference in thickness between bright and dark regions [17]. It can be noted that the dark areas are of approximately the same intensity as that for the 1-ML-thick layer. The real thickness of this layer probably varies from 1 ML, in the regions of darker contrast, to 2 ML:s or more in the bright domains. The domain-like pattern is thus consistent with the presence of an interfacial roughness resulting from a 2D growth mode, i. e. growth by the addition of atoms to ledges that propagate across the growth surface. The non-homogeneous nature of the intensity in the regions of bright contrast suggests that parts of these may be more than 2 ML:s thick. The contrast of much of the 3-ML-thick layer in this image seems to be saturated such that some contrast details can hardly be observed.

3D growth

In order to improve the contrast from the interfaces of these layers, that had thicknesses of 3 ML:s or more, another g_{311} weak beam image was taken at a $g(4g)$ diffraction condition. As shown in Fig. 3, this increased the differences in contrast arising from interfacial roughness in the thicker layers. A fine dispersion of small regions of bright contrast can be seen on the 3-ML-thick layer. These small areas (arrowed 3D), which are $\sim 10\text{-}20\text{ nm}$ in diameter, are thicker than their surrounds [17]. Their number density is about $1.4 \times 10^3 (\mu\text{m})^{-2}$. The uniformity and size of these thicker regions suggests that this interfacial roughness arises from a 3D mode of growth.

The domain-like pattern due to 2D growth can still be recognized in the 2-ML-thick layer at this $g(4g)$ diffraction condition, but the contrast is not as strong as that at the $g(3g)$ condition. The maximum intensity of the strained layer fringes in the regions between the bright islands in the 3-ML-thick layer appears to be similar to that in the bright domains of the 2-ML-thick layer. No obvious domain-like pattern can be observed in the 3-ML-thick layer and therefore, it seems that the small 3D islands formed after completed 2 ML:s.

Dislocation complexes

Cluster-like contrast arrowed DC in Fig. 3, could be observed in strained layers thicker than 5 ML:s. The size of these clusters increased with increasing thickness of the strained layer. The diffraction contrast around these clusters suggests there are considerable lattice strain variations associated with them. In the g_{200} dark field image of Fig. 4, stacking faults (arrowed) associated with significant variations in strain can be observed in the layers which are thicker than 5 ML:s. These stacking faults are generated from the strained layers and extend into the GaAs separation layers. For the 5 and 7-ML-thick layers, the stacking faults increase in number with increasing layer thickness of the strained layers but they are still confined to regions close to the strained layers. For strained layers as thick or thicker than 9 ML:s the stacking faults extended through the separation layer. Comparison between Figs. 3 and 4 suggests that the cluster-like contrast is due to dislocation complexes which mainly consist of stacking faults bounded by partial disloca-

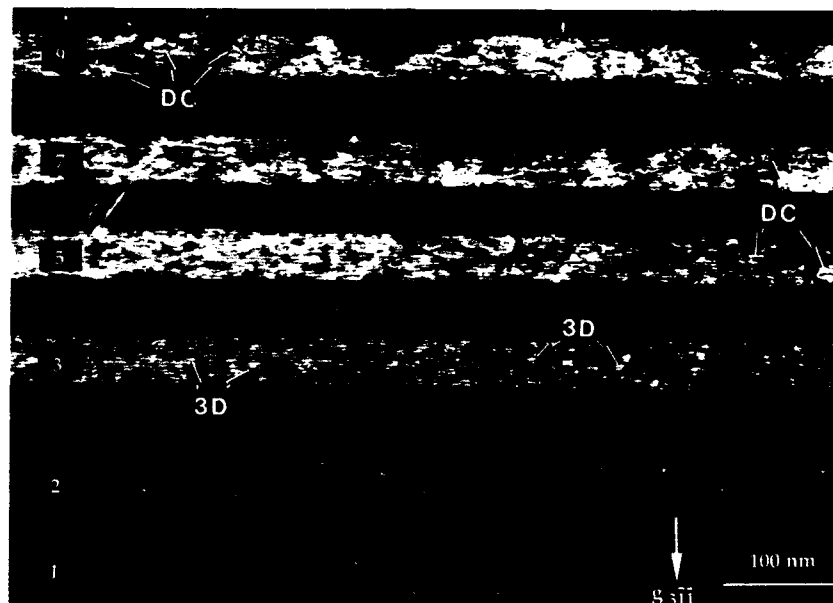


Fig. 3. A g_{311} weak beam image of $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$ multiple layered structure taken at a $g(4g)$ diffraction condition. The distribution of small regions with bright contrast (arrowed 3D) for the 3-ML-thick layer suggests that a fine distribution of islands formed during growth in a 3D mode. Dislocation complexes (arrowed DC), were generated at thicker layers.



Fig. 4. A g_{200} cross-sectional dark field image of the $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{GaAs}$ multiple layered structure showing the development of dislocation complexes with increasing of strained layer thicknesses.

tions. These dislocation complexes are probably generated by the significant local strain variations that arise because of island formation during growth of the strained layer in a 3D mode.

Misfit dislocations

Misfit dislocations have been observed in previous work [5] on similar materials at strained thicknesses less than that at which the dislocation complexes were formed. These misfit dislocations had a 60° mixed character with $\langle 011 \rangle$ directions and formed rectangular networks at the interfaces of the strained layers. No such misfit dislocations were observed in the present set of MBE samples. The possibility exists that the present samples were grown at a somewhat higher substrate temperature than previously and this caused 3D growth to occur at lower strained layer thicknesses. This would have resulted in the generation of dislocation complexes to release lattice strains and this may have precluded the generation of misfit dislocations.

Critical thicknesses

Three different critical thicknesses, corresponding to different defect structures, can be identified in heterostructures of this type [5]:

- (1) t_{3D} : the onset of 3D growth via island formation after initial 2D growth;
- (2) t_M : the generation of misfit dislocations which are 60° mixed dislocations in $\langle 011 \rangle$ directions that form rectangular networks at the lower interfaces of the strained layers; and
- (3) t_{DC} : the generation of dislocation complexes which mainly consist of stacking faults on $\{111\}$ planes.

The characteristic microstructural features of each strained layer in four different multiple layered samples are plotted in Fig. 5. The two solid curves show the dependence of the experimental values of t_{3D} and t_{DC} on the thickness and indium content of the strained layers. No misfit dislocations were observed for these multiple layers and therefore no experimental curve can be drawn for t_M . The broken curve, indicated by $t_{M(M\&B)}$, corresponds to the theory of Matthews and Blakeslee [2]. From Fig. 5 it can be concluded that, for a given x , initial growth was in a 2D

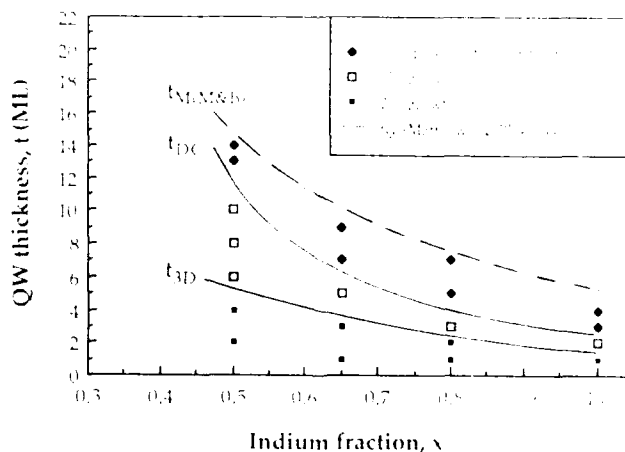


Fig. 5. The dependence of interfacial microstructure on strained layer thickness and indium fraction. t_{3D} and t_{DC} are the critical thicknesses for the onset of 3D growth and for the generation of dislocation complexes. $t_{M(M\&B)}$ is a theoretical curve for the critical thickness for generation of misfit dislocations as calculated from the Matthews and Blakeslee theory [2].

mode but this subsequently transformed at t_{3D} to a 3D growth mode via island formation. Dislocation complexes (stacking faults) were generated at t_{DC} .

CONCLUSIONS

1. A weak beam imaging technique has been used to reveal the interfacial microstructures of strained layers in an inclined projection.
2. It was found that the growth of the strained layer initially took place in a 2D growth mode. This resulted in a domain-like pattern of interfacial roughness, i. e. lattice incorporation at surface steps was the dominating growth mechanism for layer growth.
3. Rough interfaces with small islands scattered on the strained layer were observed in thicker strained layers and this corresponded to the onset of 3D growth.
4. Dislocation complexes (stacking faults) were observed in strained layers that were thicker than a critical thickness, t_{DC} .
5. No misfit dislocations were observed.
6. For a given indium fraction, $t_{3D} < t_{DC} < t_{M\&B}$.

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EXPERIMENTAL AND THEORETICAL ANALYSIS OF STRAIN RELAXATION IN $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ HETEROEPI TAXY: R. Hull and J.C. Bean, AT&T Bell Laboratories, 600 Mountain Avenue, Murray Hill, NJ 07974

ABSTRACT

By analyzing in-situ strain relaxation measurements of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ epitaxy in a Transmission Electron Microscope, we are able to quantify the fundamental parameters which describe strain energy relaxation via misfit dislocation introduction. Quantitative descriptions of misfit dislocation nucleation, propagation and interaction processes are derived. The numerical parameters obtained from these experiments are then incorporated into a predictive theoretical model of strain relaxation which relies only upon experimentally measured quantities. Good agreement between experiment and theory is obtained over a wide range of data.

INTRODUCTION

Many theoretical models have been developed to predict the breakdown of coherent or commensurate growth in strained layer epitaxy (e.g. 1-4). It is generally recognized that equilibrium models (1,2) under-estimate experimental measurements (5,6) of the critical thickness transition between strained and dislocated growth in the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ system, particularly at a relatively low growth temperature of 550°C (5), as shown in Figure 1. This discrepancy can be explained by taking into account two concepts: (i) the finite sensitivity of experimental techniques used to measure the critical thickness transition (7) and (ii) an accurate quantitative incorporation of finite dislocation nucleation and growth rates (4,8,9). When these effects are taken into account, kinetic modelling of time-dependent strain relaxation (4) in the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ system can accurately predict experimental data. Such modelling has demonstrated the crucial importance of kinetic effects in understanding elastic strain relaxation via generation of misfit dislocation line length, but experimental understanding of the dynamic defect processes involved has hitherto been lacking. In this paper, we describe in-situ strain relaxation observations of $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ structures in a Transmission Electron Microscope (TEM) which enable us to observe dynamic misfit dislocation phenomena such as nucleation, propagation and interaction processes, and to quantify the parameters describing each of these events. These quantified parameters can then be used to develop a predictive model of strain relaxation which relies only upon experimentally measured quantities.

EXPERIMENTAL

All $\text{Ge}_x\text{Si}_{1-x}$ layers described here are grown nominally undoped as single layers upon a free $\text{Si}(100)$ surface by Molecular Beam Epitaxy (MBE) as described elsewhere (10). Standard growth conditions correspond to a substrate temperature of 550° C and a growth rate of $3\text{\AA}/\text{sec}^{-1}$, unless otherwise indicated. Structures are grown in a composition/thickness regime where the equilibrium prediction (2) of critical thickness is exceeded, but experimental measurements (5) indicate an undetectable amount of strain relaxation. As indicated by Figure 1, this "metastable" regime extends through a relatively wide range of thicknesses for low x layers. Our as-grown structures thus exhibit zero or very low levels of misfit dislocations to the level of sensitivity attainable in the TEM. Thin foil plan view TEM samples are then prepared by standard etching techniques and the sample is heated in-situ in a Gatan single-tilt heating holder (11) equipped with a Pt-Rh thermocouple in a JEOL 2000FX TEM. At temperatures \geq the original growth temperature, kinetic barriers to the formation and motion of misfit dislocations are overcome and dynamic defect processes may be observed in real-time, and recorded either statically using standard photographic negatives or dynamically using a TV camera and video recording.

The experimental geometry is summarized in Figure 2 and discussed in more detail in (12). In brief, plan-view samples are employed, as in the cross-sectional geometry surface diffusion across exposed interfaces might invalidate the experiments. For quantitative measurements, thin foil effects must be considered and the most severe restriction is that the infinite substrate approximation not be too severely abrogated. Such considerations and others lead to determination of a composition range $x \sim 0.25-0.35$ and epilayer thicknesses of the order of hundreds of Angstroms as being optimum for quantitative experiments.

We frequently employ during growth shuttering of parts of the wafer surface from the incident beam flux to obtain a range of layer thicknesses on a single wafer. As the wafer cannot be rotated under such circumstances and compositional nonuniformities may result, alloy composition is often directly measured by a combination of Rutherford Backscattering Spectroscopy (RBS, to obtain the no. of Ge atoms per unit area) and cross-sectional TEM (to obtain the layer thickness, and hence composition via the RBS measurements).

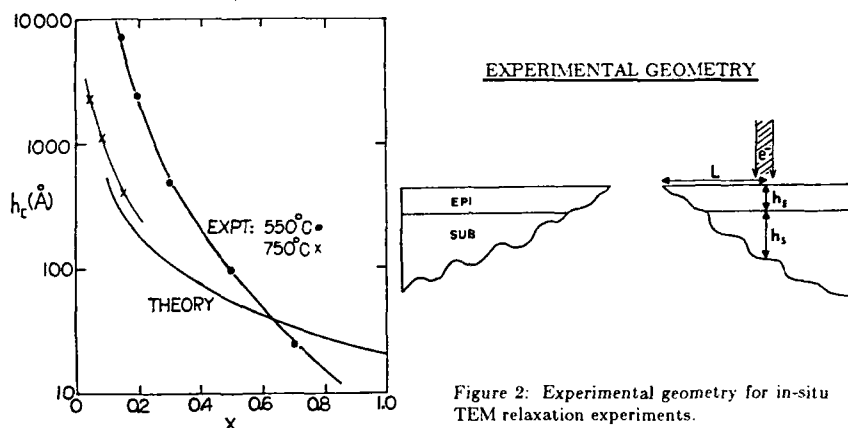


Figure 1: Comparison of the Matthews and Blakeslee model (2) for equilibrium critical thickness in the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ system with experimental measurements of critical thickness at 550°C (5) and 750°C (6).

RESULTS

Much of our in-situ relaxation work has been published elsewhere (e.g. 12-16); in this section we will reproduce only those results relevant to theoretical discussions later in this paper.

In Figure 3 we show Arrhenius plots of (a) dislocation velocity and (b) dislocation density during thermal annealing of a $340 \pm 20 \text{ Å Ge}_{0.25 \pm 0.03}\text{Si}_{0.75 \pm 0.03}/\text{Si}(100)$ structure. The dislocation velocity is calculated from frame-by-frame measurements from real-time video recording; the upper limit to the velocity which may be measured corresponds to when the defect crosses the field of view in only a few video frames (at the lowest objective lens magnification, this limits measurements to velocities $< \sim 100 \text{ micron} \cdot \text{sec}^{-1}$ which typically occurs at temperatures of the order 800°C. Velocities at the original 550°C growth temperature are of the order of a few $\text{microns} \cdot \text{sec}^{-1}$). Dislocation densities are calculated by counting the number of dislocation ends which are visible in a given area, and then dividing by two to determine the number of misfit dislocations, assuming each misfit dislocation segment terminates by threading to the nearest free surface (the growth surface).

The activation energy measured for glide of 60-degree dislocations (Figure 3(a)) is $1.1 \pm 0.2 \text{ eV}$, with a prefactor of $20 \text{ m} \cdot \text{sec}^{-1}$. This is significantly lower than measurements of the bulk activation energy for glide in Si and Ge, 2.2 and 1.6 eV respectively (e.g. 17,18). Possible reasons for this discrepancy between bulk and thin strained film values are discussed in (14). One possibility, originally suggested by Dodson (19), is that the glide activation energy will be stress-dependent and may be significantly lowered at the very high excess stresses, of the order 1 GPa, involved in the structures studied here. This concept will be invoked in our theoretical modelling of strain relaxation, as will be discussed in the next section of this paper.

The observed thermal nucleation barrier to dislocation nucleation (Figure 3(b)) is $0.3 \pm 0.2 \text{ eV}$. The detailed mechanisms of dislocation nucleation in these $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ structures are still not fully understood, but understanding to date is summarized in (15,20) and elsewhere in these proceedings (21).

Another process which is found to be of great significance in determining the rate of strain relaxation, particularly in films of the order a few hundred Å thick, is dislocation interactions. As we have discussed in detail in (13), a propagating defect may be effectively pinned by a pre-existing orthogonal dislocation if the Burgers vectors of the two dislocations are parallel and produce a mutually repulsive force which is of sufficient magnitude to make the net force driving dislocation motion negative.

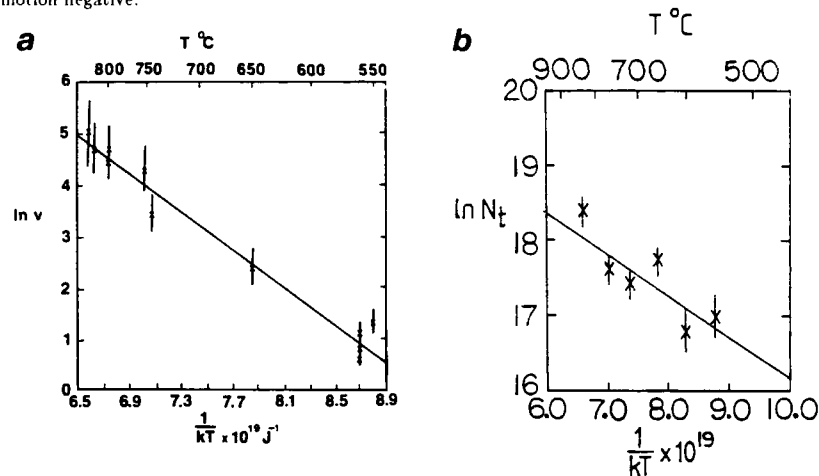


Figure 3: Arrhenius plot of the natural logarithm of (a) measured dislocation glide velocities and (b) misfit dislocation density vs. inverse annealing temperature in a $\text{Ge}_{0.28}\text{Si}_{0.72}$ layer.

THEORETICAL MODELLING

Using only experimental parameters measured or inferred from our in-situ experiments, we have developed a predictive model of strain relaxation in the $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ system. Fuller details of this model will be published elsewhere (22), but preliminary results are described here.

Our model is based upon the simple relationship that the total misfit dislocation length in a structure (and hence its strain state) will be equal to the sum of the lengths of each individual misfit dislocation segment in the structure. The length of each dislocation segment will simply be equal to the time integral of its velocity during the relaxation (annealing or growth) sequence. Thus the total dislocation length at a time t , $L(t)$, will be given by the time integral of the number of growing dislocations at each intermediate time t' , $N(t')$, multiplied by their velocity, $v(t')$:

$$L(t) = \int_{t_i}^t N(t') v(t') dt' \quad (1)$$

The lower time limit to the integral, t_i , is taken to be the time at which the Matthews-Blakeslee equilibrium critical thickness (2) is exceeded in growth sequences, or at $t=0$ for annealing sequences. The velocity, $v(t')$, is given according to Dodson and Tsao (4) by:

$$v(t') = v_0 e^{\frac{-E_v(\sigma)}{kT}} \sigma_{\text{excess}}(t') \quad (2)$$

Here $v_0 \sigma_{\text{excess}}(t') = 20 \text{ m.sec}^{-1}$ from our measurements and $E_v(\sigma)$ is the activation energy for dislocation glide, which as suggested by Dodson may be stress dependent, and σ_{excess} is the excess stress driving the dislocation motion. As described by Matthews and Blakeslee (2) and Dodson and Tsao (4), this is equal to the misfit stress acting on the dislocation line, minus the dislocation line tension. Expressions for the appropriate stresses/forces are given in (2) and (4); for the layer and dislocation geometries considered in our in-situ experiments of Figure 3, the magnitude of σ_{excess} is $\sim 0.6 \text{ GPa}$. Following Dodson (19), we use for the stress dependence of the glide activation energy:

$$E_v(\sigma) = E_v(0) \left[1 - \frac{\sigma}{\sigma_c} \right] \quad (3)$$

Where $E_v(\sigma)$ from our measurements is 1.1 ± 0.2 eV for $\sigma \sim 0.6$ GPa, $E_v(0)$ is the bulk value at zero stress (say 2.0 eV from interpolation of the values for Ge and Si), yielding $\sigma_c \sim 1.5$ GPa. The quantity σ_c is analogous to the zero-temperature flow stress (that stress at which defect motion has a zero activation energy) in metals. Its value is expected to be of the order 5-10% of the shear modulus in semiconductors, thus the value determined here appears to be a factor of the order 2-3x too low. Given the crude nature of the current estimate, however, such a discrepancy need not be too surprising (in metals the relationship between $E_v(\sigma)$ and σ involves power laws of $\sim 4/3$ rather than a simple linear dependence).

The number of growing dislocations at a time t' , $N(t')$, is given by:

$$N(t') = N_0 + N_1 t' e^{\frac{-E_0}{kT}} + N_m - N_p \quad (4)$$

Here N_0 is the density of pre-existing defects in the substrate or homoepitaxial Si buffer layer deposited prior to heteroepitaxial growth. The term $N_1 t' e^{\frac{-E_0}{kT}}$ represents the number of thermally nucleated dislocations, N_1 and E_0 having been determined from our in-situ experiments. The term N_m represents the number of dislocations generated by interaction/multiplication events such as the Hagen-Strunk mechanism (23); from our in-situ and static observations this term is essentially zero for the structures studied here. Finally, the term N_p represents the losses to the growing defect population arising from defect interaction/pinning processes as described above. Details of this modelling will be described in more detail in (22); in brief the probability is calculated that two given intersecting dislocations have parallel Burgers vectors, the magnitude of the inter-dislocation force is calculated along the propagating threading arm and it is determined whether or not propagation will continue. If pinning is expected, the probability is then multiplied by the number of defect intersections expected within the structure (this may be calculated geometrically) and the quantity N_p derived. (Note that even "pinnable" defects are allowed to grow to a length equal to the average expected distance to the first pinning event).

With the above relationships, eqn. (1) is evaluated numerically by iteration of 1 sec time steps, using the strain state from each preceeding iteration. Values used in eqns. (1) - (4) are: $G = 6 \times 10^{10} \text{ cm}^{-2}$; $\nu = 0.22$; $b = 4 \text{ \AA}$; $\sigma_c = 1.5 \text{ GPa}$; $E_v(0) = 2.0 \text{ eV}$; $v_0 = \frac{20 \text{ m} \cdot \text{sec}^{-1}}{6 \times 10^8 \text{ Pa}}$ (this value is normalized to the excess stress relevant to the data of Figure 3); $N_0 = 10^5 \text{ cm}^{-2}$; $N_m = 0$; $E_0 = 0.3 \text{ eV}$; $N_1 = 2.2 \times 10^6 \text{ cm}^{-2} \text{ sec}^{-1}$.

Preliminary results of comparison of this model with experimental data are shown in Figures 4 and 5. In Figure 4, we show experimental data from annealing experiments of a $\text{Ge}_{0.25,0.03}\text{Si}_{0.75,0.03}/\text{Si}(100)$ structure annealed for successive 4 minute intervals at each temperature for which a datum point is given. Experimental data is shown for (a) average measured distance between misfit dislocations, \bar{p} , (b) the areal density of misfit dislocation ends, N_t , and (c) the average misfit dislocation length, \bar{l} , calculated from the formula $\bar{l} = \frac{32}{\pi^2 N_t \bar{p}}$ derived in reference (14). Solid curves show the theoretical predictions of our model including the effect of dislocation interactions; broken curves show our theoretical predictions without taking into account misfit dislocation interactions. The thickness and composition regime of this sample is such that the inter-dislocation force can balance the excess stress over a distance $\sim 150-200 \text{ \AA}$ from a pre-existing misfit dislocation. In very thin layers such as analyzed in Figure 4, this can reduce the excess stress acting on a propagating threading dislocation to < 0 along its entire length. In thicker samples $> 1000 \text{ \AA}$, dislocation interactions are unlikely to pin propagating defects due to the limited extent of the inter-dislocation force, except towards the end of the relaxation process where the residual strain in the epilayer is very low and hence the excess stress acting on a dislocation also vanishes.

In Figure 5, we show experimental results and theoretical predictions for growth and growth+anneal sequences. Theoretical curves are shown for the average misfit dislocation spacing during growth of an $x \sim 0.24$ layer at $3 \text{ \AA} \cdot \text{sec}^{-1}$ for growth temperatures of 550 and 800°C and for a sequence consisting of growth at 550°C followed by an in-situ 10 minute 800°C anneal in the growth chamber. Experimental data for the 550°C growth and the growth+anneal sequences show agreement with theoretical predictions within a factor $\sim 2x$.

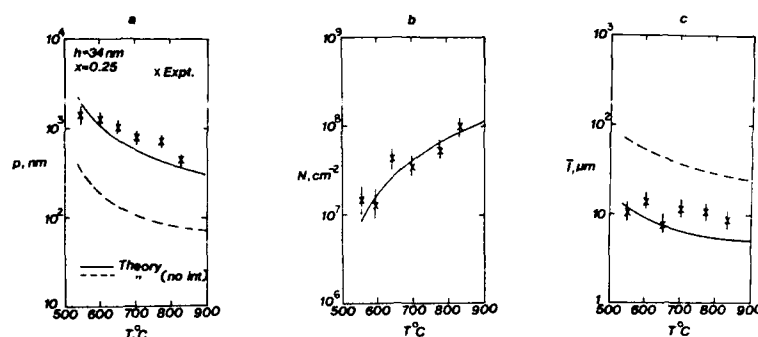


Figure 4: Theoretical predictions of (a) average distance between misfit dislocations (b) areal density of misfit dislocations and (c) average misfit dislocation length for successive 4 minute anneals at each of the temperatures for which experimental data is shown for a 340 Å $\text{Ge}_{0.26}\text{Si}_{0.74}$ layer. Curves are shown with (solid) and without (broken) dislocation interactions being taken into account.

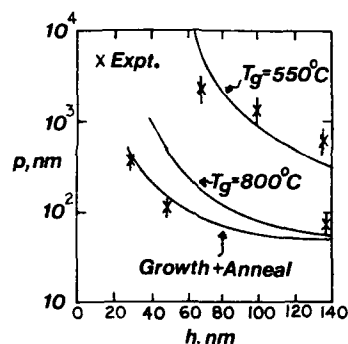


Figure 5: Theoretical predictions and experimental measurements of the average distance between misfit dislocations for $x=0.24$ $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ structures at growth temperatures of 550° and 800°C and for growth at 550°C followed by an in-situ 800°C anneal in the growth chamber.

CONCLUSIONS

It has been shown that in-situ relaxation of metastable $\text{Ge}_x\text{Si}_{1-x}/\text{Si}(100)$ layers in a TEM can produce direct and quantitative measurements of dynamic misfit dislocation processes. For Ge composition ranges $x \sim 0.25-0.35$, we have been able to study and decouple the effects of dislocation nucleation, propagation and interaction, deriving quantitative descriptions of each process.

The advantages of in-situ TEM measurements as opposed to other in-situ techniques which could conceivably be employed on metastably strained layers are (a) the high spatial resolution of the technique - of the order 100 Å even for conventional 2-beam diffraction contrast analysis and (b) the ease and precision of dislocation structure determination. These advantages allow studies of many orders of magnitude of the strain relaxation process (say average inter-dislocation spacings of the order 10 micron down to 100 Å), whilst over most of this range other in-situ techniques (X-ray topography, Electron Beam-Induced Current (EBIC) etc.) will have insufficient spatial resolution. The primary disadvantages of TEM are that (a) relaxation studies at very low relaxation levels are not

possible and (b) thin foil effects necessitate the use of very thin epilayers. In summary therefore, in-situ TEM measurements are of most use to study the later stages of relaxation, where the average dislocation spacing p varies from $\sim 10^{-8}$ – 10^{-6} m, whereas e.g. X-ray topography will be most useful in the region $p \sim 10^{-6}$ – 10^{-2} m. TEM is thus studying misfit dislocation interactions in what might be termed an "interacting environment" where misfit dislocation densities are high enough such that defects strongly influence each other. Care should thus be taken in interpreting e.g. nucleation and propagation activation energies (14), as these may be valid only in the interacting regime. On the other hand, given the crucial importance of dislocation interactions in the later stages of the relaxation process, lower resolution techniques suffer from not being able to study these interactions.

In applying experimentally measured parameters to our predictive model, therefore, we have in this paper restricted ourselves to theoretical modelling of geometries and compositions close to those measured. Within these limits, Figures 4 and 5 show that a simple theoretical model which uses experimentally measured parameters to evaluate the total line length of dislocation generated at a given stage of the relaxation process can predict experimental data with reasonable accuracy.

ACKNOWLEDGEMENTS

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COHERENCY STRAIN OF AN OVERGROWN ISLAND

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ABSTRACT

The lattice misfit strain in an overgrown island is considered to be accommodated by two distinctive domains; a pure coherency domain (ϵ domain) and a domain of misfit dislocations (δ domain). By introducing such two different constituents, the model predicts the transition condition from a "single phase" state (ϵ phase) to a "two-phase mixture" ($\epsilon + \delta$) as a function of misfit strain. Further, as in the chemical thermodynamics of a binary alloy system, energy vs. misfit strain diagrams allow us to understand possible existence of various metastable states which may be associated with an overgrowth.

INTRODUCTION

The defect structure of an overgrown island on a bulk substrate is an important factor in various fields such as solid state devices or ceramic coatings. One of the most prevalent defects present is misfit dislocation which can occur at the interface when the lattice misfit between the overgrowth and the substrate is significant. There have been several theoretical models addressing the question of what lattice misfit is necessary to induce dislocation formation and thus the loss of coherency at the interface [1-4]. As shown in Fig. 1, the boundary condition on the top and side surfaces of an overgrowth is rather complex, and thus, analytical elastic solutions for this problem are yet to be solved. Consequently, most continuum elasticity models [2,3] employ Eshelby's inclusion solution, rendering an overestimation for the coherency strain and the strain energy, when the aspect ratio, T/W is finite.

In this work, we first show the behavior of the exact coherency strain energy of an overgrowth in a plane strain condition. Based on these findings of the two-dimensional case, we consider the misfit strain to be accommodated by a pure coherency domain and a domain of misfit dislocation. Unlike the existing continuum models, however, the extent of the pure coherency domain is assumed less than the actual overgrowth thickness. For mathematical simplicity, the present analysis is limited to isotropic elasticity and rudimentary dislocation theory.

COHERENCY STRAIN IN A PLANE STRAIN CONDITION

Although no analytical solutions are available for the coherency strain, some numerical methods can provide the coherency strain and the strain energy for an overgrowth. One of the numerical methods is an atomistic approach, in which a triangular lattice is treated with linear atomic interactions. Hoover et al [5] demonstrated that a two-dimensional triangular lattice can simulate an elasticity problem in a plane strain condition. The potential energy of a triangular lattice having a uniform spring constant, κ , is given by

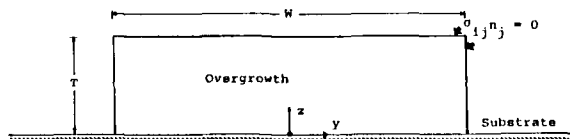


Fig. 1 A schematic for an overgrowth. $\sigma_{ij} n_j = 0$ indicates that the boundary condition is traction-free.

$$\Phi = \frac{\kappa}{2} \sum_{ij} (r_{ij} - d)^2 \quad (1)$$

where $r_{ij}^2 = y_{ij}^2 + z_{ij}^2 = (y_i - y_j)^2 + (z_i - z_j)^2$, and d is the triangular lattice parameter. The Lamé constants, λ and μ are, under a plane strain condition, given by $\lambda = \mu = 3\kappa/4$. The sub-indices i and j in y , z and r indicate the coordinates of the i th and j th atoms, not those used for a tensor notation. For a small displacement approximation, the calculation of Eq. (1) is limited to the first nearest neighbors for a given atom [6]. By calculating the force on an atom, one finds σ_{yy} stress component of i -th atom to be

$$\sigma_{yy} = \frac{4\mu}{3d^2} \sum_j \left(1 - \frac{d}{r_{ij}}\right) y_{ij}^2 \quad (2)$$

σ_{yz} and σ_{zz} can be obtained through permutations of y_{ij} and z_{ij} in Eq. (2). Within the region of an overgrowth, use of different spring constant, κ , and lattice parameter, d , suffices the coherency problem of present interest; $\kappa = \eta \kappa$ and $d = (1 + f) d$. If η is equal to 1, it represents an elastically homogeneous system, otherwise an inhomogeneous system. f is a lattice misfit strain. The elastic strain energy is then the potential energy of an equilibrium system for a given f , since the potential energy becomes zero when f is zero.

In Fig. 2, a three-dimensional perspective is displayed for a maximum principal stress, in units of μf [6]. The overgrowth has $W = 36d$, $T = 17.32d$, and $\mu = 2\mu$. The stress is found to be mostly confined in the neighborhood of the interface. With $f = +0.5\%$, the stress field starts with a strong compressive state at the interface area and diminishes as the distance from the interface increases. The behavior of the localized stress field is well demonstrated in the plot of strain energy vs. overgrowth thickness in Fig. 3. In Fig. 3(a), the strain energy, Φ/κ , is given for three different cases of μ^0 : 0.5μ , 1μ and 2μ . In all, the misfit strain, f , is 0.5% , and $W = 36d$. The strain energy is found to reach its plateau at the height of about $T = 18d$. In Fig. 3(b), $\mu^0 = 2\mu$ and $W = 18d$. Again, a plateau is attained at ca. $T = 10d$. For inclusions which are confined in an infinite matrix, it is well known that strain energy density depends only on the inclusion shape [7-10]. That is, the strain energy per unit area (or per unit volume for a three-dimensional case) of inclusion is a constant for a fixed ratio of T/W . For overgrowths, however, this is not true as demonstrated in Fig. 3. Due to the fact that the stress is localized in the proximity of the overgrowth-substrate interface, its strain energy density is found to depend both on the shape and on the size.

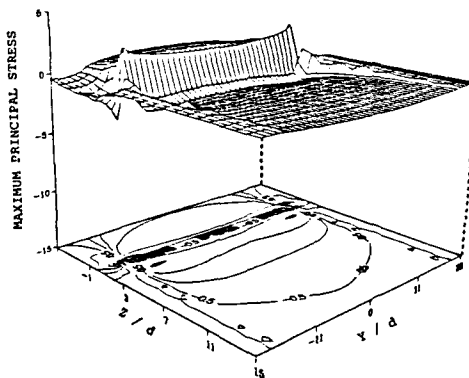


Fig. 2
A maximum principal stress
associated with an overgrowth.

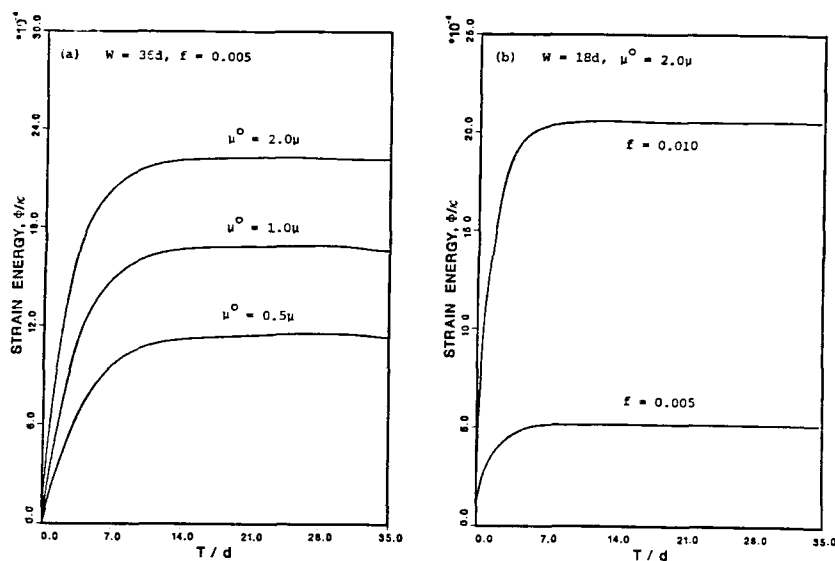


Fig. 3 Coherency strain energy vs. overgrowth thickness in a plane strain condition.

COHERENCY BREAKING AND THERMODYNAMIC CONSIDERATIONS

Though no atomistic calculations similar to the results of the previous section are demonstrated, it can be concluded that the findings for the plain strain case hold true for a three-dimensional overgrowth. Consequently, we question the use of the classical model for the elastic strain energy in predicting the coherency breaking for an overgrowth with a finite aspect ratio [2,3], and here present a new approach. Consider an overgrowth with dimensions of W , W , and T (Fig. 1). In the most general case, we assume that the lattice mismatch is accommodated by a combination of misfit dislocations and coherent elastic strain. In the limiting cases, however, a coherently strained overgrowth results when there are no misfit dislocations present, and a "relaxed" overgrowth results when the misfit dislocations have some specific spacing, designated here as $2R$, which completely accommodates the lattice mismatch and no pure elastic, or coherent, strain is present. When both plastic strain due to misfit dislocations and elastic strain are present, the region $2R$ at each misfit dislocation corresponds to a domain, a δ domain. In this most general case, the dislocations are separated by a distance greater than $2R$, and the regions in between the misfit dislocation domains correspond to elastically (coherently) strained domains, ϵ domains. The boundary between the δ and ϵ domain is located at a distance R from the dislocation center, and may be considered to correspond to that at which the strain field of the misfit dislocation in the interface plane is equal to that of the coherent strain, ϵ , but to maintain generality R will be taken as a parameter.

The ϵ domain is considered to extend to H in the direction perpendicular to the interface. When the thickness, T , is small, H is physically equal to T (for example, $T \leq 7d$ in Fig. 3). If not, as demonstrated in the previous section, H should be less than T . Again, for generality, we take H as a free

variable. When there is a square array of $2N$ misfit dislocations (N dislocations for each direction), the total energy due to misfit dislocations may be given as:

$$E_{\delta} = 2\gamma N W b^2 \quad (3)$$

where $\gamma = \mu[\ln(R^0/b)+1]/[\pi(1-\nu)]$, b is Burgers vector magnitude, ν is Poisson's ratio, and a is the lattice parameter of an overgrowth free of constraint, which is in the order of b . As in Matthews' model [2], we neglect the interaction between the two arrays of dislocations. The cut-off limit, R^0 , is a subject of ambiguity, and can be taken as either R or T . We again leave it as a free parameter, because it simply represents the energy strength of a misfit dislocation. Since the area of $4RWN$ in the interface is the domain of misfit dislocations, the total elastic strain energy in the remaining part of the overgrowth may be given by:

$$E_{\epsilon} = 2\alpha(W-2RN)WHe^2 \quad (4)$$

where $\alpha = 2\mu(1+\nu)/(1-\nu)$. Note that in the existing continuum models [2,3], the effective thickness for the elastic strain energy is taken to be T . Combining both energy terms, we obtain the total energy:

$$\Omega = 2\gamma N W b^2 + 2\alpha(W-2RN)WHe^2 \quad (5)$$

Eq. (5) is subject to the condition that the sum of the dislocation-related strain and the pure elastic strain is equal to the original misfit strain, f :

$$f = (1 - 2RN/W)e + Nb/W \quad (6)$$

For Eq. (6), we have assumed that the amount of strain accommodated through the introduction of one misfit dislocation is equal to $b/2R$.

The overgrowth will accommodate an optimum number of misfit dislocations, $2N^*$, and optimum pure elastic strain, e^* , to minimize the total energy. If N^* is equal to zero, the situation is a coherent case, and if e^* is zero, the situation is equivalent to a complete relaxation of coherency strain and total plastic accommodation of the lattice misfit. Using the method of undetermined Lagrange multiplier, the solutions are found:

$$e^* = (b/2R)\{1 - (1 - 2\gamma R/\alpha H)^{1/2}\} \quad (7)$$

$$N^* = W(f - e^*)/(b - 2Re^*) \quad (8)$$

Eqs. (7) and (8) allow the analytical description of the following three physical situations:

Case A: When $H < 2\gamma R/\alpha$, no real solutions exist. This is a situation in which the dislocation energy density is so high that any introduction of dislocation is energetically unfavorable, and thus it is a coherent case without misfit dislocations. The overgrowth is entirely in ϵ domain. Thus, $e^* = f$ and $N^* = 0$.

Case B: When $H \geq 2\gamma R/\alpha$, the solutions are real and the overgrowth may have both δ domains and ϵ domains. When $f \leq e^*$, the misfit strain will be accommodated by a pure elastic strain with its magnitude of strain equal to f . When $f > e^*$, the misfit strain will be accommodated partially by the pure elastic strain with magnitude equal to e^* and partially by misfit dislocations. As the value of f increases, the number of misfit dislocations is increasing, but in the ϵ domain, the elastic strain does not change. An analytical expression for the critical value of H , above which misfit dislocations are introduced into the system is given by rearranging

Eq. (7) with $e^* = f$:

$$H_c = \frac{\gamma b}{2(1 - fR/b)\alpha f} \quad (9)$$

Case C: When $N^* = W/2R$, $R = R_{\max} = b/2f$ and $e^* = 0$. All the misfit strain is completely accommodated by misfit dislocations and their spacing is equal to $2R$. This is the other limiting case in which the overgrowth is in δ domain.

A numerical example is given in Fig. 4, for which $v = 1/3$, $R^0 = 300b$, $W = 1000b$, $R = 4b$, $\alpha = 4\mu$, $\gamma = 3.2\mu$ and $H_c = 2\gamma R/\alpha = 6.4b$. All the strains are normalized with a maximum possible misfit strain $f_{\max} = b/2R$, whereas the energy is normalized with a maximum possible elastic strain energy, $E_{\max} = \alpha W H_c^2$. Fig. 4 shows a Case B for which $H = 7b > H_c$. In this case, the lattice mismatch is accommodated with a coherent strain as long as the misfit value is less than $0.71f_{\max}$, but when $f > 0.71f_{\max}$, it is relieved through both δ and ϵ domains. Note that the volume fraction of δ domain, ω ($= 2RN^*/W$), is zero when $f < 0.71f_{\max}$, and the elastic strain, e^* , is a constant in the coexisting region of δ and ϵ domains ($f_{\max} > f > 0.71f_{\max}$).

There is a clear analogy between the present procedure and the chemical thermodynamics of a binary, two-phase system [11] where the volumes of the two domain types are equivalent to the volumes of two "phases." Just as in chemical thermodynamics, geometrical constructions analogous to phase diagram and free energy/composition curves may be formulated to aid in the visualization of the concepts of "phase" stability and metastability. In this "phase diagram," the horizontal axis corresponds to a normalized misfit, $x = f/f_{\max}$, (analogous to composition) while the vertical axis corresponds to the energy term (analogous to free energy). Then a common tangent construction yields the critical misfit value, x_c , at the $\epsilon/\epsilon+\delta$ transition, for which it is

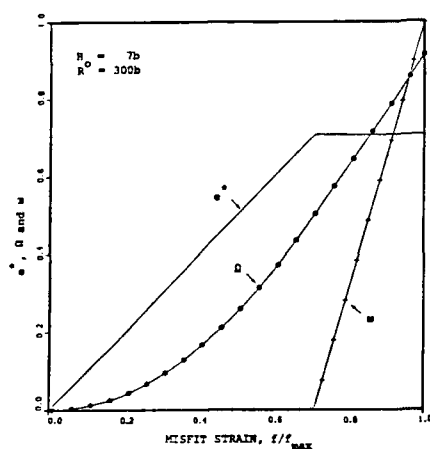


Fig. 4 Case B showing a transition from ϵ phase to a $\epsilon+\delta$ two-phase region.

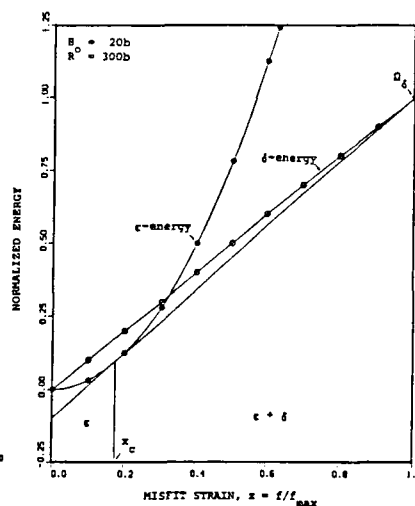


Fig. 5 Energy vs. misfit strain diagram showing a graphical solution of Eq. (7).

energetically favorable to nucleate misfit dislocations. Fig. 5 illustrates such an energy vs. misfit diagram for which parameters similar to those of Fig. 4 are employed. This construction provides a geometrical solution equivalent to Eq. (7) ($x_c = e^*/f_{\max}$). We note that x_c is also the value of the coherent strain in the ϵ domains which are in "equilibrium" with the δ domains. The form of the stable energy curve is given by the parabolic ϵ energy curve up to x_c and then assumes the linear form given by the common tangent construction.

Metastability in both the ϵ and δ "phases" can be also studied. When nucleation of misfit dislocations is difficult, the ϵ phase may accommodate more f than is predicted by equilibrium considerations; experimental result suggesting this has been reported [12,13]. In this case, the ϵ phase is metastable. A decrease in the energy of the system which occurs upon formation of δ domain is given by the vertical drop from the ϵ curve to the common tangent ($\Delta\Omega_1$ in Fig. 6). However, because the first δ phase nuclei to appear may not significantly change the misfit accommodated by the ϵ domains, a much greater driving force than $\Delta\Omega_1$ could be necessary for the initial nucleation of the misfit dislocations. The maximum possible driving force for nucleation is depicted as $\Delta\Omega_2$. Metastability in the δ domains may be also considered. This can arise when the most efficient dislocations (e.g., having Burgers vector in the interface plane) are not produced due to kinetic barriers. This effectively raises the value of the δ energy, and such a situation is depicted with a δ' energy curve in Fig. 6. Similarly, it is also conceivable to have an ϵ energy curve different from that of isotropic elasticity. This situation can arise due to anisotropic elasticity and/or difference in elastic properties between overgrowth and substrate, either of which is not considered in this analysis. Consideration of these factors will certainly shift the common tangent contact in either way, depending on the variation in the ϵ curve.

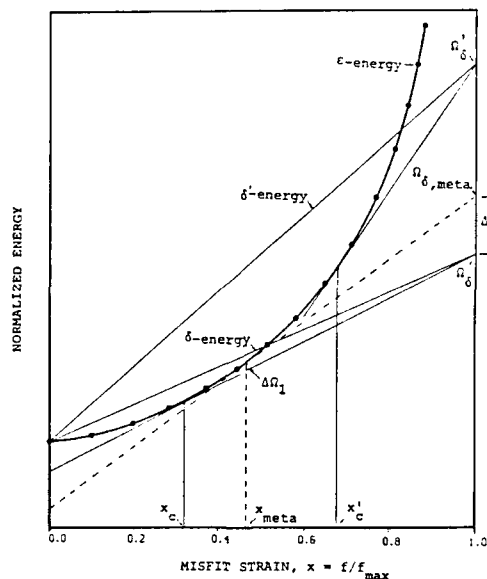


Fig. 6 Energy vs. misfit diagram illustrating various metastable states.

DISCUSSION

The continuum approach to the consideration of coherency loss in an overgrowth on a bulk substrate is analyzed so that the entire range of the interface behavior (coherent, coherency loss, plastic accommodation) can be represented on a simple energy diagram. The lattice mismatch is considered to be accommodated by two domains: a pure coherency domain and a domain of misfit dislocations. A justification for this partitioning can be made by equating the extent of the strain field of a misfit dislocation to $b/2\pi f$, but it is noted that the partitioning is not intended to reflect the actual microscopic distribution of the misfit strain; it is rather a tool which allows an energy diagram representation familiar to investigators in the materials field. When the thickness of an overgrowth is very small, the effective depth of the coherency strain domain can be taken as the thickness of the overgrowth. If the aspect ratio of an overgrowth is finite, however, understanding the relationship between H (hence H_c) and the actual overgrowth thickness, T , requires a further, detailed study on the shape and size dependency of the coherency strain energy for an overgrowth [14].

ACKNOWLEDGMENTS

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**RHEED OBSERVATION OF LATTICE RELAXATION
DURING Ge/Si(001) HETEROEPITAXY**

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ABSTRACT

We report the dynamic RHEED (reflection high energy electron diffraction) observation during Ge/Si(001) heteroepitaxy at various growth temperatures. The RHEED intensity analysis and the in-plane lattice constant analysis reveal a growth fashion and lattice relaxation. Both of them depend strongly on growth temperature.

INTRODUCTION

Ge/Si(001) has widely been attracting much attention not only as the most simple model system of mismatched heteroepitaxy but also for its wide variety of application. One of the most interesting application is Ge_m/Si_n strained-layer superlattices, which is theoretically expected to have a direct band gap [1]. To improve its crystalline quality, the understanding of an initial stage of the Ge/Si(001) heteroepitaxy is inevitable.

In this paper, we investigate intensity variation of RHEED spots during Ge/Si(001) heteroepitaxy and reveal the growth fashion. From measurement of diffraction spots spacing, we can determine the mean in-plane lattice constant during the growth, which gives the information about lattice relaxation. On the basis of these results, we discuss growth mode and the lattice relaxation during the growth of Ge/Si(001) over a wide range of growth temperature.

EXPERIMENTAL

Experiments were made in an ion-pumped MBE system. Si and Ge beams were evaporated from high-purity single-crystalline sources by a 2 kW electron gun and a PBN Knudsen cell, respectively. Typical growth rate was about 0.05 ML/sec. Si substrates were well-oriented (001) ($<0.08^\circ$). The substrates were prepared to form the Si(001) 2x1-single-domain structure [2].

The RHEED acceleration voltage was 40 kV. The incidence

angles were 4 mrad for the RHEED intensity analyses and 15 mrad for measuring the in-plane lattice constant. Details of the RHEED intensity monitoring system has been published elsewhere [3]. The in-plane lattice constant was determined by measuring the spacing of RHEED spots. RHEED patterns during the growth were recorded by a VTR and analyzed by an image processor with 256x256 pixels.

RESULTS AND DISCUSSION

Fig. 1 shows the intensity variations of RHEED specular beam spot ((00) spot) in the [010] azimuth during Ge/Si(001) heteroepitaxy. The growth temperature was varied from room temperature to 600 °C. One period of the RHEED intensity oscillation observed in this azimuth corresponds to a monoatomic-layer growth as well as in the case of Si homoepitaxy [4]. As shown in fig. 1, at the growth temperature above 350 °C, 5 or 6 periods of oscillation were observed clearly. A two-dimensional (2-D) streak RHEED pattern was observed during this

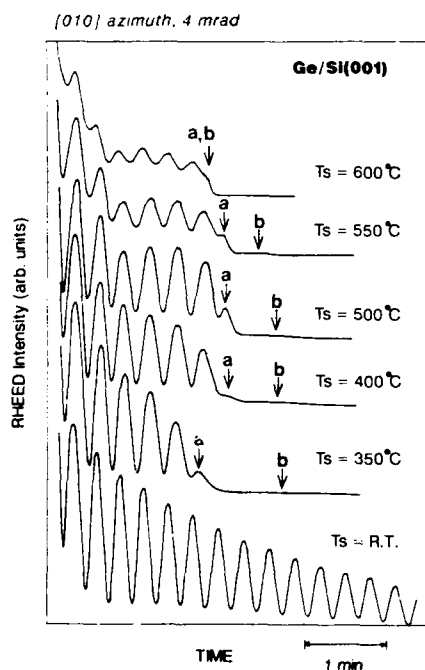


Fig. 1
Growth temperature dependence of RHEED specular intensity variation during Ge/Si(001) heteroepitaxy. Above 350 °C, clear oscillation was observed up to 5 or 6 periods, and after that, the pattern started to change from 2-D to 3-D at the point a and perfect 3-D pattern was observed at the point b.

period. At the point of peak a, the pattern started to change from 2-D to 3-D (three-dimensional). And then at the point b, where a small shoulder was observed, it became perfect 3-D pattern. The positions of these peaks varied with the growth temperature. Therefore, we conducted the following experiments focusing on these peaks.

Fig. 2 shows a typical intensity variation of RHEED specular spot and RHEED patterns observed during the Ge/Si(001) heteroepitaxy at 400 °C. Before the growth, a clear specular spot was observed accompanying the other bright part caused by a crossing of Kikuchi lines and 2-D reciprocal rods. When the Ge shutter opened, we observed 6 periods of intensive oscillation. At the maxima of the oscillation, the similar type RHEED patterns were observed as observed before the growth. On the other hand, at the minima of the oscillation, streaky patterns were observed. This alternate pattern change indicates that the growth mode of the Ge/Si(001) is 2-D layer-by-layer fashion up to 6 monoatomic-layers.

At the point a, the intensity of RHEED specular spot was much smaller than previous peaks and the RHEED pattern started to change to 3-D one. We checked the intensity profile along the 2-D reciprocal rods. It was found that the specular spot was

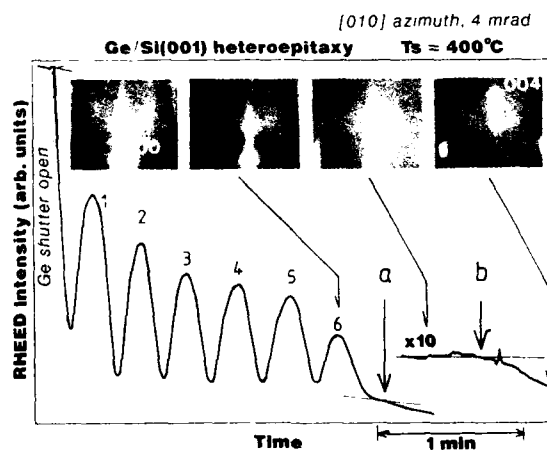


Fig. 2 Intensity variation of RHEED specular spot and RHEED patterns observed in the azimuth of [010] during Ge/Si(001) heteroepitaxy at 400°C.

still observed even after the transmission pattern appeared, and then the specular spots shifted toward the Bragg spot (004) of transmission pattern. This shift was observed as a change in intensity, such as peak a, through our fixed optical pickup. The RHEED pattern indicates that certain amount of small 3-D nucleated islands appeared on mostly flat surface.

The intensity of specular spot monotonously decreased until the point b where a perfect transmission pattern was observed. The intensity of diffused background became weak, which caused shoulder of intensity at the point b.

Fig. 3 shows the mean in-plane lattice constant during the growth at 400 °C which was measured from the RHEED spots spacing between ($\bar{1}0$) and (10) spots in the azimuth of [110]. Vertical-axis represents relative in-plane lattice constant of Ge heterolayer to bulk Si as follows;

$$\Delta = (a_{\text{surf}} - a_{\text{Si}}) / a_{\text{Si}} \quad (1)$$

Up to 6 monoatomic-layers growth, pseudomorphic growth of Ge was observed. This layer thickness well corresponds to the period while 2-D layer-by-layer growth was observed as mentioned previously. The peak a, where the surface morphology started to change to 3-D, also corresponds to the initiation of lattice

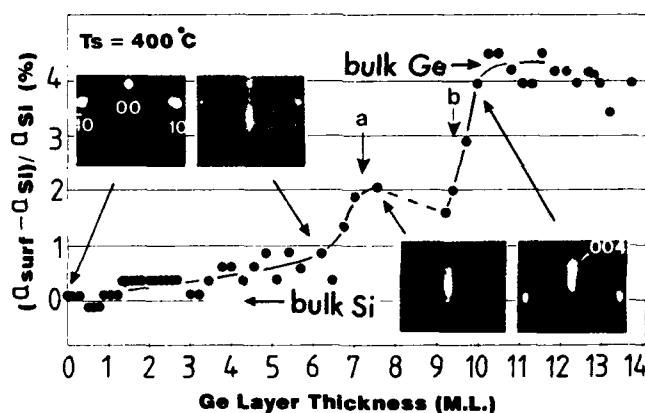


Fig. 3 Mean in-plane lattice constant variation measured from the RHEED spots spacing between ($\bar{1}0$) and (10) in the azimuth of [110] during Ge/Si(001) heteroepitaxy at 400°C.

relaxation. Over the point b, where the perfect 3-D RHEED pattern was observed, the in-plane lattice constant of Ge layer rapidly turned to the lattice constant of bulk Ge within one monoatomic-layer growth. It is conceivable that misfit dislocation is mostly induced around the point b. Lattice constant minimum was observed between points a and b. Similar behavior was reported in case of strained-layer growth of InAs/GaAs(001) [5], however clear explanation has not been done. These anomaly may essentially related to the fashion of strain relaxation. Further investigation is remained to be done. It is an interesting finding that the surface morphology and the lattice relaxation is closely related. Another interesting point is that several layers of deposition is necessary after the end of the pseudomorphic growth for the completion of lattice relaxation. Bevk et al. reported using RBS that Ge layers were pseudomorphic if the thickness was less than 6 monoatomic-layers and were relaxed if they were thicker than 10 monoatomic-layers [6]. Our result is in good agreement with their result.

Fig. 1 shows that as increase the growth temperature, the point b shifts to smaller thickness and approaches to the peak a. For instance, at 400 °C the point b was observed at 9.4 monoatomic-layers, while at 600 °C, it was observed at 6.6 monoatomic-layers and points a and b can not be discriminated, that is, the Ge layer was relaxed as soon as the pseudomorphic growth terminated. These results indicate that the process of misfit dislocation induction depend strongly on a growth temperature.

Persisting oscillations were observed below 300 °C. As shown in fig. 1, more than 35 periods of oscillation were clearly observed at room temperature. By the in-plane lattice constant determination, lattice relaxation was found to take place slowly. However in the low growth temperature case, the quality of Ge heterolayer was poor because as Ge growth proceeded, the RHEED pattern became to diffuse pattern. Growth mechanism of such a persisting oscillation is very interesting and further experiments should be needed.

CONCLUSION

We reported the dynamic RHEED observation during

Ge/Si(001) strained-layer heteroepitaxy over a wide range of growth temperatures. Above 350 °C, pseudomorphic growth was observed up to 5 or 6 monolayers, and after that, growth mode changed from 2-D to 3-D accompanying a lattice relaxation. Growth fashion and lattice relaxation strongly related with each other and both are affected by the growth temperature.

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EFFECT OF STRAIN AND INTERFACE INTERDIFFUSION ON THE VALENCE BAND OFFSET AT SI/GE INTERFACES

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ABSTRACT

The valence band offset for the Si/Ge interface is studied using the local density functional approach with a superlattice geometry. The effect of non-abrupt interfaces is modeled by including an interface layer of $\text{Si}_{0.5}\text{Ge}_{0.5}$ ordered in a $\sqrt{2} \times \sqrt{2}$ interface unit cell. The change in valence band offset is less than 0.01 eV. For an abrupt interface, the offset is found to be a function of strain in the Ge. The interface dipole is proportional to the perpendicular strain parameter which yields an interface contribution to the energy of the strained epitaxial Ge layers. The equilibrium strain parameter in epitaxial Ge differs from that in biaxially compressed bulk Ge.

1. INTRODUCTION

The prediction of valence band offsets at semiconductor heterojunctions remains a theoretical challenge [1]. The approaches to this problem break roughly into two groups: (i) alignment of bulk derived energy levels when the semiconductors are placed in contact [2]; (ii) calculation of the self-consistent interface dipole combined with the microscopic band structure calculation of the constituent materials [3]. A linear response approach based on microscopic treatment of a suitable reference system has also been proposed [4]. The possibility of interdiffusion or other types of defects at the interface further complicates the analysis. In simple terms, it allows for an interface dependent contribution to the band offset through possible modification of the interface dipole. This problem may certainly be approached on a microscopic basis within computational limits. Deeper problems are posed for the more general theories using alignment of bulk levels which are based on the premise that, to a first approximation, the details of the interface are screened out. In this regard, polar/non-polar interfaces e.g. GaAs/Ge (001) pose special problems. As is well known [5], structural models *without* some interdiffusion engender large dipoles. One may adopt a somewhat broadened view of "screening" to include atomic displacements which minimize the interface total energy. Then the alignment of the bulk derived levels might yield the valence band offset for the "optimal" interface. This is an open problem for which concrete calculations and further general theory are appropriate.

The presence of strain in either or both of the constituent materials due to lattice mismatch taken up elastically in pseudomorphic growth provides a further complication. This was certainly not taken into account in the original bulk alignment approach [2] but has been subsequently discussed [6]. Several issues arise. The strain (generally non-hydrostatic) splits the degeneracy of the valence band edge complex in semiconductors and shifts the energy levels [3]. The presence of the heterojunction may alter the strain configuration of the strained materials from the predictions based on bulk elastic constants. Finally, there may be non-uniform atomic relaxations in the region around the interface. These problems are well suited to microscopic treatment using the local density functional approach for evaluating

the total energy to optimize the structural degrees of freedom introduced by strain.

In the present work, both the problem of interface "defects" and the complications of strain are addressed for Si/Ge(001) interfaces. It is found that interdiffusion at the interface leads to a negligible change in the valence band offset. However, proper treatment of the strain yields some interesting differences with previous calculations. The epitaxial Ge is found to have a different perpendicular lattice constant than would be expected for strained bulk Ge due to the contribution of the interface energy. This in turn reduces the valence band offset at this interface by about 20 meV for 4 ML of Ge on Si.

2. INTERFACE INTERDIFFUSION

The local density functional approach used here is similar to that described in Ref. 3. Details of the pseudopotential, total energy calculations are reviewed in Ref. 7. Short period superlattices of the constituent materials are used containing two interfaces per unit cell. The (001) interface between cubic Si and tetragonally strained Ge grown pseudomorphically on Si is considered. In this section, the experimental lattice constant of Si is used together with bulk elastic constants to obtain the Ge layer spacing. The interface spacing is taken as an average. For ideal interfaces, the superlattices have either simple tetragonal (e.g. Si_4Ge_4 alternating 4 ML Si with 4 ML Ge) or body centered tetragonal (Si_6Ge_4) unit cells. In the selfconsistent superlattice calculations, a plane wave basis was used with basis functions of kinetic energy up to 7, 10 or 12 Ry included. The interface dipole potential is well converged. The "interdiffused" interface is formed by doubling the interface unit cell area with a $\sqrt{2} \times \sqrt{2}$ orientation. The cell consists of 4 ML Si, 4 ML Ge and two interface layers with 1 Si and 1 Ge atom per interface cell. This is a total of 10 Si and 10 Ge atoms per cell (nominally Si_5Ge_5). The interface layer was assumed to be planar. The distance from the Si layer was taken to be the average of the Si-Si spacing and that of a $Si_{0.5}Ge_{0.5}$ alloy lattice, suitably strained. Similarly, the distance from the Ge layer was also determined as an average. Calculations of the forces on the atoms suggest that this is a reasonable initial choice. Calculations were done with a plane wave kinetic energy cutoff of 7 Ry.

The superlattice gives an accurate representation of the interface properties to the extent that the charge density at the center of each material is bulk like. A simple measure of this is to compare the integrated electronic charge density between each of the atomic planes to the nominal bulk result (4 electrons per interface unit cell atom). This has been done for a sequence of superlattices with the results for Δn shown in Fig. 1a. These results confirm the conclusions of Ref. 3: the self consistent response to the perturbation of the interface is localized essentially within the adjoining layers. Increasing the volume of the constituents further has a negligible effect. The selfconsistent interface dipole is also evident in Fig. 1a resulting from a small charge transfer from Si to Ge. Treating the Δn observed in Fig. 1a as sheet charges separated by $2d_{001}$ gives an excellent estimate of the dipole discontinuity across the interface.

The results of the self consistent $\sqrt{2} \times \sqrt{2}$ interface are illustrated in the same way in Fig. 1b. The net charge transfer is approximately the same but leads to half the charge separated by d_{001} and the other half by $3d_{001}$. Thus, despite the "rough" interface, the net dipole is approximately the same. This is found to be the case when precise calculations of the dipole are carried out. The change in the band offset introduced by the interface interdiffusion is less than 0.01 eV. This is in agreement

with more general results of the linear response approach for non-polar interfaces [4].

The atomic relaxations from the ideal geometry assumed for the $\sqrt{2} \times \sqrt{2}$ interface clearly influence this result. The interface layer exhibits a tendency to buckle. However, these changes are coupled to in-plane distortions of neighboring Si and Ge layers. The resulting atomic relaxations propagate all the way to the center of the Si and Ge regions. This eliminates any reference bulk like region from the superlattice. Thus it is not possible to isolate the interface effect as required to obtain a band offset. This aspect of the problem remains open.

3. STRAIN DEPENDENCE

Considering the case of an ideal, abrupt interface, the interplanar separations may still all relax. Consider one structural degree of freedom:

$$a_{Ge\perp} = (1 + \epsilon_{\perp})a_{Si\parallel}. \quad (1)$$

This fixes the d_{Ge-Ge} . The d_{Si-Si} is taken from cubic Si and d_{Si-Ge} is taken as an average. In Ref. 3, ϵ_{\perp} was derived from macroscopic bulk elastic constants. Here, it is allowed to vary; the value is found through total energy minimization. The calculations were performed with a plane wave kinetic energy cutoff of 14 Ry using the Si_6Ge_4 superlattice. The Si lattice constant was taken to be that which minimizes the energy in the bulk diamond structure (5.40 Å for the present

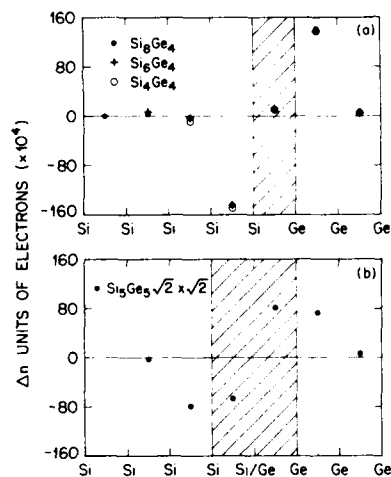


Figure 1. Deviation from bulk electronic charge (Δn) on a layer by layer basis (a) for a series of cases with differing number of Si layers and (b) for the case with an interface layer containing equal numbers of Si and Ge atoms ordered in a $\sqrt{2} \times \sqrt{2}$ interface unit cell. An ideal structure is used in each case. The interface region is indicated.

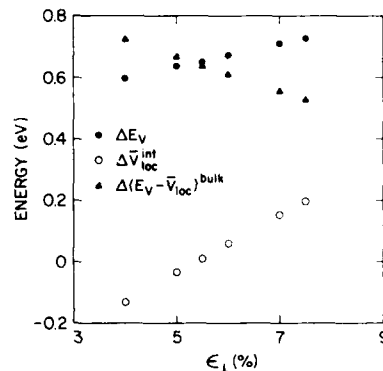


Figure 2. The calculated valence band offset (ΔE_V) as a function of the perpendicular strain parameter in the Ge region (ϵ_{\perp} in percent). The individual terms from Eq. (2) illustrate the competing effects of the strain on the band offset.

pseudopotential as compared to 5.43 Å experimentally). The bulk valence band edge position relative to the average local potential is obtained with a fully converged bulk calculation (17 Ry cutoff) including strain as appropriate.

The calculated valence band offset ΔE_v is shown in Fig. 2 as a function of ϵ_1 . It is determined by the change in the average local potential across the interface together with the position of the respective bulk valence band edges relative to the average potential [3]:

$$\Delta E_v = \Delta \bar{V}_{loc}^{int} + \Delta(E_v - \bar{V}_{loc})^{bulk}. \quad (2)$$

The bar denotes average over a slab between atomic planes. The E_v is the energy of the valence band edge state taken to include all effects of strain (uniaxial as well as hydrostatic), but does not include the spin-orbit splitting. This may also be included [3]. The two terms of Eq. (2) are plotted separately in Fig. 2. The potential step at the interface shows significant dependence on the strain parameter ϵ_1 . This is partially compensated by the strain dependence of the Ge valence band edge position yielding a smaller net dependence of the valence band offset on strain.

The total energy (per Ge_2 unit) of the Si_6Ge_4 superlattice and bulk Ge are plotted in Fig. 3 as a function of ϵ_1 . The position of the energy zero is arbitrary. The solid (dashed) line represents a polynomial fit to the calculated solid (open) points. The comparison must be made between the theoretical result for bulk Ge and the epitaxial Ge. Although the theoretical lattice constants of bulk Si and Ge have an accuracy of about 1% in comparison to experiment [7], this still leaves a large error in the theoretical *lattice mismatch*. In the present calculation, the calculated lattice mismatch is about 3.1% as compared to 4.2% in experiment. The fluctuations

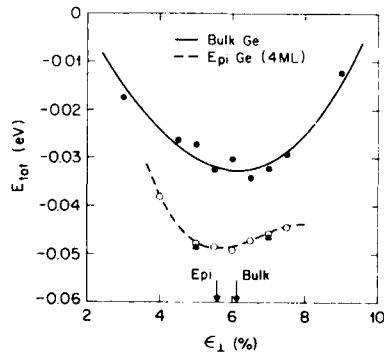


Figure 3. The total energy as a function of perpendicular strain parameter in the Ge region (ϵ_1 in percent) for bulk Ge and for the case of 4 ML of epi Ge. In the latter case, the open circles give the unrelaxed total energies while the closed triangle indicate the result of complete structural relaxation (with fixed ϵ_1). The absolute positions of the curves are arbitrary.

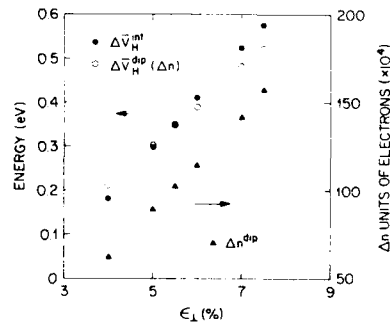


Figure 4. The dipole contribution to the valence band offset ($\Delta \bar{V}_H^{int}$) as a function of perpendicular strain parameter in the Ge region (ϵ_1 in percent). An estimate of the number of electrons forming the dipole based on the simple model in Fig. 1 (Δn^{dip}) together with the corresponding value of the dipole ($\Delta \bar{V}_H^{dip}$).

in the points represent basis set incompleteness, an effect which is larger for the bulk Ge case. The positions of the minima in the curves are well determined and show a clear difference between the bulk and epitaxial cases. These results are consistent with structural optimization of Si_nGe_n superlattice geometries using a valence force field approach where the c -axis lattice constant was also smaller than predicted by macroscopic elastic coefficients [8]. One may be concerned that the present result depends on allowing only the ϵ_1 degree of freedom. However, for two selected values of ϵ_1 , full relaxations of the interlayer spacings have been done using the calculated forces to guide the minimization. The results are indicated by the solid triangles in Fig. 3. It is clear that such relaxations make a small difference near the minimum which will not significantly affect the value of ϵ_1 which minimizes the total energy.

The total energy calculations show that the perpendicular lattice constant for epitaxial Ge is different than would be the case for bulk Ge with the same biaxial compression. This result has a simple physical basis. The interface dipole is found to be proportional to the strain parameter near equilibrium, as illustrated in Fig. 4. The simple model for the dipole from Fig. 1 yields the average charge transfer Δn for each ϵ_1 . This shows that $\Delta n \propto \epsilon_1$. The interface dipole potential step $\Delta \bar{V}_H^{dip}$ calculated from Δn is plotted in Fig. 4 in comparison to the dipole derived from the precise calculation $\Delta \bar{V}_H^{int}$. The agreement is quite good showing that the simple model for the interface dipole is rather accurate. This then implies that there is an interface contribution to the total energy in the epitaxial Ge arising from the formation of the dipole which will scale as ϵ_1^2 . This extra interface energy augments the standard elastic expression for the strain energy:

$$E_{tot} = 4C_{12}\epsilon_{xx}\epsilon_{zz} + C_{11}\epsilon_{zz}^2 + E_{dip} \quad (3)$$

where the elastic constants are taken in units of energy per Ge_2 , i.e. four Ge atoms per epitaxial unit cell. The ϵ_{xx} , ϵ_{zz} are the standard strain parameters. The E_{dip} includes two interfaces per unit cell. One has $\epsilon_{zz} = \epsilon_{xx} + \epsilon_1 + \epsilon_{xx}\epsilon_1$. From the data for Δn in Fig. 4 one can estimate that $E_{dip} = -0.007\epsilon_1 + 0.19\epsilon_1^2 \text{ Ry}$. Using the bulk Ge elastic constants $C_{12} = 1.02 \text{ Ry}$ and $C_{11} = 2.72 \text{ Ry}$, and the experimental lattice mismatch, $\epsilon_{xx} = -0.04$, one finds that for 4 ML of epitaxial Ge

$$\begin{aligned} \epsilon_1 &= 0.073 && \text{bulk, no dipole,} \\ \epsilon_1 &= 0.069 && \text{with dipole,} \end{aligned} \quad (4)$$

giving a change of -0.004, quite consistent with the full total energy minimization illustrated in Fig. 3. This shows that the interface dipole plays an important role in the structural properties of ultrathin strained epitaxial layers.

The present results are supported by ion channeling measurements of epitaxial Ge layers on Si. The "effective" Poisson ratio which was used to fit the data is smaller than expected from bulk elastic constants [9]. However, the interface contribution identified above implies that the perpendicular lattice constant depends on the number of Ge layers. For instance, the change in ϵ_1 is -0.007 for 2 ML of Ge but only -0.003 for 6 ML of Ge. Intermixing at the interface could lead to nonuniformity in the strain through this mechanism. Such intermixing also complicates the analysis of the ion channeling data [9]. Referring back to Fig. 2, the change in ϵ_1 of -0.004 implies a reduction of the valence band offset by about 20 meV. This is a relatively small change. However, the sign of the change is consistent with recent measurements [10] which gave a valence band offset smaller than that calculated in Ref. 3. The coupling observed here between interface electronic properties and structural properties of the epitaxial layer suggest that further precise measurements of the lattice constants of strained epitaxial layers would be quite

interesting. In the present case, the changes in Ge layer spacing are relatively small (less than .01 Å). The changes due to non-uniform relaxation of the layers are only two to three times smaller.

The dipole and the strain also couple to that non-uniform relaxation of the planar positions near the interface. This is, however, a "long-range" effect in the sense that such relaxations are not zero at the center of the Si and Ge regions. It would be interesting to see if these atomic displacements which further screen the dipole might also alter the valence band offset in a significant way. In the Si/Ge system, larger strained layers (Ge here) are not too physical in view of the small critical layer thickness for misfit dislocation formation. However, this may be a generic feature of strained systems.

4. CONCLUSION

It has been shown that a concrete model for interface interdiffusion has a negligible influence on the band offset at the Si/Ge strained layer interface. However, the valence band offset has a non-trivial strain dependence. This couples to a reduction in the perpendicular Ge lattice constant due to the interface dipole contribution to the energy. Although the resulting correction to the valence band offset is relatively small, it does imply a coupling between the structural and electronic degrees of freedom which may be quite interesting. The role of further inter-layer relaxation around the abrupt interface or atomic relaxation near the interdiffused interface remains an open question.

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DEFECTS AND STRAIN IN $\text{Ge}_x\text{Si}_{1-x}$ LAYERS GROWN BY RAPID THERMAL PROCESSING CHEMICAL VAPOR DEPOSITION

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ABSTRACT

We have grown single and multi-layer epitaxial $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structures by RTPCVD on (100)Si substrates using GeH_4 and SiH_2Cl_2 at 900°C and 1000°C with $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratios of 14:1 to 95:1 at 5 Torr. Plane view TEM micrographs indicate misfit dislocation free layers were grown for Ge concentrations of up to 13%. Misfit dislocation networks aligned along $\langle 110 \rangle$ were formed at the interface of films with higher Ge concentrations. Plane view TEM micrographs also showed dislocation loops at the interface. When the $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratio used was less than 25:1, the $\text{Ge}_x\text{Si}_{1-x}$ layer grew by three-dimensional nucleation, resulting in a high density of defects.

INTRODUCTION

Strained $\text{Ge}_x\text{Si}_{1-x}$ alloy layers have received considerable attention due to the ability to tailor the energy band gap by varying the Ge fraction and the band alignment by controlling the state of strain in the underlying layer. In addition, strained $\text{Ge}_x\text{Si}_{1-x}$ layers have also been observed to exhibit an enhanced reduction in the fundamental (indirect) band gap, relative to unstrained $\text{Ge}_x\text{Si}_{1-x}$ layers. The ability to tailor the energy band with strained $\text{Ge}_x\text{Si}_{1-x}$ layers has permitted the realization of many novel device structures in Si technology previously restricted to GaAs technology such as modulation-doped field-effect transistors (MODFETs) [1] and heterojunction bipolar transistors (HBTs) [2]. A superlattice structure consisting of multiple alternating $\text{Ge}_x\text{Si}_{1-x}$ and Si layers can be utilized for quantum well devices and for waveguides. $\text{Ge}_x\text{Si}_{1-x}$ waveguide photodetectors operating in the near infrared spectral range ($\sim 1.3 \mu\text{m}$) have already been fabricated [3]. Relaxed $\text{Ge}_x\text{Si}_{1-x}$ layers may be utilized as buffer layers for fabrication of GaAs/Si structures. By using relaxed $\text{Ge}_x\text{Si}_{1-x}$ buffer layers on Si, epitaxial GaAs layers can be grown lattice matched on Si.

$\text{Ge}_x\text{Si}_{1-x}$ films grown on Si by molecular beam epitaxy (MBE) have been previously reported. We have grown $\text{Ge}_x\text{Si}_{1-x}$ films on Si(100) substrates by rapid thermal processing chemical vapor deposition (RTPCVD), using GeH_4 and SiH_2Cl_2 as source gases and H_2 as a carrier gas.

RTPCVD has received considerable attention because of its ability to reduce many of the processing problems associated with thermal exposure, such as out-diffusion, auto-doping, and memory effects. Large, quick, highly controllable temperature changes start/stop the thermally driven surface reactions of the deposition. Thus, RTPCVD offers the ability to grow precisely controlled, reproducible ultra thin layers while minimizing thermal exposure, as well as a commercially viable means of producing ultra thin epitaxial layers with very low defect densities. Through quick temperature cycling and short processing times, RTPCVD offers the capability of *in-situ* multiple processing by rapidly changing the ambient between cycles. Thus, RTPCVD facilitates *in-situ* cleaning and deposition of multiple layers of different materials or material compositions. Lee *et al.* [4] have already shown that RTPCVD is capable of growing high quality epitaxial Si layers. Hsieh *et al.* [5] have also successfully shown that RTPCVD is capable of growing *in-situ* doped polysilicon layers for use as diffusion sources for ultra-shallow junction formation.

EXPERIMENT

We grew $\text{Ge}_x\text{Si}_{1-x}$ films on p-type (100)Si substrates by RTPCVD, using GeH_4 (0.92% GeH_4 in H_2) and SiH_2Cl_2 as source gases and H_2 as a carrier gas. The design of our RTPCVD system is described elsewhere [6]. Boron-doped 5" (100)Si prime wafers with resistivities of 14-22 $\Omega\cdot\text{cm}$ were used for substrates. To clean the wafers, a diluted HF solution was prepared by using an electronic grade 49% HF solution, which was further diluted by deionized (DI) water so that the ratio of the DI water to the original 49% HF solution was 30:1. After dipping the wafer in the diluted HF solution for 60s, the wafer was thoroughly rinsed in flowing DI water and blown dry with N_2 from a liquid nitrogen source. Then the wafer was immediately loaded into our RTPCVD chamber, which was pumped down to a base pressure of less than 1 mTorr.

As a final clean before deposition, an *in-situ* hydrogen pre-bake was performed. The hydrogen pre-bake consisted of heating up the wafer to temperatures above 1000°C for 60s in H_2 . After the pre-bake, the wafer quickly cooled and the source gases GeH_4 and SiH_2Cl_2 were introduced into the ambient. Film deposition commenced once the wafer was quickly heated up to growth temperature. Films grown include single and multi-layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structures. Deposition temperatures used were 900°C and 1000°C at a pressure of 5 Torr with $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratios ranging from 14:1 to 95:1.

Film quality was characterized by transmission electron microscopy (TEM) [both plane view and cross-section TEM (XTEM)]. Plane view TEM was applied to characterize defects within the layers and at the interfaces. Plane view TEM samples were prepared by chemically thinning from the back side of the wafer with a $\text{HNO}_3:\text{HF}:\text{CH}_3\text{COOH}$ etching solution at a ratio of 6:3:1. After chemical thinning of the backside, the heterointerface of single layer structures could be observed by slowly ion milling the surface of the structure with Ar^+ . Similarly, each interface of the multi-layers structures could be observed by successively ion milling the surface of the structure until each interface was reached. At the thin edge of the TEM samples, it is always possible to observe a single interface without difficulty. XTEM was used to observe defects within the layers and measure the thickness of each layer. XTEM samples were prepared by stacking and glueing samples. After curing, slices were taken along a cross-section. Each slice was then thinned first by grinding and then by ion milling. The cross-section samples were also used to determine film composition by energy dispersive spectroscopy (EDS) utilizing a scanning TEM (STEM). Auger electron spectroscopy (AES) was also used to determine film composition. In addition, strain analysis was performed by x-ray diffraction.

RESULTS

Figure 1 shows the XTEM micrograph of a single 350 nm epitaxial $\text{Ge}_x\text{Si}_{1-x}$ layer grown at 1000°C for 60s with a $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratio of 39:1. An atomic Ge concentration of about 7% was determined by quantitative analysis with EDS utilizing a STEM. Electron diffraction patterns showed the $\text{Ge}_x\text{Si}_{1-x}$ layer to be single crystal. A plane view TEM micrograph of a $\langle 110 \rangle$ misfit dislocation network at the interface with an average dislocation line separation of 0.43 μm is shown in Figure 2. The wide variation in dislocation line spacing indicates the existence of a pinning mechanism. Both plane view TEM and XTEM show that the number of threading dislocations are very small, indicating that the velocity of propagating misfit dislocations was very high at the growth temperature of 1000°C. An interesting observation from Figure 2 is that many dislocation lines are not straight, as often treated in the theoretical calculation of strain energy. We observed the dislocation lines to often make sharp turns and run along orthogonal direction. Preliminary Burger's vector analysis has shown that the dislocations are neither pure screw nor pure edge dislocations, suggesting that the dislocation are 60° dislocations. Plane view TEM micrographs of areas close to the edge of the wafer, where the deposition temperature/rate is slightly lower due to the accelerated heat loss, show even better film quality. The average misfit dislocation separation is more than 1.1 μm .

Initial x-ray diffraction results indicate that despite the misfit dislocation network at the interface, the film is not completely relaxed. Figure 3 shows the spectrum relative to (400)Si. For a commensurate $\text{Ge}_{0.07}\text{Si}_{0.93}$ film, $\Delta\theta$ should be about 0.18°. For a totally relaxed $\text{Ge}_{0.07}\text{Si}_{0.93}$ film, $\Delta\theta$ should be about 0.12°. Our results show that $\Delta\theta$ is between these values, indicating that the film is only partially relaxed.

Multi-layer structures with varying Ge content for each $\text{Ge}_x\text{Si}_{1-x}$ layer were grown in order

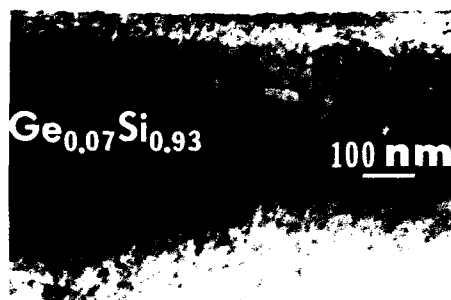


Figure 1: XTEM micrograph of single epitaxial $\text{Ge}_{0.07}\text{Si}_{0.93}$ layer.



Figure 2: Plane view TEM micrograph of $\langle 110 \rangle$ misfit dislocation network at interface.

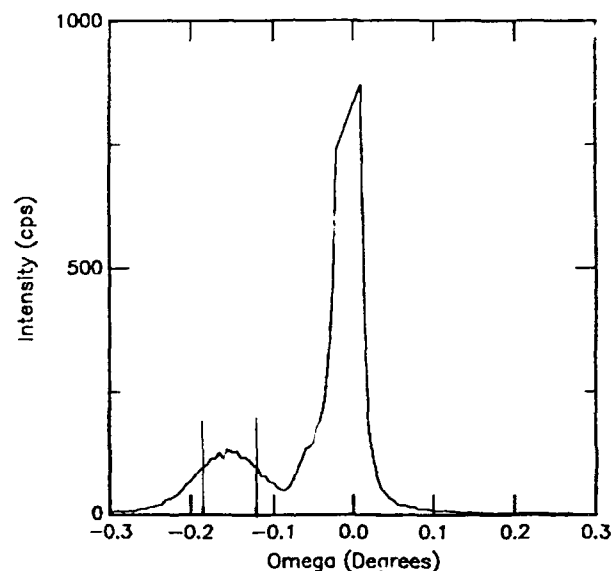


Figure 3: X-ray diffraction spectrum of single epitaxial $\text{Ge}_{0.07}\text{Si}_{0.93}$ layer, relative to (400)Si.

to facilitate process characterization. Figure 4 shows the XTEM micrograph of a five layer alternating $\text{Ge}_x\text{Si}_{1-x}$ and pure Si structure in which the $\text{Ge}_x\text{Si}_{1-x}$ layers appear as the darker layers. All five layers were grown at 900°C , but each $\text{Ge}_x\text{Si}_{1-x}$ layer was grown for 15s while each Si layer was grown for 20s. The $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratios used in growing the $\text{Ge}_x\text{Si}_{1-x}$ layers from top to bottom (first to last) were 20:1, 39:1, and 95:1, with corresponding thicknesses of 1000 Å, 900 Å, and 750 Å. Quantitative AES analysis indicates that the top layer has an atomic Ge composition of about 21% and the third layer has an atomic Ge composition of about 13%. The Ge concentration of the bottom $\text{Ge}_x\text{Si}_{1-x}$ layer was too small to be accurately quantified by AES.

The XTEM micrograph in Figure 4 show a high density of threading dislocations in the

higher Ge fraction top layer, while the other four layers appear to have little or no threading dislocations. Plane view TEM micrographs indicated that although the second interface (from the top) and the underlying interfaces show defects that were identified as dislocation loops, all the $\text{Ge}_x\text{Si}_{1-x}$ layers grew epitaxially without dislocations in each layer except the top layer.

Figure 5 shows a plane view TEM micrograph of the first $\text{Ge}_x\text{Si}_{1-x}$ layer and interface. A high density of threading dislocations in addition to defects at the interface can be seen. Electron diffraction patterns revealed that although the top layer has a high density of dislocations and small dislocation loops, the layer is completely epitaxial. Many dislocations are dissociated as evidenced by stacking fault fringes. Figure 5 also showed misfit dislocations lying along the $\langle 110 \rangle$ directions. The second interface was examined after ion milling off the top layer and interface. Plane view dark field TEM micrographs of the second interface reveal defects with dislocation loop-like contrast, but no misfit dislocations. TEM micrographs indicate that all of the other underlying interfaces exhibited very similar microstructures in terms of defect characteristics and densities. The plane view TEM micrographs indicate that no relaxation due to formation of misfit dislocations occurred in the lower four layers.

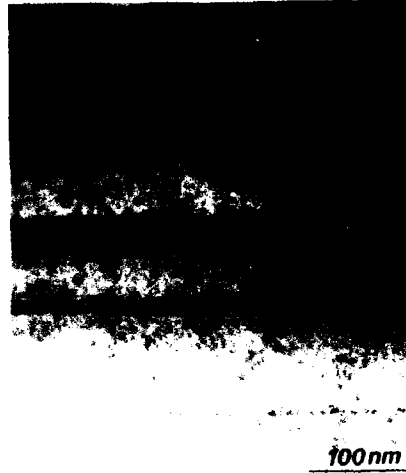


Figure 4: XTEM micrograph of five layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structure.



Figure 5: Plane view dark field TEM micrograph of top layer and top interface of the five layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structure.

We also grew the three layer alternating $\text{Ge}_x\text{Si}_{1-x}$ and pure Si structure shown in Figure 6. Each layer was grown at 900°C for 10s. The $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratios used in growing the $\text{Ge}_x\text{Si}_{1-x}$

layers from top to bottom were 25:1 and 63:1. Quantitative AES analysis indicates that the top layer has an atomic Ge composition of about 17% and the third layer has an atomic Ge composition of about 8%. Plane view TEM micrographs show similar structures as found for the five layer structure, but the first $\text{Ge}_x\text{Si}_{1-x}$ layer and interface have a higher density of misfit dislocations in addition to threading dislocations and a small number of dislocation loops as shown in Figure 7. Figure 8 is a plane view TEM micrograph of the third interface between the $\text{Ge}_x\text{Si}_{1-x}$ and the Si substrate, and shows only dislocation loops. The second interface was observed to be very similar to the third interface. The only defects observed at these two interfaces consisted of dislocation loops which were confined near the interfaces. Some of the dislocation loops were identified as hexagonal Frank loops with a Burger's vector of $\frac{a}{2}[111]$. The size of the dislocation loops varied from less than 100 Å to up to 2000 Å.

No misfit dislocation lines were observed in the second and third interfaces, indicating that no relaxation due to the formation of misfit dislocations occurred in the third layer.

As can be seen in Figures 5 and 7, $\text{SiH}_2\text{Cl}_2:\text{GeH}_4$ ratios less than 25:1 resulted in a high density of dislocations. These micrographs are similar to the $\text{Ge}_x\text{Si}_{1-x}$ layer shown in Figure 6 in a paper by Kasper *et al.* [7]. We believe that the high Ge concentration $\text{Ge}_x\text{Si}_{1-x}$ layers we deposited at 900°C grew by three-dimensional nucleation. Misfit dislocations emanating from the tangle of threading dislocations seen in Figures 5 and 7 seem to be formed by propagation of threading dislocations and demonstrate that threading dislocations can indeed be a source of misfit dislocations under certain conditions (as in our experiment where a high density of threading dislocations form during the growth process).



Figure 6: XTEM micrograph of three layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structure.

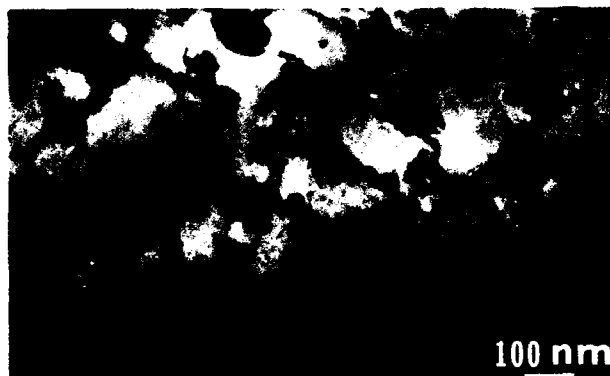


Figure 7: Plane view TEM micrograph of top layer and top interface of the three layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structure.



Figure 8: Plane view TEM micrograph of bottom interface of the three layer $\text{Ge}_x\text{Si}_{1-x}/\text{Si}$ structure.

CONCLUSIONS

We have successfully grown high quality epitaxial $\text{Ge}_x\text{Si}_{1-x}$ layers by RTPCVD for Ge concentrations of up to 13% at 900°C and 1000°C. Layers with Ge concentrations of up to 13% grown at 900°C layers showed no evidence of strain relaxation through the formation of misfit dislocations. Layers grown at 1000°C relaxed through the formation of misfit dislocations which were confined near the interface. Preliminary analysis by x-ray diffraction suggests that the film is only partially relaxed.

Multi-layer structures grown at 900°C were highly crystalline, except for the top layers which had higher Ge concentrations of greater than 17%. The top layers had high densities of threading dislocations, as well as misfit dislocations. The $\text{Ge}_x\text{Si}_{1-x}$ layers underneath, however, contained only dislocation loops and showed no evidence of relaxation through misfit dislocation formation.

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ELECTRON-BEAM-INDUCED-CURRENT (EBIC) IMAGING OF DEFECTS IN $\text{Si}_{1-x}\text{Ge}_x$ MULTILAYER STRUCTURES

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ABSTRACT

The electron-beam-induced-current (EBIC) technique has been used to image dislocations and other defects at strained $\text{Si}_{1-x}\text{Ge}_x$ epitaxial interfaces and in overlying epitaxial layers grown by Limited Reaction Processing. Depending upon the bias conditions and test structure, one can distinguish between interface defects and those in overlying films. We have found that for a low density of misfit dislocations, a high quality (defect-free) overlying epitaxial layer can be grown, but for a high density of dislocations certain line defects propagate upwards in the overlying layers.

INTRODUCTION

The commensurate $\text{Si}_{1-x}\text{Ge}_x$ strained layer system on silicon substrates has received considerable attention in the last few years as a possible material system for high quality heterojunction devices on silicon substrates. The larger natural lattice constant of the $\text{Si}_{1-x}\text{Ge}_x$ layers results in misfit dislocations at the interface if the strained layer is thicker than some "critical thickness." [1,2,3] Knowledge of the presence of dislocations is very important since the bandgap of the $\text{Si}_{1-x}\text{Ge}_x$ depends on the strain [4], and the dislocations can serve as minority carrier recombination sites. This critical thickness is strongly dependent on germanium fraction x , growth temperature, substrate preparation, and other experimental factors. Transmission electron microscopy (TEM) can be used to detect the presence of dislocations and has excellent resolution, but generally only samples an area of several square microns.

The electron-beam induced current technique monitors the minority carrier charge generated by a scanning electron beam that is collected by a nearby blocking contact (typically a Schottky barrier or a p-n junction.) When the carriers are generated close to a defect, a large number will recombine, and fewer will be collected by the contact. By displaying this collected charge as a function of position, one can thus map out an image of the defect structure [5,6].

The EBIC technique has been previously applied to single $\text{Si}_{1-x}\text{Ge}_x$ layers grown on silicon substrates to determine critical thickness for various germanium fractions [7]. Our work has focussed on a multilayer structure of Si substrate: $\text{Si}_{1-x}\text{Ge}_x$:Si as one would use for a narrow gap heterojunction bipolar transistor [8].

SAMPLE GROWTH AND PREPARATION

The samples were grown by a modified version of the Limited Reaction Processing technique [9]. The growth combines the

versatility of gas sources (chemical vapor deposition) with rapid control of the sample temperature (rapid thermal processing). The growth chamber itself consists of a 17-cm diameter quartz tube exhausted by a mechanical roughing pump. A single four-inch wafer is heated without a susceptor by a bank of microprocessor-controlled tungsten halogen lamps.

The samples grown for these experiments consisted of a single layer of $\text{Si}_{0.78}\text{Ge}_{0.22}$ sandwiched between a silicon (100) substrate and an epitaxial silicon cap of 1.3 μm thickness (fig. 1). Three different samples were grown, each having a different $\text{Si}_{0.78}\text{Ge}_{0.22}$ thickness. After sample loading and an initial high temperature bake in hydrogen for surface cleaning (1200 C, 30 s), silicon buffer layers were grown at 1000 C and then 900 C (0.4 μm each) at 6.0 torr using dichlorosilane as the source gas in a hydrogen carrier. The temperature was then changed to 625 C, and the $\text{Si}_{0.78}\text{Ge}_{0.22}$ layers were grown using a combination of dichlorosilane and germane as sources. Growth rates and the germanium fraction were measured by calibrated SIMS on samples grown under identical conditions as these just before and after these samples. The accuracy of the germanium fraction is thought to be ± 0.01 , and accuracy of the layer thickness $\pm 10\%$. The three samples were grown with a $\text{Si}_{0.78}\text{Ge}_{0.22}$ thickness of 0.17 μm , 0.34 μm , and 0.69 μm , respectively. The growth rate of this layer was approximately 10 nm/min. After these layers, a top cap of 1.3 μm of Si was grown at 800 C at a rate of 40 nm/min. None of the layers was intentionally doped, but this generally results in n-type layers in our reactor with doping levels on the order of $10^{16} - 10^{17} \text{ cm}^{-3}$.

EBIC structures were then formed by evaporating Pd dots of 40 nm thickness. This thickness was chosen to be transparent to high energy (30 KeV) electrons. Simple measurement showed that the Pd formed a Schottky barrier to the Si, and that the Si was n-type. Thus the Schottky barrier would collect minority carrier holes in an EBIC experiment. Capacitance measurements showed the Schottky barrier depletion width to be about 0.3 μm , much less than the top Si thickness of 1.3 μm . Attaching bond wires and mounting in a header completed the fabrication.

RESULTS

EBIC measurements were performed using an electron energy of 20 to 30 KeV and a current on the order of 100 nA. Images from the three samples of varying $\text{Si}_{0.78}\text{Ge}_{0.22}$ thickness are shown in figure 2. The sample with the $\text{Si}_{0.78}\text{Ge}_{0.22}$ thickness of 0.17 μm shows no defects. (The few marks on the sample were a result of processing.) The next thickest sample (0.34 μm) showed many extended defects running in $\langle 110 \rangle$ directions, with an average spacing of about 10 μm . Finally, the thickest sample (0.69 μm) showed a larger defect density, with an average spacing on the order of microns. The defect structures imaged by EBIC were in one-to-one agreement with surface features seen in the samples with phase contrast optical microscopy. A few volts reverse bias yielded no qualitative change in the images. At larger (>5 V) reverse bias, noise made imaging impractical. A micrograph of the 0.17 μm sample showed no surface features at all, even after a light defect etch. The thicker samples had an optically visible cross-hatched pattern (fig. 2d) which is commonly associated with misfit dislocations. The features were visible without any defect etching, and were measured with a stylus

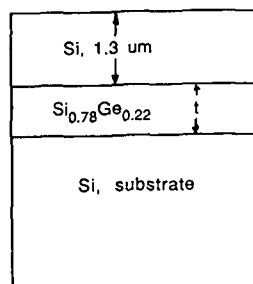
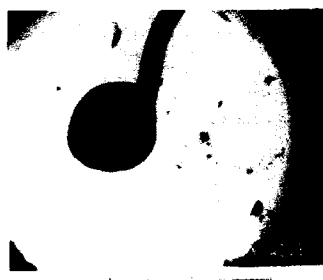


Fig. 1. The test structures used in these experiments. The middle $\text{Si}_{0.78}\text{Ge}_{0.22}$ layer was 0.17 μm , 0.34 μm , and 0.69 μm in the three samples, respectively.



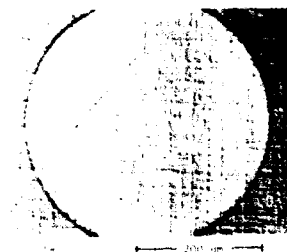
(a)



(b)



(c)



(d)

Fig. 2. Zero-bias EBIC images for the 0.17 μm sample (a), the 0.34 μm sample (b), and the 0.69 μm sample (c). In (d), an phase contrast optical micrograph of the 0.34 μm sample is shown.

profilometer to be about 50 nm in height.

The data presented so far is consistent with a straightforward interpretation that the 0.17 μm layer is thinner than the critical thickness for a $x=0.22$ Ge fraction, and that the thicker layers were over this critical thickness and hence had dislocations. However, it is generally accepted that the critical thickness for $\text{Si}_{0.78}\text{Ge}_{0.22}$ on Si, although somewhat dependent on growth conditions, is on the order of 50 nm, much less than necessary to interpret our results.

To investigate this anomaly, we etched away approximately half of the top Si cap (down to $\sim 0.6 \mu\text{m}$) on an unused piece of the 0.17 sample by careful plasma etching. Schottky barrier structures were then fabricated as before. EBIC measurements with no bias on these structures showed no defects as in fig. 2 (a). A reverse bias was then applied to the Schottky barrier to extend the Schottky barrier depletion region to the $\text{Si}_{0.78}\text{Ge}_{0.22}$:Si interface. Under such bias conditions, extended line defects (presumably misfit dislocations) were seen, with a spacing on the order of 10 μm (fig 3). Plan view TEM measurements performed on the sample also showed line defects, although with a spacing a factor of 10 closer. This discrepancy could be caused by the very variable spacing of dislocations within a sample and the small area sampled by TEM (about 2 square microns in this case), or could result if some dislocations were not electrically active (and hence gave no EBIC signal.) In any case, these measurements confirm that dislocations are present in the structure, and that the critical thickness is less than 0.17 μm , consistent with other work reported in the literature.

DISCUSSION

The EBIC technique depends on the recombination at defects affecting the current collected by the Schottky barrier, as is the usual case with minority carriers diffusing in a uniform piece of semiconductor. However, in the strained $\text{Si}_{0.78}\text{Ge}_{0.22}$:Si system (on Si substrates), a discontinuity on the order of 200 meV is expected in the valence band [4]. Therefore, in our original EBIC structures, any hole at an interface between the SiGe and the Si would tend to get trapped in the narrow gap SiGe alloy. Very few could make it to the Si cap to be collected as an EBIC signal, regardless of the presence of defects at either interface. Simple thermionic emission over a 200 meV barrier predicts a reduction of the signal by a factor of over 1000. This would explain the absence of defects in the image of fig 2(a). (See fig 4(a).) When the top Si layer was thinned and the Schottky barrier was reverse biased, the electric field from the surface extends down to the top SiGe:Si interface. With the help of this electric field, apparently holes can now acquire enough energy to get into the top Si to be collected. Thus the pattern becomes sensitive to the presence of defects (fig 4 (b)). From this one can conclude that when performing EBIC on heterojunction structures, for best imaging the minority carrier collector should be placed on the low gap side of the junction so that the flow of minority carriers is not impeded.

Since the initial probing conditions of fig 2 do not sample defects at the interfaces, the defects seen in these tests must now be in the top Si film. To confirm this, the sample of fig.



Fig. 3. EBIC image of the 0.17 μm sample after thinning and with a bias of 4.5 V.

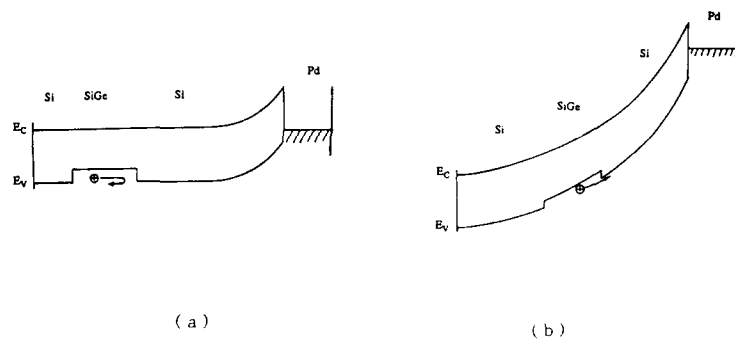


Fig. 4. Band diagrams of two samples with no bias (a), and with a 4.5 V reverse bias (b).

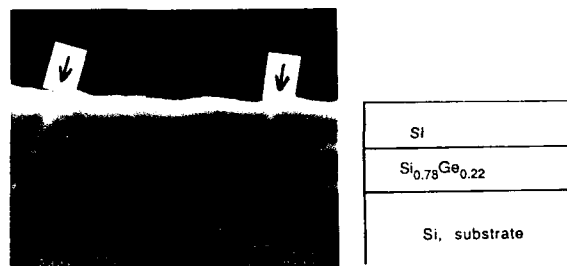


Fig. 5. Cross sectional SEM of the 0.69 μm sample after defect etching. Note the defects threading through the top Si film.

2(c) was cleaved and given a brief defect etch. The cross section was then viewed in an SEM (fig 5). The top Si and SiGe regions are clearly visible. Corresponding to each line defect on the top surface, a defect extending from the surface down to the SiGe layer was observed. This defect is apparently that which gave rise to the recombination observed by EBIC in figures 2(b), 2(c). Although the nature of this defect is not known, it can be assumed that it originated at one of the SiGe:Si interfaces because of the misfit dislocations. However, while dislocations were present in the thinnest (and thus presumably all) of the three samples, no defects extended into the top epitaxial Si of the first sample.

Thus, under our growth conditions, the criteria for defects in overlying epitaxial layers is considerably less stringent in terms of critical thickness than that for misfit dislocations at the interface. The absence of a cross-hatched pattern (indicative of no defects in the top epitaxial layer) is not a sufficient condition to infer an absence of misfit dislocations at the heteroepitaxial interfaces. This may be related to the fact that several types of dislocations to relieve strain have been found at Si:SiGe interfaces [1,2,3,7]. Some may lead to overlying defects while others may not.

CONCLUSION

EBIC can be a useful tool for looking at misfit dislocations in heteroepitaxial structures over a large area. However, one must be careful to insure that minority carriers at the heteroepitaxial interfaces may be collected. In $\text{Si}_{0.78}\text{Ge}_{0.22}$ structures, it appears that a certain amount of strain at interfaces may be accommodated by misfit dislocations without defects propagating upwards into overlying epitaxial layers. This is encouraging for the growth of defect-free "virtual" substrates.

ACKNOWLEDGEMENTS

This work has been supported by ONR (N00014-88K-0396), NSF (ECS-86157227), and the NJ Commission on Science and Technology. The advice of D. Ioannou regarding EBIC, the advice of J.M. Gibson and R. Hull on TEM sample preparation, and the assistance of E. Lenk on TEM imaging are all greatly appreciated. The assistance of S. Schwarz and B. Wilkens for SIMS and RBS is also gratefully acknowledged.

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STUDIES OF INTERFACE MIXING IN A SYMMETRICALLY STRAINED Ge/Si SUPERLATTICE

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ABSTRACT

Raman scattering and x ray diffraction were used to study the effects of annealing on a Ge/Si superlattice that had been grown upon a $\text{Ge}_{0.4}\text{Si}_{0.6}$ alloy buffer layer which distributes the strain between the layers. Anneals above 910K caused substantial mixing at the Ge-Si interfaces. The interdiffusion coefficients obtained from the x-ray data were found to obey an Arrhenius relation with an activation energy of $3.1 \pm 0.2 \text{ eV}$. Initial intermixing seems to be dominated by the diffusion of Si atoms into the Ge layers via a vacancy mechanism.

INTRODUCTION

Strained layer superlattice (SLS) structures composed of alternating layers of $\text{Ge}_x\text{Si}_{1-x}$ and Si have been extensively investigated during the past few years. Because these structures are generally grown on silicon substrates, strains are induced in the $\text{Ge}_x\text{Si}_{1-x}$ layers. However, Kasper, et al.[1] have recently demonstrated that many interesting and useful properties can be obtained by growing the Ge/Si SLSs on suitable $\text{Ge}_y\text{Si}_{1-y}$ alloy buffer layers. By matching the Ge/Si layer ratios to the appropriate buffer alloy compositions, Ge/Si SLS structures with pseudomorphicities well beyond those found for asymmetric strain distributions have been prepared [2-4]. However, Raman spectroscopy measurements of the optical phonons usually showed evidence for disorder at the interfaces between the Ge and Si layers in these samples [2-4] as well as asymmetrically strained superlattices [5]. Although perfectly abrupt interfaces will give rise to the Ge-Si vibrations near 400 cm^{-1} [5], which become stronger as the periodicity is decreased [3,4], thermally activated interlayer diffusion could enhance this disorder during growth. Consequently, the influences of growth temperature [6], substrate orientation [4], and annealing treatments [3,4,7,8] on the interfacial abruptness have been investigated. However, interpretations can be complicated by the difficulties in distinguishing among contributions due to strain relaxation [9], phonon confinement [10,11], and alloy formation [4,5] at the interfaces. The present paper describes the effects of furnace anneals (FA) and rapid thermal anneals (RTA) on the optical phonon spectra from Raman scattering and the x-ray diffraction reflections arising from the superlattice periodicity. The results obtained on a symmetrically strained Ge/Si superlattice imply that interface mixing initially occurs through the diffusion of Si into the Ge layers.

EXPERIMENTAL DETAILS

The sample used in this study had been grown at a nominal temperature of 673K by molecular beam epitaxy. A 200nm $\text{Ge}_{0.4}\text{Si}_{0.6}$ alloy buffer layer was initially grown on a (100)-Si substrate. The superlattice consisted of 50 periods, where the thickness ratio of individual Ge and Si layers ($d_{\text{Ge}}:d_{\text{Si}}$) was 2:3, which is estimated [2] to give lattice strains of

-2.4% and +1.7% in the Ge and Si layers, respectively. X-ray diffraction measurements [8] indicated that the as-grown periodicity was 3.3nm. Details of the growth procedures have been given previously [3,4].

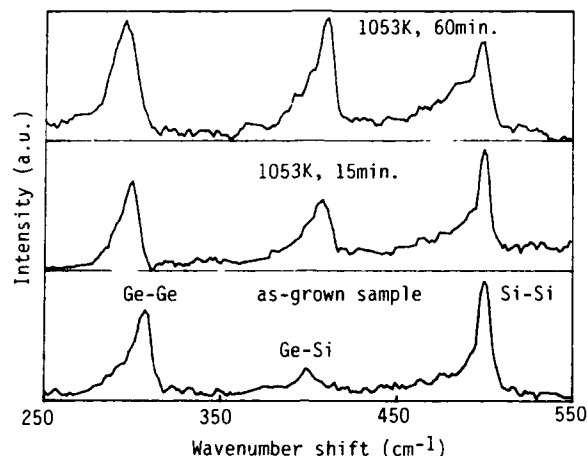


Figure 1. Raman spectra for as-grown and 1053K furnace annealed Ge/Si superlattice grown on a $\text{Ge}_{0.4}\text{Si}_{0.6}$ buffer layer on (100)-Si substrate.

The Raman experiments were performed at room temperature in a near-backscattering configuration on a system described earlier [3]. Most data were obtained with the 457.9nm line from an argon ion laser in order to limit the sampling depth to only the superlattice layers and to avoid any resonance enhancements to the phonon spectra.

Conventional x-ray diffraction techniques [8,12,13] were used to extract the interlayer diffusion coefficients (D_λ) from the intensities of the low angle superlattice reflection and the (-1)-order superlattice satellite of the (400)-peak. These measurements were made using $\text{Cu K}\alpha$ radiation in the $\theta-2\theta$ scanning mode on a powder diffractometer equipped with a graphite crystal diffracted-beam monochromator.

RESULTS AND DISCUSSION

The optical phonon portions of the Raman spectra for the as-grown Ge/Si sample as well as after FA for two different times at 1053K are presented in Fig. 1. Additional results on similar samples are also reported elsewhere [3,4]. The peak at 310.0cm^{-1} and 506.0cm^{-1} correspond to the Ge-Ge and Si-Si vibrations, respectively, from the strained layers. The relatively weak peak at 404.5cm^{-1} arises from the Ge-Si vibrations at the interfaces and corresponds to 1-2 monolayer of disorder [3-5] in the as-grown state. The anneals caused two major changes: (1) large increases in the relative intensity of the Ge-Si peak and (2) significant shifts to lower energy of the Ge-Ge peak. The increases in the Ge-Si peak intensity as a function of time for various temperatures during FA are shown in Fig. 2. These results suggest substantial interface mixing has occurred in the annealed samples. The shifts in

vibrational peak positions are given in Fig. 3 for both furnace and rapid thermal annealed samples. The Ge-Ge and Si-Si peaks moves to lower energies with increasing annealing time (note that the shifts are larger for the former peak), whereas the Ge-Si peak moves to higher energies. While the change in the Ge-Si peak position has been attributed [3,4] to alloy formation at the interfaces, it is difficult to separate possible phonon confinement [10,11] and strain relaxation [9] contributions. Hence, a quantitative assessment of the interdiffusion mechanism during the annealing process was not attempted from these Raman data. Nevertheless, the relatively large changes in the Ge-Ge peak positions imply that diffusion and/or relaxation may be more pronounced in the Ge layers. In the high temperature rapid thermal anneals, the red-shifts of the Si-Si peak also become large, which is in agreement with Brugger et al's [7] report.

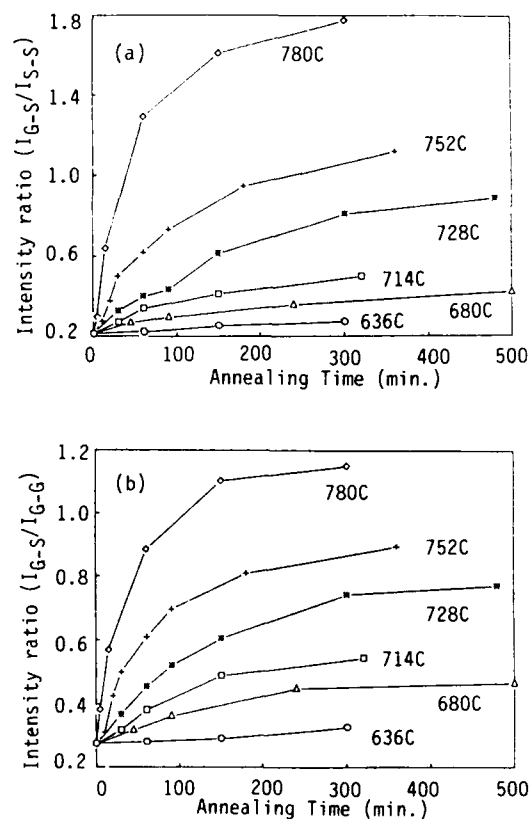


Figure 2. Intensity ratios of Ge-Si phonon mode to the Si-Si mode (a) and Ge-Ge mode (b) as a function of time at different annealing temperatures during furnace annealing.

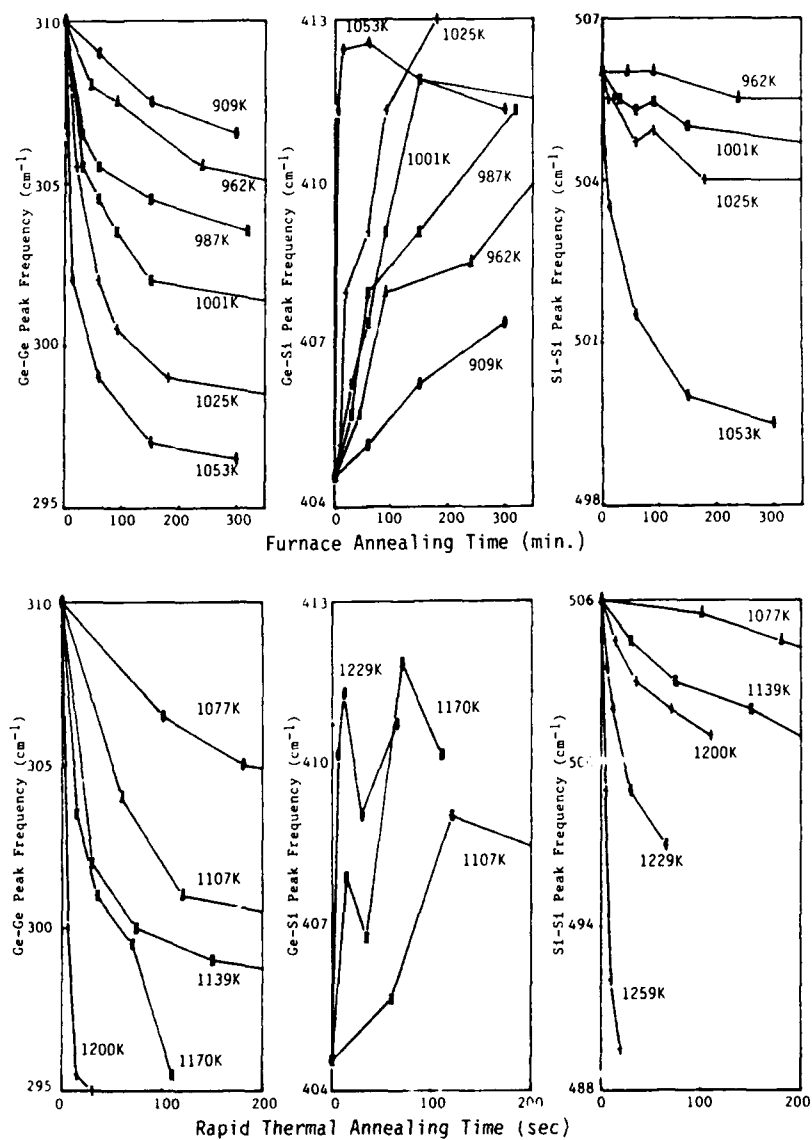


Figure 3. Frequency shifts of Raman peaks for different times at the given temperatures for FA (a) and RTA (b) treatments of the Ge/Si superlattice.

Multilayered or compositionally modulated structures can be analyzed by an x-ray diffraction technique [12] to obtain the interdiffusion coefficient with a lower boundary approaching $10^{-27} \text{ m}^2 \text{ sec}^{-1}$. An initial application of this method on the Ge/Si SLS sample gave [8] reasonable diffusion coefficients that obeyed the Arrhenius relation with an activation energy (E_a) of $3.1 \pm 0.2 \text{ eV}$. These results were based on the low angle composition modulation peaks for FA between 910K and 1053K and are reproduced in Fig. 4. The interdiffusion coefficients derived from the intensity ratios of the (400)-superlattice satellites for these samples are also shown in Fig. 4. Through the use of the RTA procedure, interdiffusion behavior at higher temperatures could be studied. The $D_\lambda(T)$ values obtained by RTA for temperatures from 1077K to 1259K are also shown in Fig. 4. The Arrhenius relation can fit the entire set of observed $D_\lambda(T)$ values. Hence, a unique activation energy of $3.1 \pm 0.2 \text{ eV}$ appears to describe the initial interdiffusion process for this crystalline Ge/Si superlattice over the temperature range between about 900K and 1250K. The self-diffusion and Ge impurity diffusion activation energy are about 5eV in crystalline Si [14], while self-diffusion and Si impurity diffusion have an $E_a = 2.9\text{--}3.1 \text{ eV}$ in crystalline Ge [14,15], as well as for Ge diffusion in $\text{Ge}_x\text{Si}_{1-x}$ alloys [16] with $x > 0.3$. The present x-ray measurements are also more consistent with intermixing occurring by diffusion processed in the Ge layers of the symmetrically strained superlattice. Mono-vacancy mechanisms are predicted [17] to give E_a values of 2.9eV and 3.2eV for Ge and Si self-diffusion, respectively. Hence, the $3.1 \pm 0.2 \text{ eV}$ activation energy in our experiments suggests that the interdiffusion processes for the Ge/Si superlattice also occur by the mono-vacancy mechanism. However, the possible influences of strain relaxation and dislocation generation during the anneals have not been determined, and the effects of gradient energy [18] may also be important for this small period structure. Consequently, experiments are underway on additional samples with different compositions and periodicities to assess more thoroughly these contributions. The results will be given elsewhere.

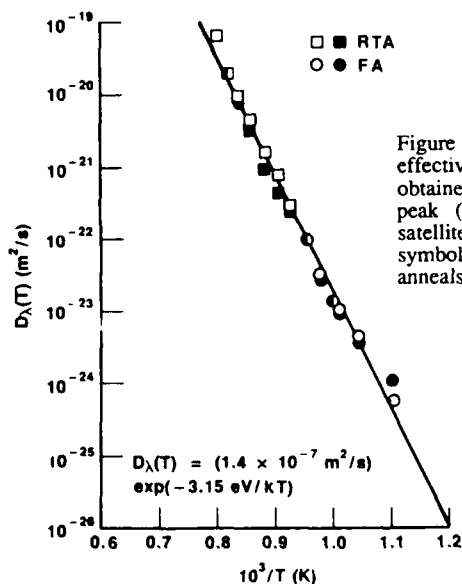


Figure 4. Temperature dependence of the effective interdiffusion coefficient $D_\lambda(T)$ obtained from the low angle superlattice peak (i.e., solid symbols) and the (-1)-satellite of the (400)-reflection (i.e., open symbols) after furnace and rapid thermal anneals.

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PART VII

Characterization of Defects
in Heterostructures I

A NOVEL METHOD FOR STUDY OF ROUGHNESS AT BURIED INTERFACES BY PLAN VIEW TEM: Si/SiO₂

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ABSTRACT

Interfacial roughness can be measured at buried interfaces using plan view transmission electron diffraction. The method relies on surface termination Bragg reflections and is applied to the Si/SiO₂ system. In contrast to other methods, this does not require stripping of the SiO₂ overlayer or projection assumptions. We find that thermal oxide interfaces are significantly flatter than previously supposed.

The Si/SiO₂ interface has been extensively examined by a wide variety of techniques. A subset of these studies have focussed on the interfacial roughness and it has been shown that increased step density reduces electron mobility.^[1,2] Although supporting the correlation of mobility with step density, the data presented here shows thermally oxidized Si/SiO₂ interfaces to be significantly flatter than previously assumed.

The most extensive study of Si/SiO₂ interfacial roughness, by Hahn and Henzler,¹ utilized the sensitivity of Low Energy Electron Diffraction to surface steps, by stripping the oxide layers in HF acid. The implicit assumption is that the exposed Si surface is identical to the buried interface. High Resolution Transmission Electron Microscopy (HRTEM) provided the first glimpse of atomic structure at the Si/SiO₂ interface.³ A careful statistical study was able to identify a correlation between roughness and electron mobility,² although assumptions about the effect of loss of information in one direction of the interface were required. This projection limitation has been shown to prevent unambiguous identification of interface structure.⁴ Incorporation of a limited signal-to-noise ratio would render such analysis even more pessimistic.⁵

In this paper we describe a novel method for studying interfacial roughness which does not require removal of the overlayer or projection assumptions. Furthermore, the technique is relatively simple, employing plan-view transmission electron diffraction measurements. We show that interface steps spaced between 30–300 Å can be readily identified in areas as small as 1 μ².

Our method evolved from the work of Lynch⁶ and Cherns,⁷ who demonstrated that certain Bragg reflections which are kinematically forbidden for infinite perfect crystals can be observed due to surface termination. These reflections, such as 1/3 422 on (111) and 110 on (001) f.c.c. crystal foils, are equivalent to the momentum transfer of (1,0) LEED beams but represent no bulk Fourier components. There are two equivalent ways of visualizing the origin of such surface termination reflections as we will demonstrate for the 1/3 422 reflection from an f.c.c. crystal. A single layer of material with the (111) surface normal scatters with amplitude $F \propto e^{2\pi i n/3}$ where $n=1$ for layer A, 2 for layer B and 3 for layer C. The amplitude-phase diagram for a (111) f.c.c. crystal stacked ABC is therefore an equilateral triangle and zero intensity results only for a foil of thickness $n = 3m$ layers exactly. A real foil containing surface steps will have some regions of thickness $n = 3m + 1$ and $n = 3m + 2$

vice versa). Note that steps on both surfaces can be equally observed and the presence of an overlayer of different structure has no direct effect. Cherns showed the application of this step imaging method to Au foils,⁶ Ourmazd et al. to Si⁸ and we have studied the native oxidation process in-situ in a UHV TEM with this method.⁹

The alternative view of surface termination reflections is as reciprocal lattice rods which come from a higher-order Laue zone. For the $1/3 \overline{422}$ reflection, this is a $1\overline{11}$ reflection in the first order Laue zone. Since the inter-zone separation is $\frac{1}{\sqrt{3}a}$ in the (111) direction, it is clear that dark field images taken with the $1/3 \overline{422}$ reflection should show foil thickness fringes of period $\sqrt{3}a$ as an example of weak beam imaging.

In this paper we focus on the observation of diffraction profiles from surface termination reflections without direct imaging. The imaging technique, although very powerful, requires both surfaces of the specimen be very flat. Information on statistical roughness can still be obtained by examining the spot profile of surface termination reflections, even if only one specimen surface/interface is relatively flat. To understand the technique we must consider the effect of surface roughness on the surface termination reflections in greater detail. Note that this analysis is very similar to that of X-ray crystal truncation rods.^{10,11}

If we make the reasonable assumption that steps on both specimen surfaces are uncorrelated, then we can show that the scattered intensity into the surface termination reflection from both surfaces add arithmetically. The scattered intensity from one surface is then

$$|F(s_x, s_y = 0)|^2 = \frac{F_g^2}{4\pi^2 V_c^2 s_z^2} \int e^{2\pi i(s_x x + s_z(f(x) - f(0)))} dx \quad (1)$$

where the surface is assumed to have fluctuating height $f(x)$ in only one direction. Note that this integral is familiar as the fourier transform of the crystal volume function ($V(r) = 1$ inside the foil and 0 outside), which is not linearly related to the surface profile's fourier transform, which is of interest. The integral can be solved analytically for some regular step distributions, for example a perfectly regular sinusoidal surface profile $a \sin(kx)$ gives rise to a spot profile $F(s_x) \propto J_n(2\pi a s_z)$ ($n = 2\pi s_x/k$) i.e. the spot is broadened due to roughness. To model a more realistic randomly rough surface we assume that the surface height follows a random walk with a large number of steps over the coherence area ($L_x \times L_y$). Such gaussian behavior predicts

$$|F(s_x, s_z)|^2 = \frac{L_x L_y^2 F_g^2 a}{4\pi V_c^2 s_z^2 \sin(\pi s_z a)} \left\{ \frac{(s_z a)^2/L}{\left[\frac{\pi(s_z a)^2}{L} \right]^2 + s_x^2} \right\} \quad (2)$$

where a is the average step height and L is the average step separation.

Qualitatively, we can see that roughness broadens the diffraction into surface termination spots. In the presence of high background (primarily inelastic) in selected-area electron diffraction patterns this can render the spot invisible, consistent with many failed attempts to observe such reflections on samples with poorly controlled specimens.

Specifically, we find that Si samples prepared by HF/HNO₃ chemical thinning have very rough surfaces¹² and do not permit observation of surface termination reflections (this corresponds to a step spacing less than ~30Å which is consistent with recent HREM observations by Ourmazd et al.)¹³.

Measurement of the half-width at half-maximum of surface termination reflections allows direct determination of L/a^2 from equation 2. The dependence of $|F|^2$ on s_x , obtained by tilting the specimen away from the zone axis, can be used to independently determine the step height a , allowing extraction of the step spacing L . In the following section we report measurement of these parameters for thermally-oxidized Si/SiO₂ interfaces.

Samples were prepared from Si (111) or (100) B-doped ~5Ωcm wafers which were oxidized in dry or wet O₂ at temperatures from 950–1000°C. Post oxidation annealing was carried out for some wafers in N₂ immediately after oxidation. Oxides with as-grown thickness 600–1000Å were thinned in HF to ~150Å. This was done to reduce background in diffraction patterns. Plan-view samples were prepared by HF/HNO₃ thinning from the backside until the Si thickness was ~1000Å in some areas. The oxide layer was protected from acid attack by beeswax. As previously noted, the HF/HNO₃ surface is very rough and does not contribute to surface termination diffraction spots in a significant fashion, so that observed diffraction arises from the Si/SiO₂ interface. This was confirmed in regions where the SiO₂ layer was removed in HF/HNO₃.

TABLE 1

Wafer Orientation and Resistivity	Oxidation Conditions	Post Oxidation Anneal (N ₂)	Fwhm (Å ⁻¹)	Resolution Limit (Å ⁻¹)	Calculated Step Spacing Å	Assumed Height
100 p-type (B) 3Ωcm	950°C	None	0.014±.007	0.008	110±60	(a ₀ /2)
	Dry O ₂	5 mins.	0.015±.002	0.008	105±15	
	600Å	15 mins.	0.010±.002	0.008	160±30	
		30 mins.	0.0083 ± .001	0.005	190±25	
111 p-type (B) 7Ωcm	Dry 1050°C 670Å	None	0.034±.014		60±25	(√3 a ₀)
		1 hr. 1050°C	0.0058±0.0004		360±30	
	Wet 1050°C 1000Å	None	>.04		<40	

Figure 1(a) shows an example of sharp $1/3\ 422$ spots seen in a well-annealed SiO₂ layer on (111) Si and (b) shows $1\bar{1}0$ spots seen from a well-annealed SiO₂ layer on (001) Si. These sharp diffraction features imply relatively flat Si/SiO₂ interfaces. To quantify this and other data, optical density measurements were made from photographic plates exposed in the linear response region of their emulsion. Background subtraction was performed on 2-dimensionally digitized intensity data. The peak was fitted to a Lorentzian as in Fig. 2 (eqn. (2)), from which the full-width at half-maximum was measured. Intensity dependence on s_z was used to

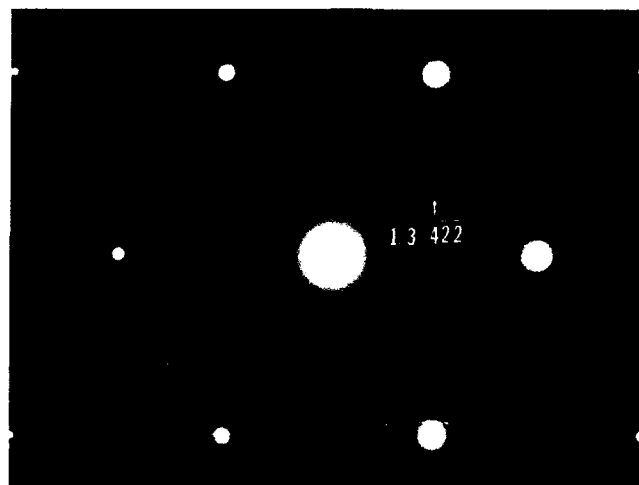


FIG. 1a

Fig. 1a A Plan-view diffraction pattern for a well annealed Si/SiO₂ interface recorded at 100kV. The Si substrate has been thinned to ~1000Å but the Si/SiO₂ interface is untouched. Sharp 1/3 (422) reflections are observed due to the flat interface.

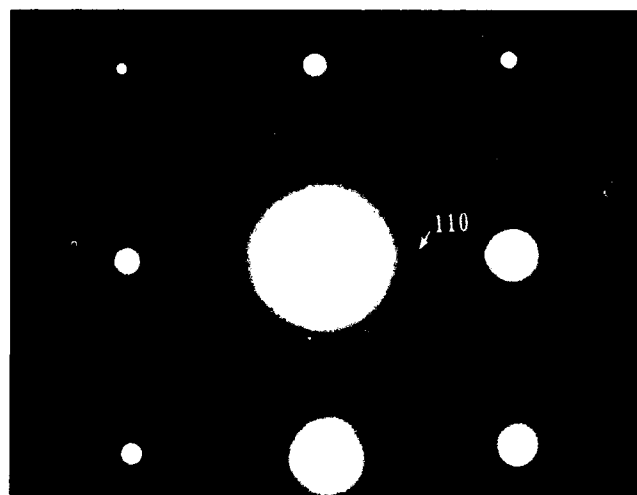


FIG. 1b

Fig. 1b A diffraction pattern from a well-annealed (001) Si/SiO₂ interface demonstrating sharp 110 diffraction spots.

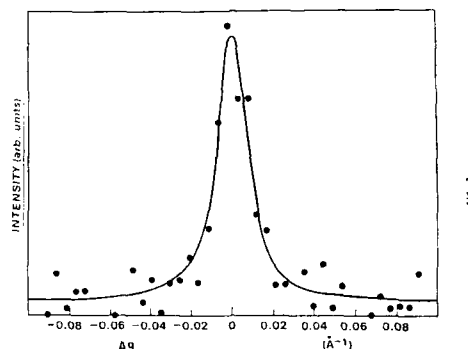


Fig. 2 The diffraction intensity profile around a type 110 diffraction spot obtained by optical densitometry and digital processing showing the background subtracted peak fitted to a Lorentzian (equation 2), which assumes 1-D roughness.

estimate step height a . The resulting values of step spacing L for a variety of oxides are given in table 1. The results show similar trends to those noted by Hahn and Henzler in their LEED study¹: dry oxides are generally flatter than wet (explained as a slower oxidation rate effect); (111) has larger terraces than (100) and post-oxidation annealing in an inert ambient drastically reduces roughness. In general, however, our results appear to show flatter Si/SiO₂ interfaces under comparable conditions. For example Hahn and Henzler report a step atom density of ~6% for a 1000°C (100) well-annealed oxide whereas our figures give a step atom density ($\frac{a}{L}$) of 1.4%. On (111) we observe step atom densities after comparable growth and annealing of <2.6%.

Note that there are upper and lower limits to the experimentally measurable step spacing: the lower is set by (inelastic) diffuse background scattering which renders broad spots invisible and the upper is set by limited coherence in the electron beam (~400Å). In general our results indicate considerably lower step atom densities than observed by Hahn and Henzler. Even though our model is simple, and should be extended to consider two dimensional roughness, we suggest that the discrepancy may arise from additional steps created during the HF stripping process used by Hahn and Henzler.¹ In-situ TEM studies in which step imaging was carried out,⁹ showed that dilute HF can increase the step density at the exposed Si surface.

At any rate, we demonstrate here a simple technique for determining statistical properties of interfacial roughness based on surface-termination Bragg reflections. The method does not require removal of the overlayer or projection assumptions and thus has advantages over previous studies. Furthermore it is simple and can be performed on microscopic (~1 μm²) areas. The method is very analogous to the study of crystal truncation rods by X-ray diffraction.^{10,11} Under suitable conditions it can be extended to direct imaging of individual steps at buried interfaces.⁹ For the Si/SiO₂ system we find evidence for significantly flatter interfaces than previously identified.^{1,2} On both (111) and (100) well-annealed interfaces step separations greatly exceed 100Å. The general trend of roughness with oxidation and annealing conditions is consistent with the landmark study of Hahn and Henzler,¹ in which correlation with electron mobility was observed.

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INTERFACE ROUGHNESS OF QUANTUM WELLS STUDIED BY
TIME-RESOLVED PHOTOLUMINESCENCE

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ABSTRACT

Optical properties of GaAs-Al_{0.5}Ga_{0.5}As multiple quantum wells affected by interface roughness have been investigated by time-resolved photoluminescence. The interface roughness affects on exciton dynamics is shown to be more complicated than those previously well studied line-width broadening of exciton transitions. A two-exponential decay of exciton luminescence and exciton peak shifting with increasing delay time have been observed. These observations have been successfully interpreted in terms of the interface roughness effects.

INTRODUCTION

The artificial structures of quantum wells (QWs) and superlattices (SLs) have revealed a wealth of novel physical phenomena.^{1,2} They have gained increasing interest in the last ten years because of their unique electronic properties³ and their promising applications in future electronic and optoelectronic devices.⁴ Interface roughness of QW affecting the optical properties has been studied by CW luminescence and photoluminescence excitation spectroscopy.^{5,6} The main effects are the linewidth broadening and Stokes shift of the emission spectrum: the exciton transition peaks in the emission spectrum generally are slightly shifted to the low energy with respect to the absorption or excitation spectrum maxima. In this paper, effects of interface roughness on the exciton dynamic process in QWs have been investigated. By well understanding these effects, time-resolved photoluminescence technique can be utilized to study the interface roughness structures in QWs.

EXPERIMENTAL

Samples used in this study were GaAs-Al_{0.5}Ga_{0.5}As multiple quantum wells grown by molecular beam epitaxy on a GaAs (100) substrate with no growth interruption and without cladding layers. The quantum well and barrier thicknesses are respectively, 250 and 278 Å, with total of 10 periods. Time-resolved photoluminescence spectra were obtained by using a YAG laser pumped dye laser (pulse width 7 ps, average power 20 mW) as an excitation source, and a time-correlated single-photon counting system together with a 1 m double monochromator as a detection system. Effective time resolution of the system is about 0.2 ns. Excitation light intensity is determined to be about 100 mW/cm², and excitation wavelength is 583.0 nm. Samples were mounted, strain-free, on a sample holder which was placed inside a closed-cycle He refrigerator. The measurement temperature was 8.5 K.

RESULTS AND DISCUSSIONS

In this study, we concentrate on the dynamics of exciton transition affected by interface roughness of QW. Fig. 1 is the plot of time-integrated photoluminescence emission spectrum (□ □ □) and time-constant of radiative decay (* * *) of 1S heavy-hole exciton. The spectrum line shape is asymmetric and the full line width at half maximum (FWHM) is determined to be about 1.75 meV. It is known that this line width is caused predominantly by interface roughness.⁵ Fig. 1 also shows that the decay time-constant decreases as the emission energy increases. The results shown in Fig. 1 can be understood by noting that different emission energies correspond to exciton recombination in different spatial domains. Because of the interface roughness, the quantum well thickness is no longer fixed, but rather fluctuating around the average well thickness. Thus spatial domains with lateral sizes varying from a few hundred angstroms to a few microns can be formed. Therefore, the lower (higher) energy shoulder appearing in the emission spectrum is due to exciton recombination in domains of wider (narrower) quantum wells. As quantum well width increases, the wavefunction overlapping between exciton electron and hole decreases, and

consequently, the decay time-constant of exciton is expected to increase.⁷ This is demonstrated by the experimental results shown in Fig. 1.

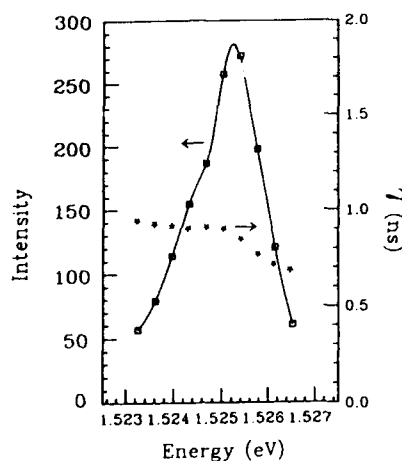


Fig. 1. Time-integrated photoluminescence ($\square \square \square$) and decay time-constant of radiative decay ($* * *$) of 1S heavy-hole exciton in $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ -GaAs MQWs. Temperature of measurements is 8.5 K.

Besides the radiative recombination, excitons can also migrate between different spatial domains. In general, the rate for excitons migrate from higher energy domains to lower energy domains is higher than that of the reverse process. Assuming N_1 (N_2) is the exciton population at higher (lower) energy E_1 (E_2) domains at delay time $t=0$, and N_1' (N_2') is the exciton population at the higher (low) energy domains at time $t=t_0$. Thus, the average energy of excitons at time $t=0$ can be written as

$$E_{ave}(t=0) = (N_1 E_1 + N_2 E_2) / (N_1 + N_2) = E_2 + N_1 \delta E / (N_1 + N_2), \quad (1)$$

where $\delta E = E_1 - E_2$. The average energy of excitons at delay time $t=t_0$ is

$$E_{ave}(t=t_0) = (N_1' E_1 + N_2' E_2) / (N_1' + N_2') = E_2 + N_1' \delta E / (N_1' + N_2'). \quad (2)$$

Notice that $N_2/N_1 < N_2'/N_1'$ because of the larger decay and migration rates for excitons in higher energy domains, which leads to $E_{ave}(t=t_0) < E_{ave}(t=0)$. Therefore, the observed exciton peak position is expected to shift towards the lower energy as delay time increases. This expectation has been demonstrated in Fig. 2(a), which shows the energy position at the heavy-hole exciton transition maximum as a function of delay time. The emission energy at the heavy-hole exciton luminescence intensity maximum has a red-shift at short delay times, and depicts a turnover at longer delay times. A maximum shift of about 0.1 meV at 4 ns delay time was observed.

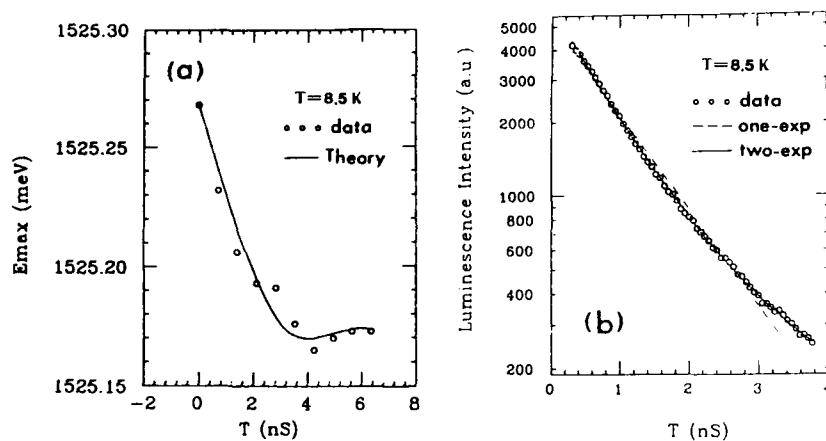


Fig. 2. Luminescence peak position of heavy-hole exciton as a function of delay time (a) and the temporal response of the heavy-hole exciton transition (b). The solid line in (a) is calculated from Eq. (4), and the solid line in (b) is a least square fit by two-exponential decay.

Measurements on time-resolved photoluminescence yield the results that the decay of the heavy-hole excitons shows exactly a two-exponential form.⁸⁻¹⁰ The result is shown in Fig. 2(b). The physical origin of this two-exponential decay has been fully explored.¹¹ The fast decay component is attributed to the exciton

radiative recombination; and the slow decay component (together with the fast decay component) is attributed to the migration of excitons between different spatial domains via acoustic phonon-exciton interaction.

The origin of the observed exciton transition peak shift cannot be correlated with the filling state phenomena,^{12,13} because of the temporal behavior. Due to the interface roughness, near the energy of the exciton emission intensity maximum, the decay time-constant of exciton, τ , depends on the emission energy, E , which can be written as $\tau(E)$. In the vicinity of the energy position of the exciton emission intensity maximum, the luminescence intensity as a function of the emission energy E and delay time t is¹⁴

$$I(E, t) = \exp[-(E-E_0)^2/\sigma^2] \{A \exp[-t/\tau_1(E)] + B \exp[-t/\tau_2(E)]\}, \quad (3)$$

where A and B are constants, and τ_i ($i=1,2$) is the time-constant which is a function of E . σ defines the linewidth which correlates QW thickness fluctuation parameter. From Eq. (3), we can derive an expression for the peak position as a function of delay time, t_d , as¹⁴

$$E_{\max} = E_0 + (\sigma^2/2) \left\{ \sum_{i=1}^2 [C_i \alpha_i t_d / \tau_i^2(E_0)] \exp[-t_d / \tau_i(E_0)] \right\} \\ \times \left\{ \sum_{i=1}^2 C_i \exp[-t_d / \tau_i(E_0)] \right\}^{-1}, \quad (4)$$

where E_0 is the energy position of intensity maximum at delay time $t_d=0$, α_i ($i=1,2$) is the rate of the time-constant change

with respect to the emission energy, $\left. \frac{d\tau}{dE} \right|_{E_0}$, $C_1=1$, and $C_2=B/A$.

The results of Eq. (4) is shown as a solid line in Fig. 2(a). The calculated results of heavy-hole exciton in Fig. 2(a) is obtained by using the parameters σ , $\tau_1(E_0)$, $\tau_2(E_0)$, and C_2 from experimental measurements which are $\sigma=1.05$ meV (FWHM= $2(\ln 2)^{0.5} \sigma$), $\tau_1(E_0)=0.9$ ns, $\tau_2(E_0)=4.2$ ns, and $C_2=0.15$. From Fig. 2(a), we see that the calculated results are in good agreement with experimental data.

In conclusion, we investigated the interface roughness effects on the dynamic process of exciton transitions. The interface roughness causes the excitonic transition maxima

shifting towards lower emission energy with increasing delay time and decay of exciton transitions to have a two exponential form.

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DEFECTS AT THE INTERFACE OF $\text{GaAs}_x\text{P}_{1-x}/\text{GaP}$
GROWN BY VAPOR PHASE EPITAXY

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ABSTRACT

Defects and microstructures in a ternary $\text{GaAs}_x\text{P}_{1-x}$ compound have been studied by transmission electron microscopy. The compound was grown on a (100) GaP substrate by vapor phase epitaxial. Crystal growth striation contrast was detected in a TEM image. This contrast was explained by local compositional variation of As and P. The distribution of misfit dislocations in the interface region was also studied.

INTRODUCTION

It is well known that a ternary $\text{GaAs}_x\text{P}_{1-x}$ compound can be grown by vapor phase epitaxy (VPE)[1]. A considerable amount of structural data has been accumulated concerning misfit dislocations near the interface between a GaAs substrate and epitaxially grown $\text{GaAs}_x\text{P}_{1-x}$, and concerning a cross hatch pattern on the growth surface[2-9]. Since GaP has a higher transparency, $\text{GaAs}_x\text{P}_{1-x}$ grown on a GaP substrate is preferable to obtain more intense light-emitting diodes. Furthermore, since yellow light-emitting diodes require materials with low As content such as $\text{GaAs}_{0.3}\text{P}_{0.7}$, the choice of GaP as a substrate material is more logical. Therefore, a $\text{GaAs}_x\text{P}_{1-x}$ layer has been grown on a (100) GaP substrate instead of a GaAs substrate by VPE. Structural properties of the ternary layer on a GaP substrate are less well known[4], so characterization has been carried out by transmission electron microscopy (TEM). The defect distribution in the compositionally graded region and local fine compositional variations were studied by TEM.

EXPERIMENTAL PROCEDURE

Epitaxially grown compounds were prepared using hydride vapor phase growth with AsH_3 , PH_3 and HCl gas carrying Ga. A homolayer was grown on a (100) GaP substrate, and then an AsH_3 gas flow was initiated to deposit a ternary $\text{GaAs}_x\text{P}_{1-x}$ compound. The ratio of the partial pressure of AsH_3 and PH_3 determined the composition of the deposited ternary compounds. The composition of the final layer is $\text{GaAs}_{0.07}\text{P}_{0.93}$ or $\text{GaAs}_{0.3}\text{P}_{0.7}$. In order to accommodate the lattice mismatch, a compositionally graded layer was fabricated between the homolayer and a final constant compositional layer of $\text{GaAs}_{0.3}\text{P}_{0.7}$. Both continuous and step compositional graded layers were grown. Thin foils for cross sectional electron microscopy were prepared by Ar ion thinning. TEM was performed by a JEM 2000EX operated at 200kV.

GROWTH PROCEDURES AND DISTRIBUTION OF DEFECTS

Growth of $\text{GaAs}_{0.07}\text{P}_{0.93}$ without a graded layer

The growth procedure for $\text{GaAs}_{0.07}\text{P}_{0.93}$ is shown schematically in Fig.1. The substrate temperature was lowered after the growth of a homolayer, because the optimum substrate temperature for $\text{GaAs}_x\text{P}_{1-x}$ layer is lower than that for the homolayer. No compositionally graded layer was required for the growth of $\text{GaAs}_{0.07}\text{P}_{0.93}$. A cross-sectional TEM image is shown in Fig.2. The dislocation network seen in the micrograph is a result of the sudden change in composition due to abrupt injection of AsH_3 gas. X-ray microprobe

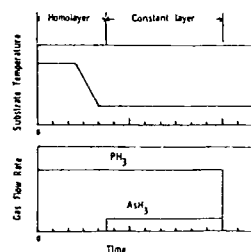


Fig. 1 Growth procedure of $\text{GaAs}_{0.07}\text{P}_{0.93}/\text{GaP}$.

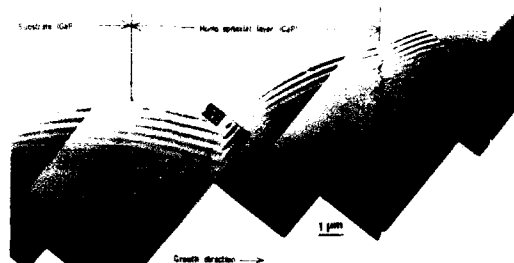


Fig. 2 Cross-sectional electron micrograph of $\text{GaAs}_{0.07}\text{P}_{0.93}/\text{GaP}$.

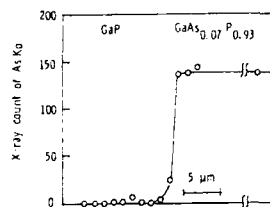


Fig. 3 An XMA analysis of As content.

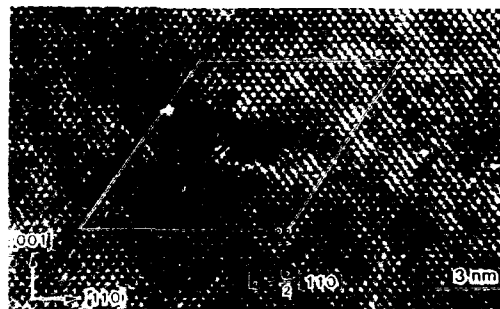


Fig. 4 A HREM image of a misfit dislocation.

analysis reveals the compositional variation along the growth direction shown in Fig. 3: The transition region between the substrate and the $\text{GaAs}_{0.07}\text{P}_{0.93}$ layer has a thickness of $2\ \mu\text{m}$ or less. A high-resolution image of one of the dislocations is shown in Fig. 4. An extra half plane is seen in the homolayer in the lower side of the micrograph. The dislocation is, therefore, a misfit dislocation. The Burgers vector of the dislocation is deduced directly from the Burgers circuit depicted in Fig. 4 and is $a/2\langle 110 \rangle$. It is not concluded at present that all of the misfit dislocations are of this type. Since the lattice mismatch between GaAs and GaP is larger than 3%, an abrupt change in the composition x by more than 0.07 resulted in a polycrystalline material. In order to grow a ternary layer with a composition $\text{GaAs}_{0.3}\text{P}_{0.7}$ on GaP, grading of the x -value in a step-wise or continuous manner is required.

Step-wise compositional grading in the growth of $\text{GaAs}_{0.3}\text{P}_{0.7}$

It is known that a compositional step gradient in the interface region suppresses the propagation of dislocations into the desired constant compositional layer, which is grown in compression[4]. This was well demonstrated for $\text{In}_x\text{Ga}_{1-x}\text{P}$ on a GaP substrate, but there have been very few reports about the present system in literature[4].

The ratio of the partial pressure of AsH_3 and PH_3 was changed step-wise three times, followed by a gradual change of the ratio. The substrate temperature was kept constant during the growth of the graded layer.

The cross-sectional electron micrographs shown in Fig. 5(a) and (b) exhibit a dislocation network (indicated by arrow heads). Since a very small leakage of AsH_3 was inevitable during the growth of the homolayer,

the dislocation network nearest to the substrate might have been introduced. Other networks perpendicular to the growth direction are related to the step-wise increase in the flow rate of AsH_3 . A gradual increase in the flow rate after the step probably results in dislocations dispersed throughout the area between the networks shown in Fig. 5(b). The network nearest to the growth surface seems to correspond to a temporary interruption in the growth of a constant composition. In the area between this dislocation network and the growth surface (represented by double arrow heads), neither dislocations nor grain boundaries are found in the electron micrograph.

Continuous compositional grading

In a continuous graded layer, dislocations were observed to be dispersed throughout the graded layer as we can see in Fig. 5(c). In the constant-composition layer, a dislocation network resulting from the interruption of epitaxial growth is observed as found in the previous specimen. This network is indicated by double arrow heads. Again, between this dislocation network and the growth surface, no dislocations or grain boundaries have been observed at present.

Growth temperature gradient together with continuous compositional gradient

The procedure in this section consists of applying a temperature gradient as the function of growth time during the growth of the graded layer. A cross-sectional micrograph is shown in Fig. 5(d). Dislocations are distributed randomly and the dislocation lines are not always perpendicular to the growth direction. It should be mentioned that a few dislocations are present in the constant layer. The dislocations are indicated by smaller arrow heads in Fig. 5(d). Since dislocations are not observed in the constant layer in the previously discussed specimens, we have to consider that the continuous temperature gradient resulted in the propagation of the dislocations in the constant layer.



Fig. 5 TEM micrographs of $\text{GaAs}_{0.3}\text{P}_{0.7}/\text{GaP}$. (a) Step graded procedure. (b) an enlarged image of (a). (c) Continuous graded and (d) temperature graded as well as continuous compositional graded procedures. Growth direction is indicated by an arrow.

CRYSTAL GROWTH STRIATION

Crystal growth striation was observed in cross-sectional TEM images of the VPE grown layer. In Fig. 6, dark field images from both the (011) and (01 $\bar{1}$) cross-sections of the same material are shown. The operating g vector in both images is the (200) reflection. Fringes are observed nearly parallel to the (200) plane in the (011) section, while the fringes in the (01 $\bar{1}$) image are tilted by 6 degrees from the (200) plane. Since the substrate surface was tilted from the (100) plane by 6 ± 2 degrees around the $\langle 011 \rangle$ direction, the observations show that this kind of variation occurs just along the growth direction.



Fig. 6 Striation in dark field TEM images of the (011) section in left, the (01 $\bar{1}$) section in right. Fig. 7 Dark field images with three different g-vectors.

Figure 7 shows a set of dark field electron micrographs of the same area with different g-vectors (022), (200) and (311). One can easily see the fine fringe contrast in the (200) dark field image. However, fringe contrast can be seen only in a very restricted area in the (022) and (311) images. Since the image employing the (200) type reflections is known to be compositionally or chemically sensitive [10,11,12], we believe that the striation is related to variation of the composition x. The chemical sensitivity of the reflection is usually explained in terms of the structure factor, or kinematical dark field intensity. We consider the dark field image intensity in the present ternary system based on the two beam diffraction approximation. The intensity of a dark field image I_g is given by [13]

$$I_g = (\pi / \xi_g)^2 \cdot \sin^2(\pi \cdot t \cdot s_{eff}) / (\pi \cdot s_{eff})^2 \quad (1)$$

where t denotes crystal thickness and ξ_g is the extinction distance proportional to the inverse of the structure factor F_g .

$$\xi_g = \pi \cdot V_c \cdot \cos \theta / (\lambda \cdot F_g) \quad (2)$$

The electron wavelength, scattering angle of reflection g and unit cell volume are, respectively, represented by λ , θ and V_c . The effective deviation parameter s_{eff} is given by

$$s_{eff} = \sqrt{s^2 + 1/\xi_g^2} \quad (3)$$

where s is the deviation parameter. Since we assume that the P sites are occupied by either P or As randomly, the atomic scattering factor of atoms in the site is

$$f(\sin\theta/\lambda) = x \cdot f_{As}(\sin\theta/\lambda) + (1-x) \cdot f_P(\sin\theta/\lambda) \quad (4)$$

Since no misfit dislocations were observed near the striation, it result from a kind of strain superlattice. Thus, the lattice parameter along the growth direction may be dilated or contracted locally. This, however, does not effect the image[13]. The variation of the contrast is mainly due to local variation of the scattering power, or the composition. We assume for simplicity that the reflection satisfies the Bragg condition exactly, so that we could omit the deviation parameter s in (3). Figure 8 shows the dark field image intensities I_{200} and I_{220} as a function of the crystal thickness t in $\text{GaAs}_{0.3}\text{P}_{0.7}$. Since the extinction distance for the 200 reflection is much larger (or an extremely small structure factor) than that of (220) reflection, very long period pendellösung of I_{200} can be seen in Fig. 8.

Compositional sensitivity of a dark field image is defined as

$$\partial I_g / \partial x \quad (5)$$

Positive sensitivity means that increasing x corresponds to the enhancement of the brightness in an image and vice versa. Since a small amount of compositional change does not affect the atomic scattering factors, we assume that they are compositionally independent. This assumption is verified in the simulated images described later. Then, the compositional sensitivity can be calculated as shown in Fig. 8. Both functions of I_g and $\partial I_g / \partial x$ have the same periodicity ξ_g with thickness. The phase difference between the functions is equal to $2\pi/4$. Therefore, the higher sensitivity is obtained in between the bright and dark band in a dark field image. High sensitivity is expected in a 200 dark field image in wide range of thickness. A wedge shaped crystal is usually prepared for transmission electron microscopy, so that the (200) dark field image provides high compositional contrast in much larger area. This is not expected in a (220) dark field image, because the sensitivity is high only in a very narrow range of the crystal thickness.

The dark field image intensity was simulated at 200kV based on the simple column approximation[13]. The results were shown in Fig. 9. In our

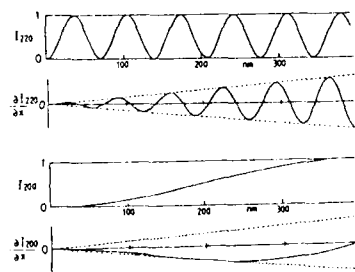


Fig. 8 Dark field image intensity and chemical sensitivity of 200 and 220 reflections as a function of t .

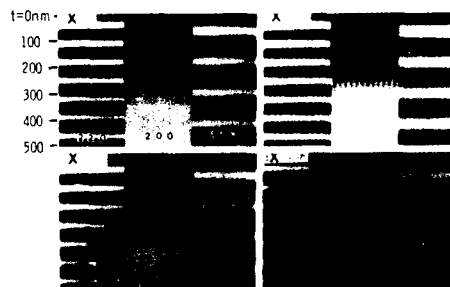


Fig.9 Simulated dark field images. Average composition is $\text{GaAs}_{0.3}\text{P}_{0.7}$

model, the composition x is varied sinusoidally in one dimension along the edge of a wedge shaped crystal. The thickness of the wedge shaped crystal t and the amplitude of compositional variation Δx are shown in Fig. 9. Here, it is assumed that the lattice parameters of the present ternary compound approximately obey Vegard's law as described in the literature[1,14]. Since the extinction distance of the (200) reflection is extremely large, the compositional sensitivity is negative in the whole area of the (200) dark field image; Dark lines in Fig. 6 correspond to an As rich region. The simulated images with compositional variation $\Delta x = 0.02$ well reproduce the image in Fig. 7. Therefore, local compositional variation during VPE growth is detected in dark field images, and the comparison between the observed images and the simulated images shows that the compositional variation is within $\pm 2\text{at.}\%$. The compositional variation is induced probably due to compositional fluctuation of gas flow through rotation of the substrate as observed in a MOCVD grown AlGaAs superlattice[15].

CONCLUSIONS

The distribution of misfit dislocations in $\text{GaAs}_x\text{P}_{1-x}/\text{GaP}$ was closely related to the growth procedures with a step or continuous compositional gradient and temperature gradient as a function of the growth time.

Compositional variation of As and P was detected within $\pm 2\text{at.}\%$. The chemical sensitivity of a dark field image was defined, and the usefulness of the (200) reflection was understood in terms of two beam dynamical theory.

ACKNOWLEDGMENT

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EFFECTS OF CHARGE TRANSFER ON THE MICROSCOPIC THEORY OF STRAIN-LAYER EPITAXY

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ABSTRACT

Whenever an atom of As is substitutionally replaced by a P-atom in a compound such as GaAs, due to the difference in ionicity, local puckering is effected by charge transfer. This paper deals with a calculation of the total energy stored, $E_{ex} = E(\text{strain}) + E(\text{interface}) = E_s + E_{int}$. For thick epilayers of GaP on GaAs, E_{ex} is dominated by E_s . However, for several atomic layers of GaP on GaAs, the dominant stored energy is actually represented by the electrical dipole-dipole energy at the interface. The creation of dislocations may release the strain energy, it cannot affect the interface dipole term. Only inter-diffusion can lower the interface energy.

INTRODUCTION

J.W. Matthews¹ and Matthews and Blakeslee² have shown that for film thicknesses below that at which misfit dislocations are formed between layers of a strain-layer superlattice, multilayers containing few dislocations can be made from materials with a significant mismatch in lattice constants. Recently, Fritz et al.³ found that strain relaxation proceeds more slowly than expected from equilibrium models. It is suggested that the driving force for relaxation is not the misfit stress, but rather an excess stress which includes the effects on the misfit dislocation tension.⁴ It has been further argued that the dislocation sources are inhomogeneous in nature resulting from local stress concentrations near the interface⁵. This paper deals with a calculation of the stored energy in an epitaxial strain-layer system of GaP on GaAs as a function of the layer thickness of the epilayer. Our calculated stored energy consists of the sum of the stored elastic energy and the stored interface energy. For thick epilayers of GaP on GaAs, the dominant contribution comes from strain. However, for very few layers, the interface energy due to the electric dipole-dipole interaction far exceeds the strain energy. This interface energy cannot be released by the creation of dislocations. Rather, inter-diffusion can lower the interface energy.

When GaP is epitaxially grown on GaAs substrates, the distances in the plane of the interface is constrained. However, the vertical separation may be adjusted because of charge transfer. Basically, electrons will be transferred from the less electronegative sites towards the sites having higher electronegativity?

EXCESS ENERGY IN A STRAINED EPILAYER

The excess energy of L number of strained epilayers of GaP on a GaAs substrate shown in Fig.(1) is calculated from a minimization of the total internal energy U ,

$U = U(\text{repulsive}) + U(\text{electrostatic})$. In Fig.(1), the a of GaP is confined to the GaAs substrate in the plane of the interface, the (100) plane, and leaving the vertical dimensions $\delta_i = \delta_1, \dots, \delta_L$ to be determined via a minimization of U . Instead of using the Madelung sum of the electrostatic term, we have chosen a unit tetrahedron for the calculation of the electrostatic energy, i.e.

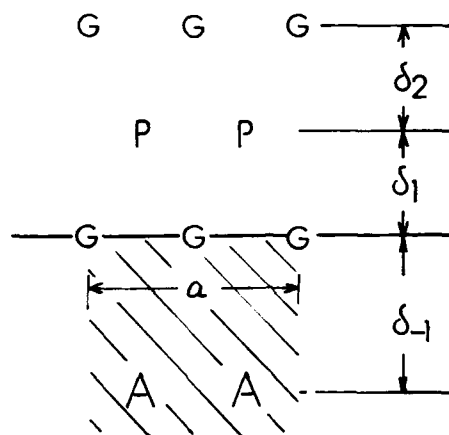


Fig.(1) Two epilayers of GaP are shown on a (100) GaAs substrate. Note that the distance in the (100) plane is fixed by the lattice constant of GaAs, while the vertical distances are adjusted via a minimization of the total internal energy.

$U(\text{electrostatic}) = U(\text{tetrahedron}) + U(\text{dipole-dipole}) + U(\text{higher order})$. In this work we have neglected the higher order multipoles. This procedure is similar to finding a faster convergence for the Madelung sum⁷. Table I gives the charges in various III-V of interest. In calculating the effective charge e^* , our starting point is the ionicity f . Using a simple heteronuclear diatomic model, $f = (1 - b^2)/(1 + b^2)$, in which the wavefunctions are $(1 + b^2)^{-1/2} (\psi_A \pm b\psi_B)$. Then using the 8-N rule, for GaAs, the effective charge $e^*(\text{Ga}) \approx 3/(1 + b^2) = 1.97e$ and $e^*(\text{As}) = -1.97e$ for $f=0.31$.⁸

From Kittel⁹, the repulsive energy U_R is given by

$$U_R = NZ\lambda \exp(-R/\rho) \quad (1)$$

in which R is the nearest neighbor distance. The parameter $Z\lambda$ and ρ are obtained from the relationship between the bulk modulus and the energy $U = U_R - \alpha q^2/R$, with α being the known Madelung constant. These values for various III-V compounds of our interest are included in Table I.

TABLE I

	$a(\text{\AA})$	$(Z\lambda)$ in 10^3eV	$\rho(\text{\AA})$	e^*
AlAs	5.66	8.29	0.33	1.91
GaAs	5.64	6.26	0.345	1.97
GaP	5.45	6.09	0.34	2.02

Due to the differences in the charge transfer of successive layers, δ 's are all different. We made a simplifying approximation by assuming all these δ 's are equal. Of course the value of δ for one layer will be different from ten layers, consequently this average value is a function of L , the number

of epilayers. For the interface plane of (100), the Ga-P distance in the plane is a , the lattice constant of GaAs, but the vertical distance is δ . Then the repulsive energy

$$U_R = (Z\lambda) \exp(-(1+8(\delta/a)^2)^{1/2} a/2.828\rho) \cdot (L+1)/2 \quad (2)$$

The energy of the tetrahedron, U_{tet} is given by

$$U_{tet} = \frac{(L-1)(2.02e)^2}{2a} ((1+16(\delta/a)^2)^{-1/2} - 5.657(1+8(\delta/a)^2)^{-1/2}) \\ + \frac{(1.97)(2.02e)^2}{4a} (5/16 + 0.5(\delta/a) + (\delta/a)^2)^{-1/2} \quad (3) \\ - \frac{(1.97+2.02)2.02e^2}{1.414a} (1+8(\delta/a)^2)^{-1/2}$$

The last two terms in Eq.(3) represent the electrostatic energy of a unit tetrahedron located just below the interface. The dipole-dipole term is given by

$$U_{d-d} = \frac{(1.97e)(2.02e)\delta a}{4(a/4 + \delta)^3} \quad (4)$$

Except the tetrahedrons at the interface, the dipole-dipole terms of all others are zero. Next, we minimize the total energy $U = U_R + U_{tet} + U_{d-d}$ with respect to δ , and calculated the total energy for the determined $\delta(L)$. Since we are interested in the excess energy due to the dipole-dipole and the strain energies, we subtracted from the calculated energy a term having $a(\text{GaP})/4$ for the vertical distance and $a(\text{GaP})$ in the plane. In other words we are calculating for the case of the unstrained GaP without the interface dipole term. Therefore the excess energy, E_{ex} , includes the dipole and the strain terms because we have eliminated the inherent energy of the crystal.

Figure (2) shows our result comparing with the classical stored strain energy for a film having two equal strains in the (100) plane and a stress free direction normal to the interface. The stored strain energy for this case is given by

$$E_s = 0.5 (C_{11} + 2C_{12})(1 - C_{12}/C_{11})S^2, \quad (5)$$

in which S for GaP on GaAs is 0.036. Note that the excess energy is normalized to \bar{X}^2 . (For a given (100) plane, there are two Ga atoms in an area of $(5.65)^2 \bar{X}^2$) The agreement of the asymptotic value of the excess energy with E_s is quite good considering that we have not used any adjustable parameters in our calculation. Also shown in Fig.(2) is the fact that the stored interface energy is far greater than the strain energy for $L=1$, being four times greater. This large stored interface energy serves to drive the inter-diffusion. At sufficiently low temperature of deposition, diffusion is difficult so that the epilayer is far from equilibrium.

CONCLUSIONS

Whenever there exist differences in ionicity, we claim that an excess interface energy must be present. Other strained-layer superlattices such as Ge/Si, GaAs/Si, etc., as well as the graded system of GaP on $\text{GaP}_{1-x}\text{As}_x$ may be treated similarly. The important concept obtained in our calculation is the appearance of a large interface energy. Creation of dislocations may

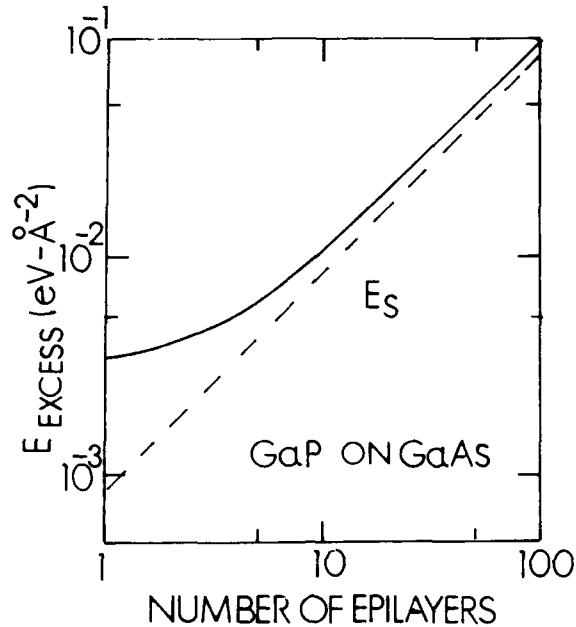


Fig.(2) Calculated excess energy in $\text{eV}/\text{\AA}^2$ versus the number of the epilayers, L . The dashed line is for the classical strain energy. Note that for large L , our result is 20% higher, which is quite good considering that no adjustable parameters were used.

release the stored strain energy. It cannot remove the interface dipole energy. Only a change of chemistry near the interface, for example, intermixing via diffusion at higher temperatures can affect this interface term. Therefore, this interface energy serves as a driving force of diffusion to increase the entropy of mixing. At low substrate temperatures, the system is metastable.

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POSITION-SENSITIVE ATOM PROBE AND STEM ANALYSIS OF THE MICROCHEMISTRY OF GaInAs/InP QUANTUM WELLS

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ABSTRACT

The recently developed techniques of pulsed laser atom probe microanalysis (PLAP) and position sensitive atom probe (POSAP) have been applied to the study of quantum well interfaces in samples that have also been well characterised by the more conventional techniques of TEM and STEM. These techniques have the potential for providing chemical information with a spatial resolution of better than 2nm, but the atom probe has the ability to independently resolve morphological and microchemical features of interfaces in three dimensions.

This paper presents results taken from GaInAs/InP MOCVD-grown samples, comparing information on well composition, and on the chemical abruptness and morphological roughness of interfaces using complementary analysis techniques. We have concentrated on obtaining reliable quantitative data on the phosphorous content of the GaInAs wells and on the gallium and arsenic contents of the InP barrier layers.

INTRODUCTION

The nature of the interfaces in quantum well structures is of crucial importance in determining how well they will perform both optically and electronically [1,2]; however, it is extremely difficult to reliably characterise the interfaces in such structures. We have used the very different, but complementary, techniques of STEM/EDX analysis [3] and PLAP [4] and POSAP [5] to examine the same set of samples, and have obtained consistent results with these microanalytical methods.

EXPERIMENTAL

The VG HB501 STEM used in this work has a lateral resolution for energy dispersive X-ray analysis of $\approx 2\text{nm}$, but must integrate the composition over the thickness of the specimen. The POSition Sensitive Atom Probe (POSAP) has sub-nanometre lateral and depth resolution and is capable of producing a three-dimensional reconstruction of the analysed volume. The STEM, however, can analyse a relatively large area in a matter of minutes, while the POSAP has a limited field of view ($\approx 10\text{nm}$) and takes several hours to produce an analysis. The wells examined by atom probe are selected randomly by the polishing process, while the cross sectional samples used in the STEM allow selection of the area to be studied. PLAP analysis is capable of providing relatively accurate compositional information from small ($\approx 2\text{nm}$) areas, while POSAP provides extremely good information on the morphology of structures, but the compositional data it provides is not as accurate as that obtained by PLAP or STEM analysis. The methods of sample preparation for atom probe analysis are described elsewhere [6].

RESULTS

The two sets of GaInAs/InP quantum wells used in this study were grown by Metal-Organic Chemical Vapor Deposition (MOCVD). The first set of wells was grown in a reactor containing a quartz wool baffle, the second in one without.

Sample Grown with Quartz Wool Baffle

Figure 1(a) shows a STEM micrograph of the first sample with a contrast intensity profile across it. The GaInAs wells (light) are of relatively poor quality, ranging in thickness from 3-

7nm, and appear to have rather diffuse interfaces. The contrast intensity profile shows a sharp increase at both edges of each well.

The first sample was analysed extensively in the STEM, with analyses of the well compositions being taken from the first ten and the last four wells. Figure 2 shows the compositions of each well analysed. It is clear that there is a significant amount of phosphorous in these wells, and that the phosphorous content is at a maximum of about 14% in the wells next to the substrate, and gradually decreases to a roughly constant level of about 5% in the wells next to the capping layer.

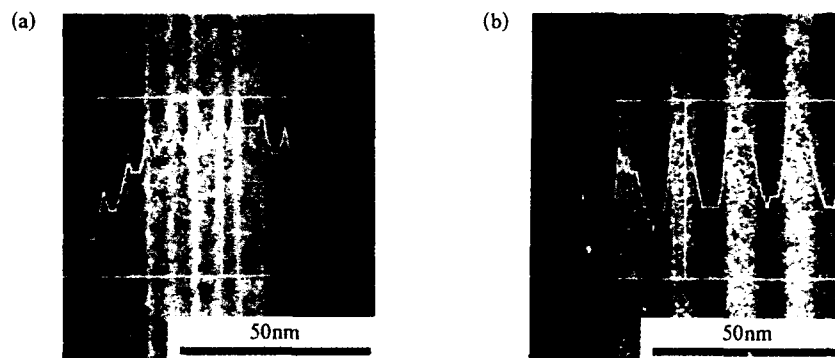


Figure 1. STEM micrograph and contrast intensity profiles of (a) wells grown with a quartz wool baffle in the reactor (sample 1); (b) wells grown without quartz wool baffle present (sample 2).

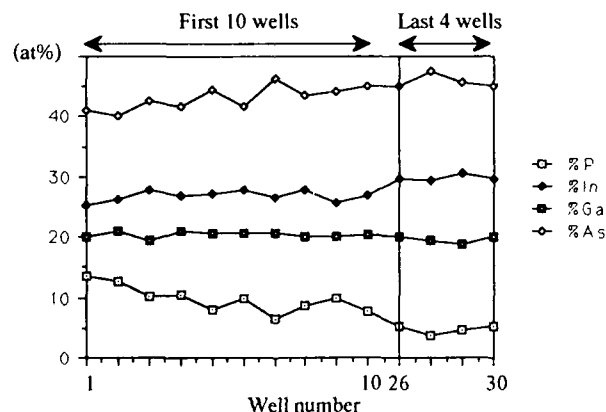


Figure 2. Compositions, in atomic %, of the first ten and last four wells of a 30 period stack of GaInAs/InP quantum wells (sample 1), as determined by STEM microanalysis.

Detailed analysis was carried out on the second well of this sample. Figure 3, a plot of In/Ga and P/As ratios, shows the results obtained. It can be seen from this plot that not only is there a high level of phosphorous in the well, but that the gallium profile lies inside the arsenic profile. Analyses taken from the barrier layers in this sample showed that they contained significant amounts of gallium and arsenic with compositions of up to 4% gallium and 5% arsenic.

This sample was also characterised by the POSAP and PLAP techniques. The STEM data from the second well, and PLAP data from an unknown position, are summarised in Table I.

The high phosphorous level observed in the well analysed by atom probe suggests that it is relatively close to the substrate. The composition of the wells appears to be that of a lattice matched quaternary.

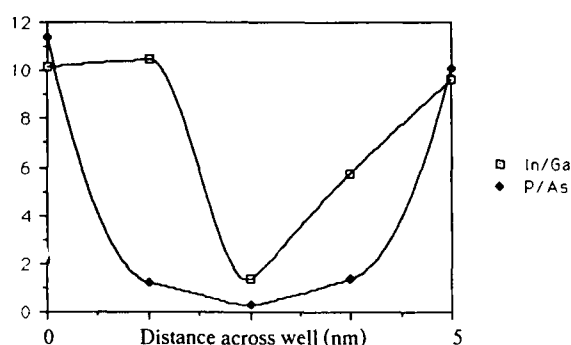


Figure 3. Plot of In/Ga and P/As ratios for a number of points across the second well from the substrate in the first sample.

Figures 4 and 5 show the POSAP composition maps and corresponding profiles for gallium and arsenic obtained from this well. The intensity of each pixel corresponds to the composition integrated over the area of the pixel and the thickness of material analysed. These maps show that the gallium distribution is rather patchy, and the overall gallium content of the well is below the nominal composition of 23.5%. It can also be seen from the maps that the arsenic distribution is wider than the gallium distribution. This is shown in the composition profiles from both the STEM and POSAP data, and in the contrast in the STEM image. The increase in average atomic mass at the edges of the wells, as arsenic substitutes for phosphorous, gives rise to the bright contrast at the well edges.

TABLE I: STEM and PLAP data obtained from wells in the first sample.

	%Ga	%As	%In	%P	Ga/As	In/P	%Ga+In	%As+P
STEM (accurate to $\pm 4\%$)								
Barrier	3.9	4.6	39.7	51.9	0.86	0.71	43.6	56.4
Well edge	4.0	24.4	41.5	30.2	0.16	1.37	45.4	54.6
Well centre	19.8	40.8	27.0	12.4	0.48	2.18	46.8	53.2
Well edge	6.5	23.7	37.2	32.7	0.27	1.14	43.6	56.4
Barrier	4.0	5.2	38.6	52.2	0.77	0.74	42.6	57.4
PLAP (accurate to $\pm 2\%$)								
Well	16.0	26.5	33.7	23.8	0.60	1.42	49.7	50.3
Barrier	6.8	10.6	40.4	42.1	0.64	0.96	47.2	52.7

Sample Grown without Quartz Wool Baffle

Data was also collected from wells in the second sample. The STEM data exhibited relatively uniform compositions from well to well, with small amounts of phosphorous in the wells, but both techniques showed relatively high levels of gallium and arsenic in the nominally pure InP barriers (see Table II).

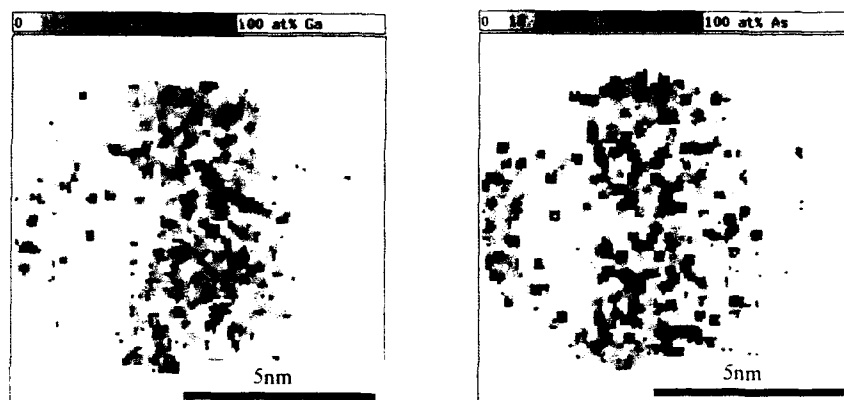


Figure 4. POSAP composition maps for gallium and arsenic from well grown with quartz wool baffle in reactor (sample 1). The maps show (moving from left to right) part of one well followed by a barrier, a complete well, and then another barrier layer

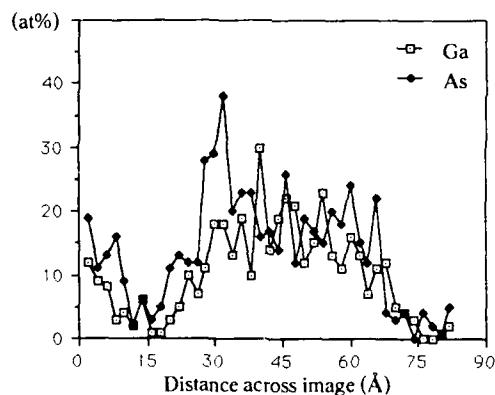


Figure 5. POSAP composition profile for gallium and arsenic across a well from the first sample.

TABLE II: STEM and PLAP data obtained from wells in the second sample.

	%Ga	%As	%In	%P	Ga/As	In/P	%Ga+In	%As+P
STEM (accurate to $\pm 4\%$)								
Barrier	1.6	3.2	46.7	48.6	0.50	0.96	48.28	51.7
Well	25.2	51.0	27.9	0.7	0.50	38.26	48.29	51.7
Well	25.7	48.9	24.9	0.5	0.53	46.09	50.57	49.4
PLAP (accurate to $\pm 2\%$)								
Barrier	4.8	9.5	48.9	36.8	0.51	1.33	53.7	46.3
Well centre	23.2	41.6	29.2	6.0	0.56	4.87	52.4	47.6

Figure 6 shows the composition maps for gallium and arsenic. The well in sample two is much more sharply defined than those in the first sample, but the arsenic distribution is again

wider than the gallium distribution. In the POSAP profiles (Figure 7) taken from each side of the well, the arsenic distribution extends beyond the gallium distribution on one side; this corresponds to the asymmetry in the contrast profile seen in the STEM image (Figure 1(b)).

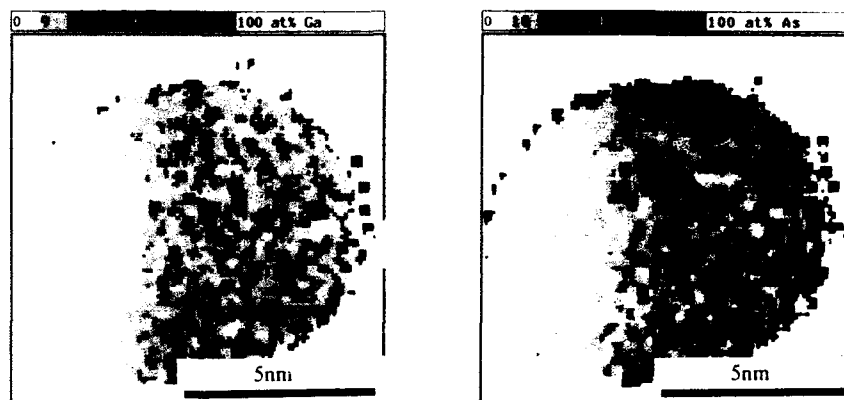


Figure 6. POSAP composition maps for gallium and arsenic.

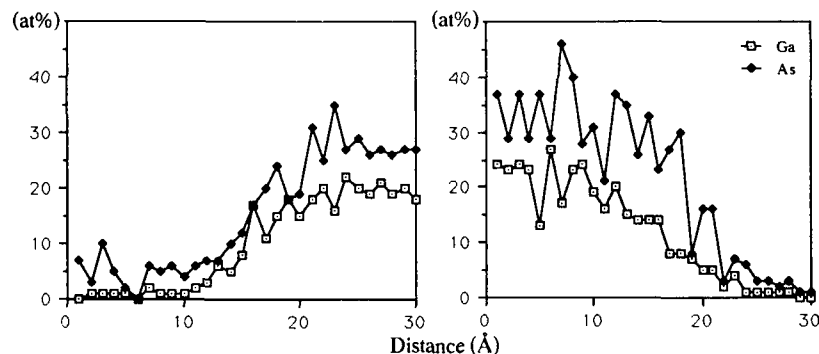


Figure 7. POSAP composition profiles across each interface of a well from the second sample.

In Figure 1(b) the contrast intensity profile shows an abrupt rise at the termination of each InP barrier, and a more diffuse profile at the end of each GaInAs well. The POSAP data acquired from this sample clearly shows that there is an arsenic "tail" extending from each well in the growth direction.

As a further illustration of the power of the POSAP technique Figure 8 shows cross sectional views of the same data shown in Figure 6, but in dot map format. The position of the interface is clearly apparent, and any steps or roughness can be easily identified. This section of interface is relatively smooth.

CONCLUSIONS

We have shown that the complementary techniques of POSAP, PLAP and STEM are capable of providing extremely detailed information on the composition of individual quantum wells, and on the chemical diffuseness and morphological roughness of their interfaces. The POSAP technique has been shown to give quantitative information on the extent of arsenic tails at well

edges which cannot be easily identified by STEM analysis. This information should prove useful in improving both the fabrication and assessment techniques used for these structures.

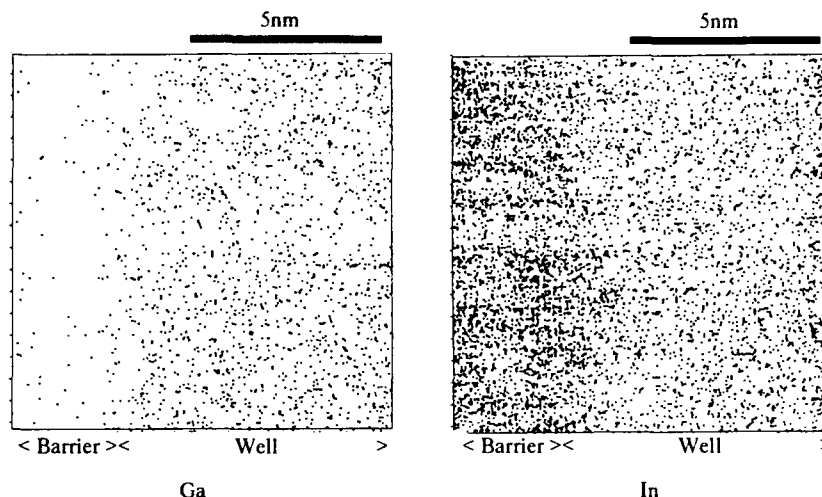


Figure 8. Cross sectional representation of the Ga and In distributions in the POSAP data obtained from sample two. The depth of material displayed is $\approx 10\text{nm}$. Each dot represents a single atom.

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A CORRELATION BETWEEN DEFECT PRODUCTION AND EXCITONIC EMISSION IN THE IRRADIATED ZnSe-ZnS STRAINED LAYER SUPERLATTICES

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ABSTRACT

The effects of thermal heat-treatment, N⁺-ion, Ar⁺-ion, γ -ray and electron-beam irradiations have been studied on MOCVD-grown ZnSe-ZnS strained-layer superlattices (SLSs) by means of low-temperature photoluminescence and X-ray diffraction measurements. As-grown SLS structure seems to be stable against the heat treatment compared to ZnSe thin film, but after the defects are introduced in the SLS by irradiation, additional fluctuation at the interface between the ZnSe well and the ZnS barrier layers takes place. However, no significant intermixing and the changes of strain can be detected in the irradiated SLS.

INTRODUCTION

Ion implantation and subsequent annealing are an efficient procedure to dope impurities and to control the structure of strained-layer superlattices (SLSs) for fabricating optoelectronics devices. Although it is important to understand the stability of the hetero-interface between the well and barrier, and the mechanism of the defect introduction, there are a few studies which concentrated on ion-irradiation effects of the II-VI compound SLSs [1,2].

Since the lattice mismatch between ZnSe and ZnS (4.5 %) is entirely accommodated by elastic strains within a 100Å thickness for each layer [3], it is possible to grow a high quality epitaxial ZnSe-ZnS SLS without generation of misfit dislocations. The fluctuation in the well width or at the hetero-interface shall change the optical transition energy and the linewidth of the exciton emission or absorption, and at the same time, the defects at the interface can trap excitons. Then it is necessary to control layer thickness within one monolayer and to reveal the correlation between the states of the interface and its optical properties before and after heat-treatment or irradiation.

In this paper, in order to investigate the influence of heat-treatment and defects creation by N⁺-ion, Ar⁺-ion, γ -ray and electron-beam irradiations on the ZnSe-ZnS SLSs, grown by the low-pressure metalorganic chemical-vapour-deposition (MOCVD) method, photoluminescence (PL) at 4.2 K and X-ray diffraction properties are measured.

EXPERIMENTAL PROCEDURE

ZnSe-ZnS SLSs were grown on (100) just-oriented GaAs substrates by the low-pressure MOCVD method using dimethylzinc (0.16 % concentration in He gas), H₂Se (10 % in H₂) and H₂S (10 % in H₂) gases. The growth temperature was 350 °C and the total SLS layer

thickness was about $1\mu\text{m}$. The samples were annealed for 30 min. in an atmosphere of H_2 gas (~ 20 Torr). N^+ and Ar^+ ion beams at an energy of 50 keV were irradiated at room temperature (RT) on the sample. The penetration depth of the ions into SLS is estimated to be $0.1\sim 0.5\mu\text{m}$ at 50 KeV. γ rays from Co^{60} (1.5 Mrad/h) and electrons with an energy of 10 MeV were found to penetrate the SLS completely. PL spectral measurements were made at 4.2 K using a 1.8 mW He-Cd laser (325 nm) as the excitation source and with a 1 m Jobin-Yvon grating monochromator. The SLS structures were characterized by the appearance of higher order satellite peaks in the X-ray diffraction spectra before and after the heat treatment or irradiation.

RESULTS AND DISCUSSION

Well-width dependence of the PL linewidth

Because of the step like density of states, it is expected that PL linewidth of a two dimensional superlattice becomes narrow compared to that of bulk crystal. However, the line broadening is caused by the following mechanisms: (1) the structural defects at the hetero-interface between the well and the barrier layers and (2) the interaction between exciton and phonons [4]. Especially, a correlation between the fluctuation of the hetero-interface and PL linewidth has been recently reported in InV compounds superlattices [5]. As shown in Figs.1 (A) and (B), two kinds of fluctuation are suggested [6].

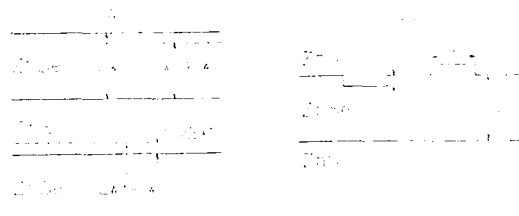


Fig.1 A schematic illustration for the fluctuation of the well width (A) and at the interface (B). $a_0/2$ shows one-monolayer thickness.

Fig.1 (A) describes the case that has different widths at each layer. As a result, the overlapping of the exciton emission lines, which correspond to respective well widths, causes the PL linewidth broadening. By controlling layer thickness, this problem can be overcome. On the other hand, the existence of islands and valleys at the hetero-interface (Fig.1 (B)) should be taken into account, because the optical transition occurs at energies which correspond to each well width as a result of the fluctuation of one well layer. It can be considered that the evaluation of the exciton-emission linewidth gives information on the control of layer thickness and the interface states of SLS. It has been reported that the ZnSe-ZnS SLS linewidth is about 50 meV [7], and it has an asymmetrical lineshape with a tail at lower energies which may originate from the $n=1$ free exciton emission and $n=1$ bound exciton emission. These overlap will form a single emission line [8]. We can obtain high quality ZnSe-ZnS SLS with the narrow PL linewidth of 15 meV. In Fig.2, the experimental results on the well-width dependence (the barrier layer, $L_b = 71\text{\AA}$) of the PL linewidth are

shown. It can be written as

$$\Delta H (dE/dL_w) \times \Delta L_w \quad (1)$$

where ΔH is the linewidth, E is the photon energy and ΔL_w is the fluctuation of the well width. (dE/dL_w) is the gradient of the emission energy as a function of well width. From eq. (1) we can see that if (dE/dL_w) becomes large and ΔH also becomes correspondingly large. The uniformity of the well width and the fluctuation can then be estimated by analyzing the linewidth broadening as a function of well width. If we assume that ΔL_w is one or two monolayers thick, by using eq.(1) and the experimental results of the well dependence of the photon energy (the insert in Fig.2), the curves in Fig.2 can be calculated. The experimental data in Fig.2 is higher in energy than the predicted theoretical results because of scattering of free excitons with impurities and phonons. From the data, it is possible to estimate the interface states using the well-width dependence of this linewidth, and then the fluctuation at the interface is evaluated to be $\Delta L_w = 2.0$ Å. This result is smaller than one monolayer, so we therefore suggest that there are valleys and islands at the interface. When the step height and the lateral extent of the islands and valleys are assumed to be δ_1 and δ_2 , the fluctuation at the interface can be calculated as shown in Table I, using Fig.2, eqs. (2) and (3) in Ref. [5] and taking $r_B = 28$ Å as the Bohr radius.

Thermal stability and the effects of irradiation

No significant PL spectral differences were observed in ZnSe-ZnS SLSs before and after heat-treatment at 580 °C [2]. As shown in Fig.3 (A), X-ray diffraction satellite peaks of ZnSe/ZnS SLS are retained even after heat treatment at 500°C, and the diffraction angles, 2θ , of the peaks are not changed. Since the peak intensities, normalized to the GaAs (400) $K\alpha_2$ peak intensity, are constant (Fig.3 (B)), the SLS structure can be considered to be stable against the heat-treatment.

N⁺ ion irradiation was performed with a dose of 2×10^{16} cm⁻²

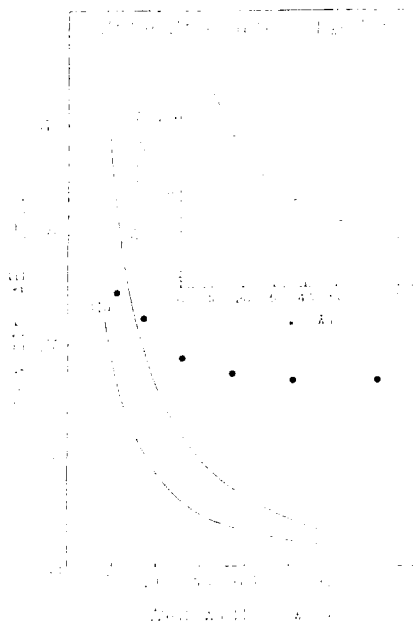


Fig.2 Well-width dependence of the exciton linewidth. ● shows the experimental results and the calculated curves are assumed that the fluctuation of the well width is (a) two monolayers and (b) one monolayer. The insert shows the well-width dependence of PL (4.2K) exciton peak energies.

Table I The interface fluctuation which fits with the experimental results.

δ_1 (monolayer)	δ_2 (Å)
2	5
1	7.5
1	10
0.5	20

on ZnSe-ZnS SLSs:
 (a) $L_w=11$ Å, $L_b=51$ Å,
 (b) $L_w=14$ Å, $L_b=22$ Å,
 (c) $L_w=38$ Å, $L_b=37$ Å,
 (d) $L_w=71$ Å, $L_b=71$ Å,
 where all the exciton lines originate from the $n=1$ heavy-hole free exciton. The PL bands have disappeared after the irradiation, and they were not recovered even after the heat-treatment at 350 and 400 °C. X-ray diffraction satellite peaks are diminished after subsequent heat-treatment at 500 °C, as shown in Fig.4 (A), and peak intensities are decreased (Fig.4 (B)). We found no variations in strain, which differs from Picraux's result [1]. It is suggested that N^+ -ion irradiation effect results in interdiffusion between the heteroepitaxial interfaces.

Ar^+ -ion was irradiation with a dose of 2×10^{14} cm $^{-2}$. PL emission intensity is weakened and deep-level intensity (about 550 nm) becomes strong in comparison with the exciton emission. In Fig.5 (a), it can be seen that the exciton-emission linewidth is narrow ($\Delta H=27$ meV) and the lineshape is rather symmetric. From Fig.2, the fluctuation at the interface can be estimated to be approximately one monolayer thick. After irradiation, the photon energy does not shift, but the linewidth is broadened (39.8 meV) and becomes 1.5 times larger than the original value, and the lineshape becomes asymmetric with a tail at the lower photon energy side, as can be seen in Fig.5 (b). It is apparent that the half linewidth at half maximum (HWHM) on the high energy side is almost constant, but it increases by more than 10 meV on lower energy side.

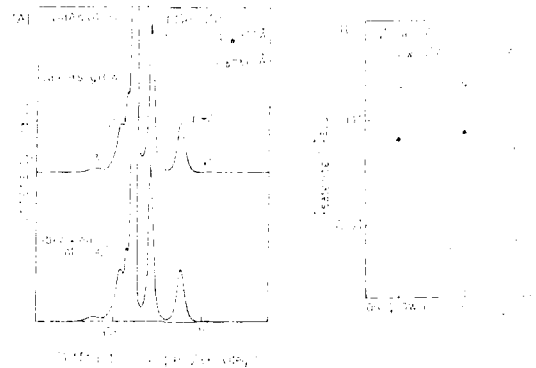


Fig.3 X-ray diffraction satellite peaks (A) and the variation of their intensities normalized to GaAs (400) $K\alpha_2$ peak intensity (B) before and after annealing.

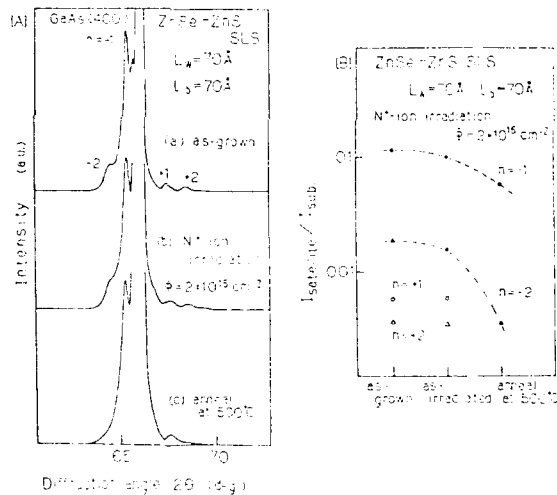


Fig.4 X-ray diffraction satellite peaks (A) and the variation of their intensities (B) before and after N^+ -ion irradiation and subsequent annealing.

There are two reasons for the additional linewidth broadening.

First, knock-on recoil atoms at the hetero interface between the well and the barrier layers cause an increase of interface fluctuation. If we assume that the fluctuation of linewidth and well width, before and after irradiation, are $\Delta H(0)$, $\Delta H(1)$, $\Delta L_w(0)$ and $\Delta L_w(1)$, respectively, from eq. (1),

$$\frac{(\Delta H(0) - \Delta H(1))}{(dE/dL_w) \times (\Delta L_w(0) - \Delta L_w(1))} \quad (2)$$

it is estimated that well-width fluctuation is increased by two monolayers after irradiation. Second, it is suggested that excitons bound to the irradiation defects will appear at the lower photon energy side of the free-exciton emission line, and their overlapping forms a single broad emission peak. It is necessary to irradiate SLS with a low dosage to analyze this broadening mechanism.

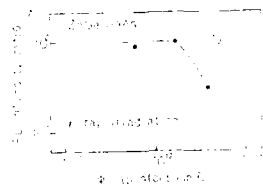


Fig. 6 [A] Variation of excitonic emission intensity as a function of γ -ray dose.

Next, the effect of γ -ray irradiation will be discussed. SLSs and ZnSe thin film were irradiated with a dose of 1×10^{11} , 5.9×10^{11} , 1.6×10^{12} and 3.8×10^{12} photons/cm², respectively. The SLSs show no change in both PL and X-ray diffraction spectra. On the other hand, the ZnSe PL emission intensity decreases for the donor bound-exciton, I_2 line (Fig. 6 (A)) and its line-width becomes rather broad as shown in (c) of Fig. 6[B] at 3.8×10^{12} photons/cm², but no energy shift of this line or significant deep-level emission band can be observed.

Electron-beam irradiation with a dose of 1×10^{14} , 1×10^{15} and 1×10^{16} electrons/cm² have no influence on SLSs, but the I_2 line intensity of ZnSe film becomes weak at 1×10^{16} electrons/cm² (Fig. 7). The comparison of the effect on irradiation between the SLSs and ZnSe film suggests that it is difficult to form complex defects or non-radiative defect

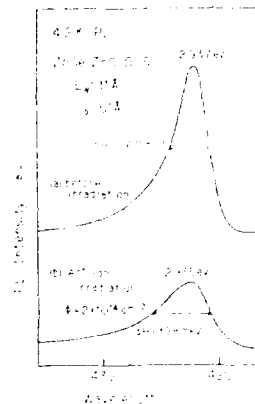


Fig. 5 Excitonic emission obtained at 4.2 K of ZnSe-ZnS SLS before (a) and after (b) Ar⁺ ion irradiation.

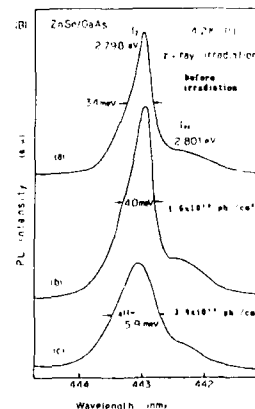


Fig. 6[B] PL intensity and linewidth as a function of γ -ray dose.

centers in the SLS after low-dose irradiation, because the present SLS suppresses misfit dislocations in the strained-layer or diffusion of impurities from the substrate.

CONCLUSION

We were able to control ZnSe-ZnS SLS growth within one monolayer by using low-pressure MOCVD and showed that it is possible to study lattice defect in this SLS. From the effect of heat-treatment and irradiations, the characteristics of ZnSe-ZnS SLS interface, deposited on (100) GaAs substrate, are stable against the heat-treatment at about 600 °C, and no significant interdiffusion is caused. Defects induced by irradiation behave differently in SLS from ZnSe film. In this work, irradiation dose dependence on the PL properties of SLS can be observed as a result of linewidth broadening at 4.2 K, and it is revealed that exciton emission line in the SLS is very sensitive to the defect creation in the heteroepitaxial interface states.

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Fig.7 The variation of excitonic emission intensity of ZnSe/GaAs irradiated with electrons.

EPITAXIAL GROWTH OF II-VI SEMICONDUCTORS ON VICINAL GaAs SURFACES

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ABSTRACT

We demonstrate that the use of vicinal (001) GaAs surfaces allows twin suppression in M.B.E. grown (111) CdTe. High Resolution Electron Microscopy is used to investigate the atomic structure of and the defects present at the interfaces, as a function of cutting angle and surface preparation. A model is presented that takes into account possible coincidences of facets in CdTe and GaAs in order to explain twin suppression, layer misorientation and the type of interfacial defects.

INTRODUCTION

In spite of the large lattice mismatch with most II-VI semiconductors, GaAs has been extensively used as a substrate for epitaxial growth of these materials mainly because of the potential technological implications and for its low dislocation density compared to available II-VI substrates.

We shall further concentrate on the growth of CdTe on GaAs for which the misfit is maximum (14.6 %). Growing CdTe in the (001) orientation onto (001) GaAs necessitates that the interfacial misfit be accommodated by an array of misfit dislocations running along the interface $\langle 110 \rangle$ directions [1][2]. Because of the high energy of such an interface, CdTe has a tendency to grow (111) on (001) GaAs. In this case, if the [112] CdTe direction coincides with the [110] GaAs one, the misfit in this common direction is reduced to 0.7 % in tension, whereas in the direction at 90° from this one, [110]GaAs/[110]CdTe, the misfit is kept at 14.6 % in compression.

However the major drawback of (111) growth is twinning which appears to be easy in most II-VI materials and which degrades the structural and optical properties of the epilayers [3].

We shall show hereafter that using vicinal GaAs surfaces [3][4] allows us to prevent (111) CdTe layers from twinning. This will be studied as a function of cutting angle and surface preparation.

EXPERIMENTAL

GaAs surfaces were cut of few degrees away from the exact (001) orientation by tilting around the [110] or $\bar{[110]}$ axes, exposing respectively Ga or As dangling bonds at step edges. The substrates were subsequently degreased, etched and deoxidized in an As flux at 600°C, according to a procedure described elsewhere [3]. Subsequent anneals were carried out in the deposition chamber and lead, according to the chosen conditions, to faceted substrates mainly with (115) and (117) facets or to regular surfaces with no facetting.

The overall structural quality of the obtained epilayer and the existence of twins were assessed by double-crystal X-ray diffraction and ion-channeling. These structural informations were compared to reflectivity and luminescence measurements [3]. We shall dwell here on the results obtained by high-resolution electron microscopy at 200 KeV (in a JEOL 200 CX microscope) and at 400 KeV (JEOL 4000EX) on the atomic structure of the CdTe/GaAs interface. The specimens were prepared in $\langle 110 \rangle$ cross-sections by Ar⁺ ion milling.

RESULTS

Fig. 1a is a micrograph of a typical interface between (111) CdTe and a nominal (001) GaAs substrate, when viewed along the 0.7 % misfit direction, the e^- beam being along the common [110] high misfit direction. Note that twinning occurs very close to the interface. We first have to emphasize that all layers deposited onto GaAs substrates tilted around the [110] direction, i.e. with As dangling bonds at step edges, did reveal considerable twinning as in the case of nominal substrates. Therefore all the results below concern vicinal GaAs surfaces with Ga dangling bonds at step edges.

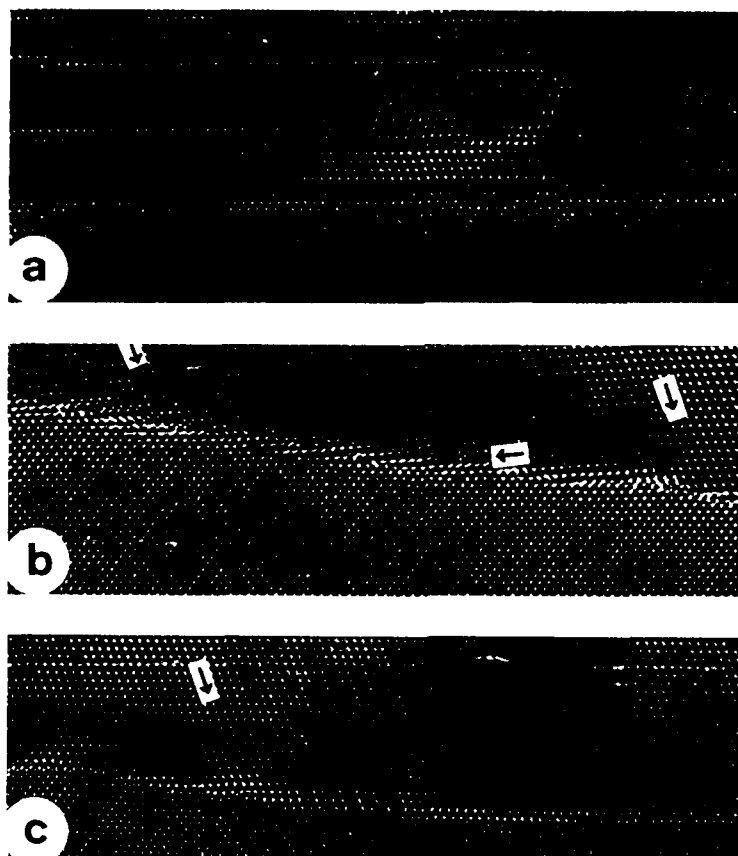


Fig. 1. (111) CdTe/(001)GaAs ; a : nominal surface ; b : 7.5° vicinal regular surface ; c : 2° vicinal faceted surface. Arrows denote (111) and (111) extra-half-planes.

Fig. 1b represents the interface obtained on smooth surfaces, when the GaAs substrate is cut at an average angle of 7.5° to the exact (001) orientation. Twinning has completely disappeared. In addition, the (111) CdTe planes are no longer parallel to the (001) GaAs planes, the misorientation angle being 3.1° as precisely determined from X-ray rocking-curves. There

also appears to be (111) and $(\bar{1}\bar{1}\bar{1})$ extra-half planes within the layer as denoted by arrows. The same observations were obtained for faceted surfaces cut at the same average angle of 7.5° , but in this case the misorientation was found greater, namely 5.3° . Fig. 1c is an image of the interface for a 2° cutting angle when the substrate surface was purposely faceted. In this case the misorientation angle is 0.65° and only widely separated dislocations with (111) extra-half planes could be detected on the analysed interfacial zone.

In all these cases, the (111) CdTe planes retain the same orientation with respect to the inclined GaAs surfaces, which, for the sake of brevity, will be referred to as the "+" orientation in the following. The twinned orientation, the "-" orientation, could never be obtained alone. (note that the "+" and "-" orientation refer to the same surface inclination). Fig. 2

DISCUSSION

The first point we would like to discuss concerns the layer misorientation with respect to the substrate. It is commonly said that the layer rotates in order to accommodate the misfit along the inclined interface. In other words, if a_l as a_s are the layer and substrate lattice parameters in the growth direction, and if δ is the cutting angle, the layer growth planes undergo a rotation i such that :

$$a_l / \sin(\delta+i) = a_s / \sin\delta$$

This presupposes a continuous atomic occupation of the lattice planes involved. One should rather try and find out if it is possible to bring the atoms that sit at the edge of terraces into coincidence, for terraces of equal number of atoms in both substrate and layer. Since these atoms truly define the inclined interface, one should further work out the strain necessary for these atoms to be coincident, in other words for growth to be coherent.

In this respect, Fig. 2a represents the atomic projections along the $[110]$ axis of a (001) GaAs vicinal sample, the surface of which would exhibit terraces of variable length. If N is the number of missing As atoms on the terrace (black dots), the Miller indices of the facets would be $(1,1,2N+1)$. The same scheme may be applied to a vicinal (111) CdTe surface and yields that successive facets have Miller indices of the type $(N+1, N+1, N-1)$ in the case of the orientation we defined as the "+" orientation (Fig. 2b) and $(N, N, N+2)$ in the case of the "-" orientation (fig. 2c).

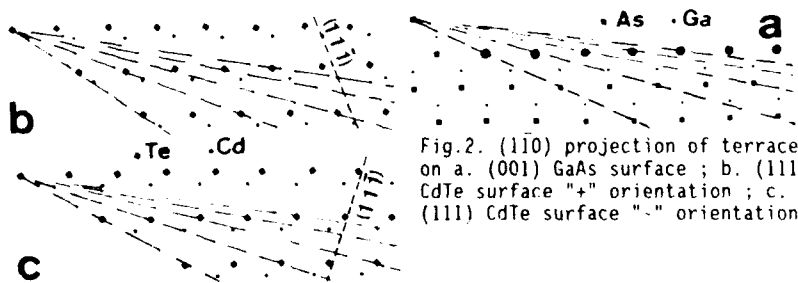


Fig. 2. (110) projection of terraces on a. (001) GaAs surface ; b. (111) CdTe surface "+" orientation ; c. (111) CdTe surface "-" orientation.

If one supposes that Te atoms occupy As vacant sites on the Ga stabilized GaAs surfaces [5], [6], [7], one has the same number of vacant As sites on the GaAs terrace and of Te atoms on the (inverted) CdTe terrace. If one tries to align the $(1,1,2N+1)$ GaAs facet with corresponding facets in CdTe, one has to rotate the (111) CdTe planes by an angle i such that :

$$(1) \tan(\delta+i) = 4/3\sqrt{2}(N+\alpha) \text{ where } \alpha=1/3 \text{ for the "+" orientation and } \alpha=2/3 \text{ for}$$

the "-" orientation.

The atoms on the edge of steps are not strictly coincident and coherent growth would require to strain the CdTe layer along the interface by an amount denoted ϵ_{\parallel} ,

$$(2) \epsilon_{\parallel} = (d_L - d_s)/d_s$$

where d_L and d_s are the distances between atoms sitting at step edges respectively in the layer and the substrate :

$$(3) d_s = (N+1/2)a_s/\sqrt{2} \cos \delta ; d_L = (N+\alpha) a_L \sqrt{6}/4 \cos(\delta+i)$$

with α defined as above.

Fig. 3 represents ϵ_{\parallel} as a function of N, number of steps on the terraces.

The main conclusions to be drawn are the following :

- 1- In the "+" orientation, the CdTe layers undergo a tensile stress, while the stress is compressive in the "-" orientation down to cutting angles of the order of 2° and then tensile again for lower angles.
- 2- For high cutting angles (low N), the "+" orientation is favoured because it induces less strain when growth starts (cf. fig. 1b).
- 3- Facetting, with (1,1,3), (1,1,5) or even (1,1,7) facets, leads to the "+" orientation as found in Fig. 1c (cf also fig. 5).
- 4- There happens to be a misorientation domain, around 2° , where growth should proceed in the "-" orientation since $\epsilon_{\parallel} = 0$. This was not observed experimentally.

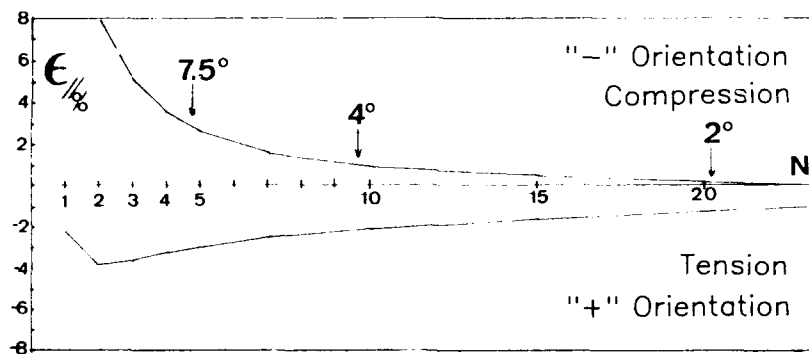


Fig. 3. Interfacial strain ϵ_{\parallel} as a function of N, number of atoms on the terraces.

As a conclusion, the "+" orientation is highly favoured in the case of high cutting angles and for faceted surfaces cut at a small angle from the (001) orientation as definitely found experimentally. For unfaceted surfaces with a low cutting angle down to nominal surfaces, twinning occurs presumably because widely separated steps of opposite signs coexist on the initial surfaces. One has to bear in mind that in the case of the "-" orientation, (111) CdTe growth is faster since only one atom is needed for the step to move on, whereas in the "+" orientation, both Cd and Te atoms are necessary. In the case where widely separated opposite steps coexist on the surface growth will proceed rapidly in the "-" direction from both sorts of steps, thus leading to the formation of twins. Indeed, if the starting surface of a nominal (001)GaAs is fairly rough, steps could be close to each other : growth would then proceed in the "+" orientation on each sort of steps, leading here again to the formation of twins and twin boundaries. This was definitely observed within small pits of ill-prepared nominal GaAs surfaces.

Relaxing the interfacial strain imposes that coincidences be found on the interface, namely that an integer p satisfies $pd_L = (p+1)d_s$, for the "+" orientation, where d_L and d_s are defined by (3). This does entail the existence of extra-half planes, in this case within the CdTe layer. The equivalent Burgers vector of a dislocation that would satisfy these conditions

would be $\vec{b} = d_L$. Perfect dislocations in CdTe have $\frac{a}{2} \langle 110 \rangle$ Burgers vectors

\vec{b} either in the (111) (set 1) or in the (11 $\bar{1}$) (set 2) planes. A vectorial combination of dislocations of set 1 alone or set 2 alone cannot amount to

the desired \vec{b} : one has to resort to n_1 dislocations of the first set

(Burgers vector \vec{b}_1) and n_2 dislocations of the second set (Burgers vector

\vec{b}_2) in order to achieve $n_1\vec{b}_1 + n_2\vec{b}_2 = \vec{b}$ as closely as possible.

On regular surfaces, this can, on the average, be achieved almost exactly and this succession of set 1 and set 2 dislocations was found rather systematically (fig. 1b), with no supplementary rotation compared to that given in equation (1). In fig. 1b, $(\delta+i)=2.85^\circ$ according to (1) is rather close to the experimental $2.1^\circ \pm 0.2^\circ$.

In the case of faceted surfaces, the situation is rather more complex. On either side of facets with low indices, the stress is alternately tensile and compressive (fig. 4).

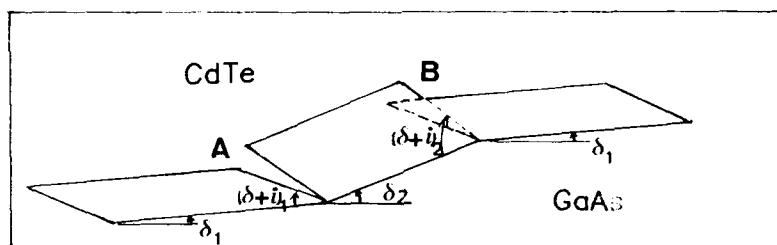


Fig. 4. Schematic of tensile and compressive zones on either side of a facet.

In zone A, the stress necessary to maintain atomic coherency is tensile: CdTe extra-half-planes are introduced so as to compensate for the different $(\delta+i)$ angles. In zone B, the stress is compressive: dislocations should have their extra-half-plane lying within or pointing towards GaAs. This is depicted in the micrograph of fig. 5: dislocations are found out where the inclination of the surface is suddenly increased as in zone B. These dislocations are frequently dissociated. Such dislocations are found of both set 1 and set 2. Since such dislocations have Burgers vectors with edge components opposite to those of interfacial dislocations, they will interact and lead to the formation of screw type dislocations as we have checked by Burgers vector analysis on these micrographs. No net additional misorientation will result from these zones.

On the contrary, the extra-half-planes introduced in zone A under the action of the tensile stress contribute to increasing the average misorientation angle up to a value intermediate between $(\delta+i)_1$ and $(\delta+i)_2$. In the case of fig. 5 $(\delta+i)_1 \approx 9.46^\circ$ ((1,1,11) facet) and $(\delta+i)_2 \approx 14.45^\circ$ ((1,1,7) facet). The experimental $(\delta+i)$ angle is found to be $7.5^\circ + 5.31^\circ = 12.81^\circ$.

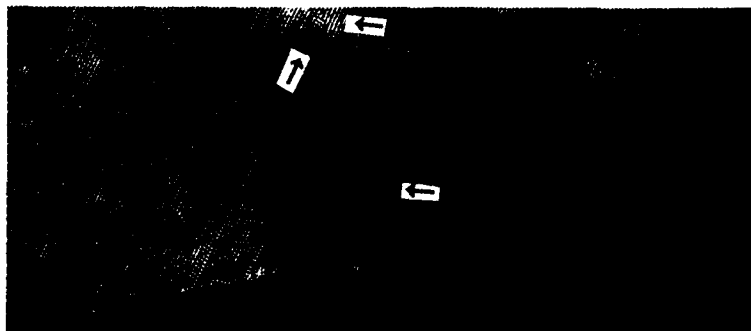


Fig. 5. Interfacial dislocation structure for a faceted 7.5° vicinal surface.

CONCLUSION

Growing (111)CdTe onto vicinal (001) GaAs surfaces has the definite advantage that it allows twin suppression in the layer. A high cutting angle (62.5°) and/or the creation of low indices facets facilitates twin suppression by favouring the "+" orientation against the "-" orientation. The possible occurrence of negative steps on poorly inclined or nominal surfaces is shown to induce twinning. Indeed, twinning could also happen if, for instance, the growth conditions are such that the diffusion length of impinging atoms is less than the terrace length. By close inspection of the quasi-coincidences of facets on (111)CdTe and (001) GaAs vicinal surfaces, we have worked out how much the layer rotates for coherent growth to occur. We also have shown that dislocations of both set 1 and set 2 are introduced to release the interfacial strain and that these dislocations do not introduce any additional layer misorientation in the case of regularly inclined surfaces. Faceted surfaces exhibit misorientations higher than the value deduced from the conditions for coherent growth. This was explained by considering the introduction of new dislocations on the tensile side of the facet and the annihilation of the edge character of dislocations introduced within the compressed region of the facet. This structural approach to the problem of twin suppression and strain relaxation for vicinal surfaces will be further extended by reference to growth dynamics.

Acknowledgements

We are indebted to J.L. Pautrat, Y.M. d'Aubigné and A. Bourret for their scientific direction and to the rest of the II-VI Epitaxy team for their fruitful collaboration. We thank C. Martin and C. Bouvier for their technical expertise.

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PART VIII

Characterization of Defects
in Heterostructures II

FORMATION OF INSULATING LAYERS IN GaAs-AlGaAs HETEROSTRUCTURES

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ABSTRACT

We describe two methods for producing thermally stable high resistivity layers in GaAs-AlGaAs heterostructures. These rely on the interaction of implanted ions with dopant impurities already present in a buried layer in the heterostructure. In the first case, oxygen implanted at a concentration above that of the acceptors in p-type GaAs is shown to create thermally stable, high-resistivity material *only* in the case of Be-doping in the GaAs. The effect is not seen for Mg-, Zn- or Cd-doping. Similarly there is no apparent interaction of O with n-type dopants (S or Si). The Be-O complex in p-type GaAs is a deep donor, creating material whose sheet resistivity shows a thermal activation energy of 0.59 eV. In the second case oxygen implantation into n⁺AlGaAs, followed by annealing above 600°C, creates a deep acceptor level that compensates the shallow donors in the material. Temperature dependent Hall measurements show the resistivity of the compensated AlGaAs has a thermal activation energy of 0.49 eV, in contrast to a value of 0.79 eV for ion-induced damage compensation.

INTRODUCTION

One of the primary advantages of GaAs technology over that of Si is the use of high resistivity substrates which reduce parasitic capacitances and increase device speed. Isolation between devices is then particularly simple if a selective implant process is used to fabricate doped regions for MESFETs. Increasingly however the high speed, III-V device arena is being dominated by the use of epitaxially grown GaAs-AlGaAs heterostructures which have a number of unique transport properties. Typically these heterostructures are deposited on a buffer layer on a semi-insulating GaAs substrate, the purpose of which is to reduce impurity diffusion from the substrate and to achieve the optimum morphology. In order to isolate devices from each other, this buffer would ideally be semi-insulating. However under most normal growth conditions in either Metal Organic Chemical Vapor Deposition (MOCVD) or Molecular Beam Epitaxy (MBE), this is not the case.

In this paper we report two methods by which thermally stable, buried layers can be produced in GaAs-AlGaAs heterostructures by the implantation of oxygen. We emphasize that this is not the usual damage-related compensation in which ions such as O, B or H are implanted at relatively low doses into GaAs and AlGaAs in order to create deep levels which trap the charge carriers in the material.⁽¹⁾ This creates high resistivity layers, but for temperatures above ~600°C the damage is annealed out and the material is returned to its original conductivity. While the thermally stable high resistivity layers can be selectively formed by masked implantation, for example in fabricating quantum well wires, the general method of oxygen incorporation into individual layers during epitaxial growth can be used to produce three-dimensional structures. In addition our experiments help to clarify the role of oxygen in GaAs and AlGaAs. In most epitaxial growth methods, water vapor or minor air leaks in the gas lines and growth chamber are usually present to a greater or lesser extent, and this makes oxygen a common contaminant in GaAs and related compounds.

EXPERIMENTAL

Two different types of sample were used in these experiments. In the first set, doped layers were formed in semi-insulating GaAs by multiple energy implants of Be, Mg, Cd and Zn (acceptors) or S and Si (donors). The energies and ion doses were chosen to create layers 3000-4000 Å thick and doped in the range $2 \times 10^{18} \text{ cm}^{-3}$ for donors and $\sim 8 \times 10^{18} \text{ cm}^{-3}$ for acceptors. The samples were then annealed using the proximity technique at 850°C for 3 sec (acceptors) or 900°C, 10 sec (donors). The sheet resistivity after these treatments is in the range 140-260 Ω/\square for Si or S implanted layers and 850-920 Ω/\square for Be, Mg, Cd or Zn implanted layers. All of the samples were then implanted with O^+ at 30, 60, 120 and 200 keV to a dose ranging from 2×10^{13} – $2 \times 10^{14} \text{ cm}^{-2}$ at each energy. This varied the O concentration from below the dopant density to value in excess of this density. The sheet resistivity was then measured as a function of annealing temperature (500-1000°C for 5 sec).

The second type of sample consisted of $\sim 2000 \text{ Å}$ of n^+ , Si-doped AlGaAs (0.22 AlAs mole fraction) on 5000 Å of undoped ($p \sim 10^{14} \text{ cm}^{-3}$) GaAs on a semi-insulating GaAs substrate. The layers were grown by MBE in a Varian Gen 11 system. Oxygen was then implanted at 40, 200 and 400 keV to doses between 10^{12} – $3 \times 10^{14} \text{ cm}^{-2}$ in order to create an approximately uniform oxygen concentration. The sheet resistivity of the samples was measured after annealing up to 950°C.

RESULTS AND DISCUSSION

Oxygen in GaAs

Figure 1 shows the sheet resistivity of GaAs doped with the various donor or acceptor species after oxygen implantation and subsequent annealing. In all cases the O concentration is a factor of two above the dopant concentration. With the exception of the Be-doped GaAs, all of the other material shows the typical evolution of sheet resistivity with annealing temperature, similar to that of GaAs doped with Mg, Cd, Zn, Si or S and implanted with oxygen.⁽²⁾ This is the behavior expected for damage-related compensation of carriers, which is removed once the damage is annealed out. Note that the p-type GaAs shows higher maximum resistivities than n-type material, which is a consequence of the lower hopping probabilities for holes trapped at implant damage sites, compared to those of electrons. By contrast, the behavior of oxygen-implanted, Be-doped GaAs is what would be expected of chemical compensation in the material. The other important point obvious from the data in Figure 2 is that when the O concentration is below the Be concentration, the GaAs does not retain its high resistivity upon annealing above $\sim 750^\circ\text{C}$. This is consistent with a threshold dose of O being needed to complex all of the Be ions. We emphasize that this is a chemical effect between Be and O. Figure 2 also shows the evolution of sheet resistivity of GaAs(Be) implanted with N at the same dose as the "high" O condition. The sheet resistivity in this case shows the usual damage-related compensation effect, which is removed once this damage is annealed out. The fact that the O concentration must be at least equal to that of Be implies the formation of a complex involving one Be ion and one oxygen ion. The simplest configuration would be a $\text{Be}_{\text{Ga}}\text{-O}_{\text{As}}$ nearest neighbor pair. Since it compensates the carriers in p-type GaAs the center must be a deep donor.

An estimate of the apparent energy level of the Be-O complex can be made from the temperature dependence of the sheet resistivity in Be-doped GaAs implanted with oxygen and annealed to remove the implant damage. Figure 3 shows this data for GaAs(Be) implanted with oxygen and annealed at 850°C, 10 sec, and for a control GaAs(Be) sample annealed at the same conditions. The activation energy in the former case is $0.59 \pm 0.05 \text{ eV}$. This is consistent with the high resistivity ($\sim 4 \times 10^7 \Omega/\square$) of the material after an 850°C anneal. By contrast, the GaAs(Be) displays an activation energy of only $44 \pm 21 \text{ meV}$. This is due to the shallow level Be acceptors in the material.

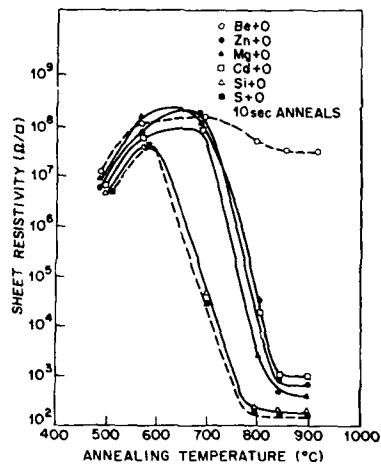


Figure 1 Sheet resistivity in GaAs doped with different donors and acceptors and implanted with O to give an oxygen concentration approximately twice the dopant concentration.

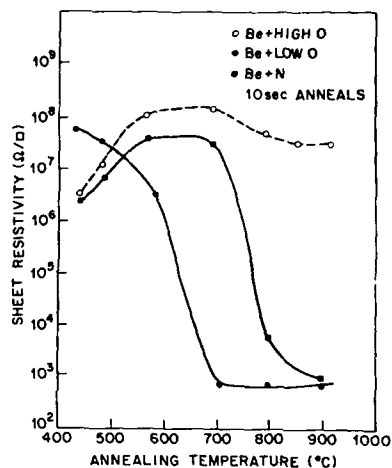


Figure 2 Sheet resistivity of Be implanted GaAs (annealed to activate the Be) subsequently implanted with O to give an O concentration either above (high O) or below (low O) the Be density, as a function of post-implant annealing temperature.

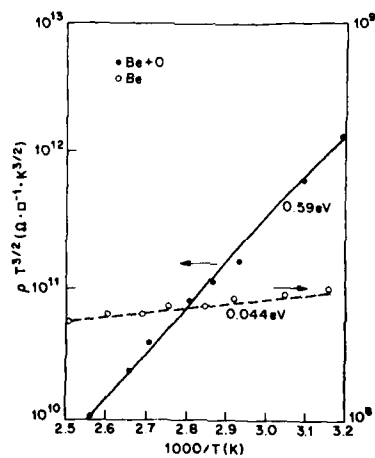


Figure 3 Measurement temperature dependence of GaAs(Be) or GaAs(Be+O) sheet resistivity. The Be and O was incorporated by implantation and annealing at 850°C, 3 sec.

We emphasize that the activation energy we measure for the GaAs(Be,O) material is an estimate only. The structure after O implantation and annealing consists of $\sim 5000 \text{ \AA}$ of resistive GaAs, on top of $\sim 500 \text{ \mu m}$ of semi-insulating material. The sheet resistivity of the substrate material is generally at least a factor of 5-10 higher than we have measured for the full structure here, implying significant conduction through the GaAs(Be,O) layer. As well, the Fermi level in the substrate is controlled by the mid gap donor EL2, and the measured activation energy for this is in the range 0.74-0.78 eV. A more accurate method of measuring the energy level of the Be-O complex in the upper thin layer would be by Deep Level Transient Spectroscopy (DLTS) which would require diode fabrication. From the difference in apparent resistivity of the structure compared to the substrate only, it is clear that there is significant conduction through the GaAs(Be,O) layer, and hence the apparent activation energy of 0.59 eV for the Be-O complex is a reasonable estimate.

We reiterate that oxygen implantation into GaAs doped with a variety of acceptors or donors created thermally stable, high-resistivity material only in the case of Be doping. When oxygen was implanted at a concentration lower than that of the Be, annealing above $\sim 700^\circ\text{C}$ caused a return of the resistivity of the material to its initial, pre-implanted value. Only in the case where the implanted oxygen concentration was equal to, or in excess of, the Be concentration was there creation of thermally stable, high-resistivity material.

Oxygen in AlGaAs

The resistivity of the AlGaAs-GaAs structure is shown in Figure 4 as a function of O implant dose and annealing temperature. For low doses ($\leq 1 \times 10^{13} \text{ cm}^{-2}$ at 40 keV) the evolution of the resistivity with annealing temperature can be completely explained by the usual damage-induced compensation arguments.

For the dose of $5 \times 10^{13} \text{ cm}^{-2}$ (40 k·V) + $1 \times 10^{14} \text{ cm}^{-2}$ (200 keV) + $1.5 \times 10^{14} \text{ cm}^{-2}$ (400 keV), where the O concentration will be comparable to the electron concentration, the resistivity of the AlGaAs stays high ($> 10^8 \text{ } \Omega/\square$) until 800°C and then falls by three orders of magnitude after a 900°C anneal. Under these conditions there may well be very close chemical compensation of the electrons by deep O-related acceptors, explaining the higher thermal stability of the high-resistivity layer. At 900°C any significant amount of O diffusion or clustering would lower the concentration below the threshold for complete chemical compensation, and thus the resistivity of the AlGaAs falls.

At O implantation doses of $1 \times 10^{14} \text{ cm}^{-2}$ (40 keV) + $2 \times 10^{14} \text{ cm}^{-2}$ (200 keV) + $3 \times 10^{14} \text{ cm}^{-2}$ (400 keV), the oxygen concentration is well above the initial electron density in the AlGaAs, and this correlates with a considerably greater thermal stability of the now high-resistivity AlGaAs. To ensure the high-temperature stable compensation is indeed a chemical effect due to the presence of a high concentration of oxygen, we implanted N at similar energies and doses into the AlGaAs-GaAs structure. The variation of the resistivity of the structure was exactly as expected for damage-only compensation, with a complete return of the initial conductivity for annealing temperatures above $\sim 700^\circ\text{C}$. There was no evidence of any thermally stable, chemically induced compensation.

The temperature dependence of the AlGaAs resistivity was then measured to obtain the activation energies corresponding to different annealing temperatures after oxygen implantation. Figure 5 shows the resistivity of the AlGaAs implanted with O at a dose of $1 \times 10^{14} \text{ cm}^{-2}$ (40 keV) + $2 \times 10^{14} \text{ cm}^{-2}$ (200 keV) + $3 \times 10^{14} \text{ cm}^{-2}$ (400 keV) and then annealed at either 400°C , where damage effects will still be dominant, or at 900°C , where the chemical effect of the O will be the impurity compensation mechanism. In the former case the resistivity shows an activation energy of 0.79 eV, consistent with the creation of midgap levels associated with the implant damage.⁽¹⁾ In the latter case, the 900°C anneal removes all of this implant damage, and the activation energy of 0.49 eV must be associated with an oxygen-related deep level. This value is consistent with a level

measured by capacitance spectroscopy in metalorganic chemical vapor deposition grown AlGaAs samples in which O_2 was deliberately injected during the growth.⁴¹ At constant oxygen concentration, the electron concentration in the material fell as the aluminum mole fraction was increased, suggesting an interaction between Al and O.⁴² There was a direct correlation between the reduction in the doping density in the AlGaAs and the increase in concentration of the deep level. This level is presumably due to a deep acceptor-like center that is able to compensate the shallow donors in the AlGaAs. In Fig. 5 we also show the temperature dependence of resistivity in a sample implanted with O at a dose of $5 \times 10^{12} \text{ cm}^{-2}$ (40 keV) + $1 \times 10^{13} \text{ cm}^{-2}$ (200 keV) + $1.5 \times 10^{13} \text{ cm}^{-2}$ (400 keV) and annealed at 400°C. This sample also shows an activation energy of ~0.8 eV, consistent with damage-induced compensation. In samples receiving the same dose but annealed above 700°C, where the initial conductivity of the material has been restored, the activation energy of the resistivity was below 0.1 eV and is due simply to the shallow states due to the Si doping.

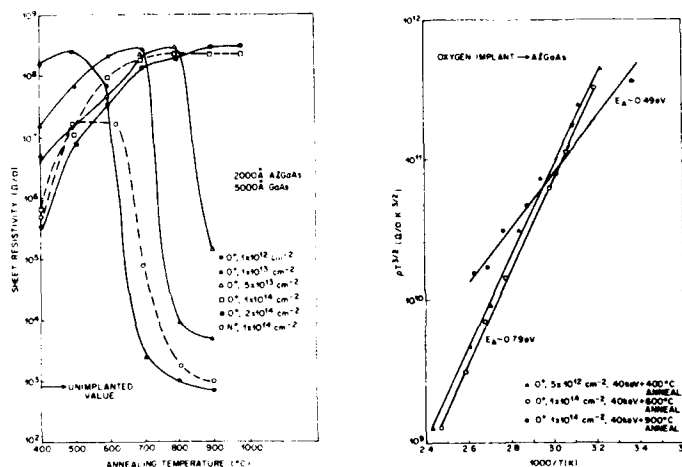


Figure 4 Sheet resistivity of AlGaAs-GaAs. Figure 5 Temperature dependence of resistivity structure implanted with O or N at various doses. in O-implanted AlGaAs-GaAs structure as a function of post-implant annealing temperature function of annealing temperature and implant dose.

We also implanted Be into AlGaAs and then annealed at 850°C for 3 secs to produce p-type layers whose sheet resistance varied from 183 Ω/\square for $\text{Al}_{0.09}\text{Ga}_{0.91}\text{As}$ to 502 Ω/\square for AlAs. These layers were then implanted with oxygen at multiple energies and doses of $2 \times 10^{14} \text{ cm}^{-2}$. The evolution of the resistance with post-implant annealing temperature is explained by damage-related compensation, and there is no evidence for a chemical interaction between Be and O.

SUMMARY AND DISCUSSION

There is no shortage of O-related deep levels in III-V semiconductors. Apart from the Be-O complexes and the O-related deep acceptor in n⁺AlGaAs described here, there are also the Zn-O radiative recombination centers found in GaP.^{15,40} The known reactivity of Be and O in their free states might lead one to suspect a strong pairing between them even in a semiconductor lattice. What is somewhat surprising is that the other acceptors, occupying the same sub-lattice as Be do not

show any evidence of an interaction with oxygen. There is clearly a need for a total energy calculation for the various acceptors in GaAs as an oxygen ion is placed in the vicinity of the acceptor, to try to explain this difference.

The fact that Be and O show a strong interaction implies that the Be is no longer as mobile after pairing with an oxygen ion, as in its unbound state. Evidence that this is actually the situation comes from the work of Humer-Hager and Zwicknagel,¹⁷⁾ who implanted oxygen into GaAs already implanted with Be, and saw not only a strong compensation effect on the tail of the Be distribution, but also a reduced tendency for redistribution of the Be.

In summary, we have demonstrated the creation of a deep donor level in oxygen-implanted, Be-doped GaAs. The presence of this level creates thermally stable, high-resistivity material. The simplest explanation is the formation of a Be-O nearest neighbor complex. Oxygen implanted into GaAs doped with the other acceptors Mg, Zn and Cd, or the donors Si and S, does not show any evidence for formation of stable dopant-oxygen complexes. Oxygen does not appear by itself to be electrically active in GaAs, forming a deep donor only when complexed with Be. In n-type AlGaAs, oxygen implantation and annealing creates high resistivity material by formation of a deep acceptor. In p-type material there is no apparent interaction of Be with O. This may be caused by competition for the oxygen by the Al in the AlGaAs.

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DEFECT HETEROJUNCTION MODEL FOR ANOMALOUS PHOTORESPONSE OF p/n GaAs GROWN ON n-Ge SUBSTRATES

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ABSTRACT

A GaAs p/n junction grown on a n-Ge substrate has an anomalous photoresponse that includes a quantum yield response starting at the 0.7-eV band edge of Ge. In terrestrial sunlight, its I-V characteristic has an anomalous "notched" shape that is progressively removed by increasing the infrared light content. The I-V is well modeled by a space charge-limited-current diode theory with a GaAs/Ge interface defect density of $1.92 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.4 eV below the conduction band edge. Similar defect densities have been reported for GaAs/oxide interfaces and for a GaAs p/n junction interface specially selected for high defect densities.

INTRODUCTION

GaAs p/n junction solar cells are now in large-scale production on Ge substrates with reported performance levels approaching those on GaAs substrates [1]. The motivation is to take advantage of Ge's higher mechanical strength compared to GaAs, which allows thinner substrates with reduced weight. Ge also offers the potential for growth on larger areas for higher yields and lower costs. Special steps keep the GaAs/Ge interface passive [1].

The more standard GaAs-on-Ge growth processes give devices with significantly higher operating voltages and potentially higher performance than the best GaAs-on-GaAs devices due to contributions from an active GaAs/Ge interface [2]. However, problems with "notched" current-voltage (I-V) characteristics in sunlight have so far reduced such devices' performance to less than that of GaAs-on-GaAs [3,4]. If this can be understood and controlled, substantially improved device performance may be possible.

Years ago, Sah et al. [5] discussed how defects can influence the rectifying I-V properties of semiconductor p/n junctions. More recently, a defect-controlled junction model has been developed for the case where defects overwhelm the effects of shallow donors and acceptors [6]. This has been extended to solar cells in general [7], and in particular to GaAs solar cells dominated by defects [8]. The model predicts solar cell response not only for p/n junctions, but also for isotype junctions like n/n interfaces. High densities of defects are expected at the hetero-interface of dissimilar materials because of mismatched properties.

DEFECT-CONTROLLED JUNCTION MODEL

The electron occupation of defect states in the bandgap of semiconductors changes as the quasi-Fermi level moves in response to stimuli like light exposure or applied voltage. When the net charge on these defects exceeds the net charge of the shallow donors and acceptors in a junction region, the electric field and charge transport are controlled by the changing charge on these defects. This condition is well described by space-charge-limited-current (SCL) expressions dominated by drift currents [6,9]. The I-V characteristics are obtained from Gauss and Ohm's laws using Fermi-Dirac statistics to describe defect occupation and Maxwell-Boltzmann statistics for the free carrier concentrations as specified by the quasi-Fermi level [6]. Rectification and photocurrent collection is produced by asymmetric boundary conditions for charge injection into and charge collection by the junction region [6,7].

EXPERIMENTAL RESULTS

The p/n GaAs was grown by OMVPE on a n-Ge substrate at 700°C using an arsine ambient during the preheat stage. The growth parameters and device processing were similar to those described by Bertness et al. [10]. Figure 1 shows the normally-shaped I-V characteristics of this device under an infrared-rich incandescent lamp. This gave an open circuit voltage (V_{oc}) of 1.18 V and a fill factor (FF) of 0.806, with the lamp intensity adjusted to give a short circuit current density (J_{sc}) of 30 mA/cm². The FF is a measure of the squareness of the I-V curve [11]. Figure 1 also shows the anomalous shape change in this characteristic when the light source was switched to a visible light-rich xenon lamp. Then a "notch" appeared that lowered the FF to 0.606 and the V_{oc} to 1.14 V with the lamp intensity adjusted for the same J_{sc} value. These V_{oc} values are 0.09 to 0.13 V higher than the V_{oc} values as high as 1.05 V reported for the best GaAs-on-GaAs cells [10].

Figure 2 plots the internal quantum yield spectra [11] measured on the GaAs-on-Ge device. To assure accuracy [12], the data below 1.4 eV were measured with chopped monochromatic light and a lock-in amplifier and with the device biased with constant visible-wavelength-rich light intense enough to induce a 0.4-mA/cm² dc current. Similarly, the data above 1.4 eV were measured under constant infrared-rich light intense enough to induce a 0.006 mA/cm² dc current. The bias is intended to turn on one junction so it will not current limit the other one being stimulated by monochromatic light that induces microampere-level currents [12]. Surprisingly, the data were unchanged when the dc bias lights were turned down or off. However, if they were turned up, the signals became too noisy to measure. The visible-wavelength-rich light was obtained by shining incandescent light through the filter shown in Fig. 3(A), and the infrared-rich light by shining incandescent light through the Fig. 3(B) filter.

Figure 2 shows the device has a weak response beginning at the 0.7-eV band edge of Ge, followed by a dead region and then by a standard GaAs p/n junction response starting at the 1.4-eV band edge of GaAs. Integrating this yield with known terrestrial sunlight spectra (air mass 1.5, or AM1.5) gives a calculated photocurrent of 0.8 mA/cm² for the Ge part of the curve and 26.1 mA/cm² for the GaAs part of the curve (normalized to 100 mW/cm² sunlight intensity). The latter current density is 65 to 4350 times greater than the bias current densities described above.

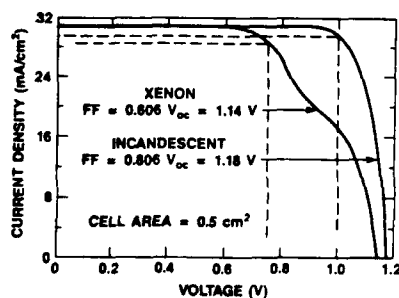


Fig. 1 I-V characteristics under xenon and incandescent lamps.

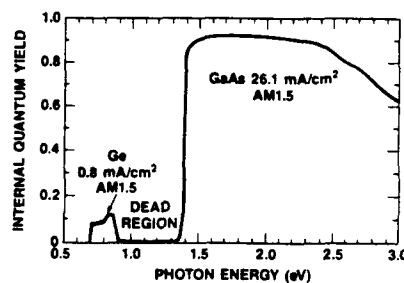


Fig. 2 Quantum yield spectra.

Because of the sensitivity to spectral content, the GaAs-on-Ge cell was measured in actual Palo Alto sunlight and plotted in Fig. 4. This shows the anomalous "notch" characteristic was maintained. Its efficiency was 18.0% with a V_{oc} of 1.05 V, a FF of 0.612, and a J_{sc} of 25.0 mA/cm² in 89.5 mW/cm² sunlight intensity. For control, the sunlight was collimated to only admit the direct radiation from the solar disk which was tilted at an angle corresponding to air mass 2.6 (AM2.6D). For comparison, the best GaAs-on-GaAs devices have much higher efficiencies of 24.0% and FF of 0.845 in terrestrial sunlight because no anomalous "notch" is present [10].

Doping profile information was obtained from the resistance measured between two microprobes stepped across the beveled edge of the GaAs-on-Ge sample as shown in Fig. 5. Sharp changes in this resistance clearly mark the 0.5- μ m thick p-GaAs layer, the 5-6 μ m thick n-GaAs layer, and finally the n-Ge substrate. For GaAs, this resistance is a contact resistance inversely proportional to doping concentration [13]. The minimum resistance of $10^5 \Omega$ in the GaAs corresponds to p-doping of $3(10^{18})$ cm⁻³. The n-GaAs was doped at $5(10^{17})$ cm⁻³, which should give a contact resistance of $\approx 2(10^8)$, which exceeds the $1(10^8) \Omega$ maximum of the ohmmeter which saturated this region. Over $\approx 0.3 \mu$ m, the transition is made from the n-GaAs to the n-Ge where the resistance then becomes a spreading resistance that is inversely related with and well calibrated to Ge doping levels [14]. The 2.5- μ m wide dip in resistance is due to As autodiffusing into the Ge during the GaAs growth, and the minimum resistance of 57.5Ω at the 7- μ m depth position corresponds to $5(10^{19})$ cm⁻³ n-doping. The $10^3 \Omega$ in the bulk of the Ge substrate corresponds to $1(10^{17})$ cm⁻³ n-doping.

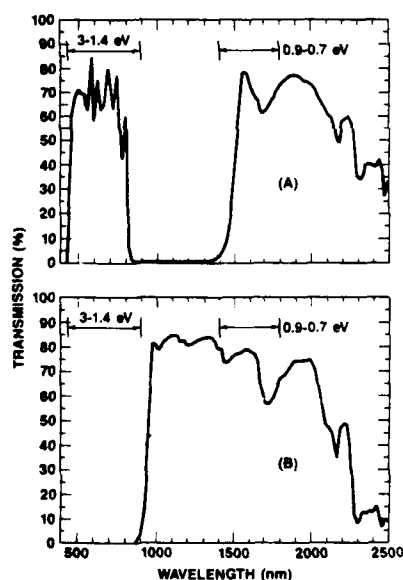


Fig. 3 Transmission spectra of the two filters.

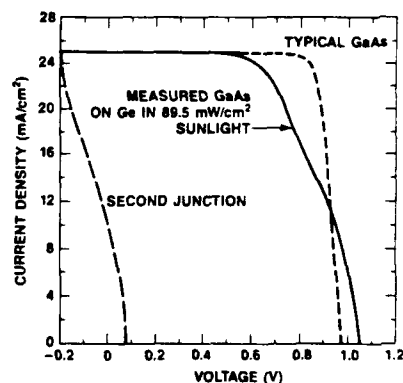


Fig. 4 Measured sunlight I-V characteristics (solid curve) and their decomposition into two tandem (broken line) curves.

DISCUSSION

A typical GaAs-on GaAs I-V characteristic is plotted in Fig. 4 as a broken line curve. Subtracting it from the measured data gives the I-V properties a second junction would need (as indicated by the second broken line curve) to explain the anomalous "notch" behavior. This typical GaAs data correspond to a 23.0% efficiency with a V_{oc} of 0.979 V, a FF of 0.841, and a J_{sc} of 25.0 mA/cm², while the second junction data correspond to an efficiency of 0.3% with a V_{oc} of 0.073 V, a FF of 0.355, and a J_{sc} of 10.8 mA/cm². Here we model the second junction as a n-GaAs/n-Ge isotype heterojunction (indicated by Fig. 5 data) with the Ge quantum yield response given on the left of Fig. 2.

The "dark" diode portion of the second junction's characteristic was obtained by subtracting its J_{sc} value of 10.8 mA/cm² from each data point, and by then plotting them on log-log scales as shown in Fig. 6. The fit of this forward and reverse bias data with the SCL diode model is given by the solid line curves. The details of this fitting process are given elsewhere [6,7]. The width of this n-GaAs/n-Ge isotype heterojunction was taken as 0.3 μ m and was assumed to lie mainly in the GaAs with an electron mobility of 2000 cm²/V-sec, a relative dielectric constant of 12.9, and an electron effective mass ratio of 0.067. A concentration gradient across this transition layer accounts for the equilibrium conduction band electron concentrations n_0 in this layer being slightly different for forward and reverse bias. A higher injection efficiency from the Ge side of the transition layer ($n(0)/n_0=10^6$) than from from the GaAs side ($n(0)/n_0=1.18$) accounts for the soft rectification and short circuit current collection. The $n(0)$ is the electron concentration boundary condition at the edge of the transition layer that is negatively biased. Fitting the shape of this data required a defect trap density of $6.41 \cdot 10^{16}$ cm⁻³ eV⁻¹ at 0.4 eV below the edge of the conduction band in the transition layer.

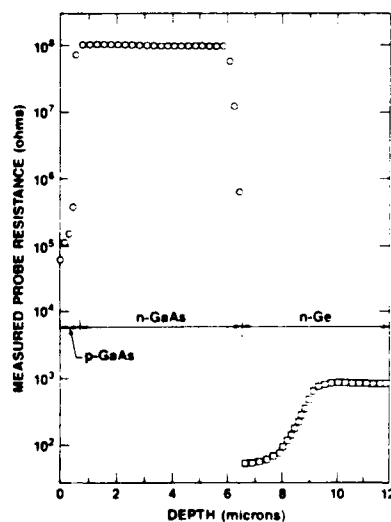


Fig. 5 Measured probe resistance profile.

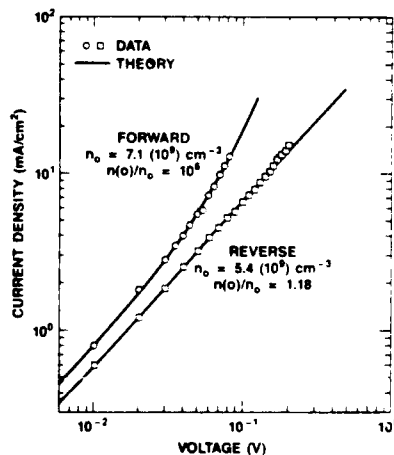


Fig. 6 Log-log plot of "dark" second junction I-V characteristics.

This volume trap concentration is shown by the datum point in Fig. 7. It can be compared to the literature by multiplying by the $0.3\text{-}\mu\text{m}$ width of the transition layer to convert it to a surface concentration of $1.92 (10^{12}) \text{ cm}^{-2} \text{ eV}^{-1}$ for the GaAs/Ge interface. This shows it in the same range of interface state densities reported for GaAs/oxide interfaces given by the three broken line curves at the top of the figure [15-17]. It is also in the range of most of the defects recently found in a GaAs p/n junction specially selected to have a high interface trap density [8]. For reference, the reported density of AlGaAs/GaAs interface states [18] is also shown to indicate that the GaAs/Ge interface does not have values as low.

If the isotype heterojunction model is accurate, increasing the relative infrared intensity of the light should continuously raise the second junction's J_{sc} , as well as the position of the notch, until it disappears at a sufficiently high infrared content (see Fig. 4). The measured data of Fig. 8 show this to be the case. The GaAs-on-Ge device was placed under two quartz-halogen lamps, where one lamp was shown through the Fig. 3(A) filter and the other through the Fig. 3(B) filter. With the intensity to the first lamp held constant to give J_{sc} of 30 mA/cm^2 , the relative infrared intensity (RIRI) from the second lamp was increased from 1.0 to 4.6 with a lens-iris attenuator, and the "notch" progressively disappears.

The measured $25.0 \text{ mA/cm}^2 J_{sc}$ in Fig. 4 compares well to the 23.4 mA/cm^2 value calculated from the Fig. 2 GaAs quantum yield data after adjusting for the different light intensities ($26.1 \times 89.5/100 = 23.4$) and allowing for the different spectral content of the AM1.5 and AM2.6D sunlight [19]. However, the 0.8 mA/cm^2 value calculated for the second junction from Fig. 2 is not comparable to the 10.8 mA/cm^2 attributed to the second junction in Fig. 4. Adjusting for the lower intensity ($89.5/100$) and correcting for the enhanced infrared content of AM2.6D compared to AM1.5 ($1.39/3.56$ [3]) only lowers the 10.8 down to 3.77 mA/cm^2 . This remaining factor of five disagreement is probably due to the intensity dependence of the second junction's quantum yield. Intensity-dependent quantum yields are well known in defect-filled solar cells like $\text{Cu}_x\text{S/CdS}$ [20], in contrast to well-behaved solar cells like GaAs whose quantum yields remain constant under bias light intensities well above 100 suns concentration [21].

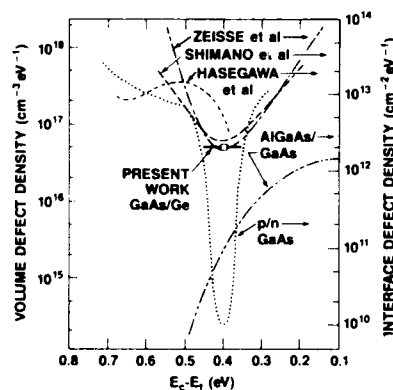


Fig. 7 GaAs/Ge defect density needed to fit "dark" I-V data with comparisons to literature values.

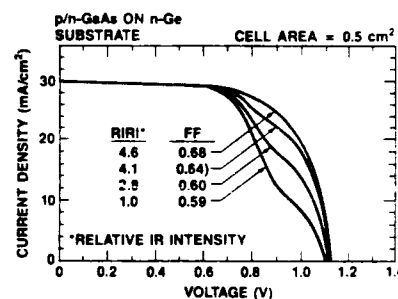


Fig. 8 Measured I-V characteristics with variable infrared light content.

Even $10.8 \text{ mA/cm}^2 J_{sc}$ performance is too low for tandem operation under GaAs with over $25 \text{ mA/cm}^2 J_{sc}$ levels. However, the GaAs-on-Ge devices measured by Hart et al. [4] indicate the second junction J_{sc} is 75% of the GaAs values and it has good V_{oc} and FF values. While this J_{sc} is still too low for two-junction operation, it would be sufficient for three-junction structures of AlGaAs/GaAs on top of the GaAs/Ge that only requires $\approx 16 \text{ mA/cm}^2 J_{sc}$ to give projected efficiencies exceeding 30% [22].

SUMMARY

A GaAs p/n junction grown on an n-Ge substrate shows an anomalous photoresponse that is sensitive to the spectral content of light. There is a "notch" in its sunlight I-V characteristics that can be progressively removed by increasing the infrared light content. The I-V data are well fit by a SCL diode model of the n-GaAs/n-Ge hetero-interface for an interface trap density of $1.92 (10^{12}) \text{ cm}^{-2} \text{ eV}^{-1}$ located 0.4-eV below the conduction band edge. This defect density is greater than that reported for AlGaAs/GaAs interfaces and is similar to that reported for GaAs/oxide interfaces and for a GaAs p/n junction interface chosen for high defect densities. The photocurrent from the n-GaAs/n-Ge junction is a factor of five higher than the measured quantum yield would indicate. The latter may be due to an intensity-dependent quantum yield like that reported for other defect-filled solar cell junctions. Understanding and control of the hetero-interface could provide improved device performance such as solar cells with efficiencies over 30%.

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CRYSTALLINITY OF ISOLATED SILICON EPITAXY (ISE)
SILICON-ON-INSULATOR LAYERS

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ABSTRACT

Isolated silicon epitaxy (ISE) is a proven method of producing single crystalline silicon-on-insulator (SOI) material with excellent electrical properties. The presence of the remaining isolated dislocation trails in the epitaxial silicon has led to this investigation of the crystallinity throughout the ISE SOI layer and across the isolated dislocations. The structural perfection of these layers has been examined by defect etching, Nomarski optical microscopy, electron channeling patterns, and with more sensitivity using double crystal synchrotron X-ray diffraction and topography. Defect etching reveals the dislocation density within the layers of production ISE SOI material to be $\sim 5 \times 10^5/\text{cm}^2$. Electron channeling pattern techniques have reached the resolution limit of angular orientation resolution for the isolated silicon layer. Finally, synchrotron studies have shown that orientation homogeneity across 5" wafers are preserved to 0.006° and the variation in orientation across the defect trails to be, in general, less than 10 arcsec (0.003°), indicating single crystalline ISE SOI production material.

INTRODUCTION

There is considerable interest in silicon-on-insulator material (SOI) owing to structural advantages for adiation hardened, high-voltage, high packing density, 3-dimensional circuitry, and high temperature applications[1-4]. Isolated silicon epitaxy (ISE) has been shown to be a leading process technology for producing SOI wafers[5-6] and is an attractive technology from a manufacturing point of view because of the potential for large scale, low cost production. Fundamentally, the process is a simple one, and the equipment required is relatively inexpensive.

ISE SOI has evolved from the technologies of Zone Melt Recrystallization (ZMR) and Lateral Epitaxy by Seeded Recrystallization of Si (LESS)[7-8]. In the ISE SOI process, a bulk silicon wafer is converted to an ISE SOI structure in the following way. The wafer is prepared by growing a thermal oxide upon which a thin polycrystalline silicon film is deposited. The structure is capped with SiO_2 deposited by chemical vapor deposition (CVD). The entire process is carried out in large wafer batches in commercial tube furnaces. Unlike ZMR, production ISE SOI has overcome material defect problems such as protrusions, high wafer warp, high micro-surface roughness, and waviness[9]. Values for these wafer characteristics are now comparable to bulk[10].

ISE SOI results in single crystalline Si material with isolated dislocation trails found along the growth direction as shown in Figure 1. The isolated dislocation trails are located $\sim 100\mu\text{m}$ apart from one another along [100] with defect free material in between. These remaining isolated defect trails result in a material defect density of $\sim 5 \times 10^5/\text{cm}^2$. The defect trails have an associated thickness variation of $< 80\text{\AA}$ when viewed along a 1.09° angle-lapped cross-section of the structure using Nomarski optical microscopy and confirmed using a stylus measurement technique. The

study of the material crystallinity across the isolated defect trails can be taken as a measurement of material quality. This study examines the crystallinity across the layer, paying particular attention to the structural perfection of the material across the defect trails. The latter has been examined through Schimmel etching and defect density measurements, SEM electron channeling patterns, and double crystal X-ray diffraction and topography using synchrotron radiation.

EXPERIMENTS AND RESULTS

The process of Schimmel etching and defect density measurements has been described in detail elsewhere[6,7]. For production ISE SOI, one 5" wafer per 25 wafer batch is Schimmel etched and examined for material crystallinity and defect density. The former is determined by the lack of grain boundaries or sub-grain boundaries in the material. The latter is evaluated through the examination and etch pit density count on $\sim 40,000 \mu\text{m}^2$ of material per wafer. While research material has lower defect densities, typical isolated defect trails on production ISE SOI material yield overall defect densities of $\sim 5 \times 10^3/\text{cm}^2$. Figure 1 shows one such trail as observed by SEM after Schimmel etch.

The electron channeling patterns (ECPs) were observed in a JSM 840 SEM (Scanning electron microscope) at an accelerating voltage of 15kV. Bulk Si, ZMR SOI, and ISE SOI material were examined for assessment of crystalline quality. The electron channeling patterns were taken from the surface of the crystals, so that the electron beam was perpendicular to the specimen. Over $500,000 \mu\text{m}$ of material were illuminated per pattern. The working distance was $\sim 10\text{mm}$. Figure 2 shows an ECP from bulk Si as compared with the ECPs of old ZMR SOI[11] and new ISE SOI. The figure also shows backscattered electron images of the ZMR SOI and ISE SOI surfaces. Any multigrains within the Si material appear in different contrast in the backscattered electron images produced by the SEM. These grains, in the ECPs, will produce superpositions in the patterns as is observed for the case of old ZMR material and marked in the micrograph with white arrows. No discontinuities in the ECP for bulk Si or ISE SOI Si were found, indicating a single crystalline material. The patterns, however, are very sensitive to small non-uniform lattice strains which can be detected to $\sim 0.1\%$ accuracy[12]. This approaches the accuracy of measuring the distances when a microphotometer is used. In particular, a close examination of enlarged ECP triangles formed by the intersection of the two higher order Laue zone $\{175\}$ lines and the zero-order Laue zone (660) -type line (marked triangle A in the ECPs) yields sensitive information on strains in the lattice parameter of the isolated silicon material as compared to the bulk sample. The height of the triangle and the longer side are extremely sensitive functions of the interplanar spacings. The value of observed asymmetry between the bulk and ISE SOI ECPs expressed as

$$\Delta H/d_{220} ,$$

where ΔH is the difference in heights of the triangles and d_{220} is the width of the prominent horizontal 220 band. This yielded a value of $\sim 0.7 \times 10^{-3}$. In comparison, a 2% strain in silicon yields a calculated value of 0.8×10^{-2} . The low level of strain in the film, reaching the detection limit of the SEM ECP technique prompted investigation of the film crystallinity by synchrotron radiation studies.

FIGURE 1: Schimmel etched ISE
SOI surface showing
remaining defect trails

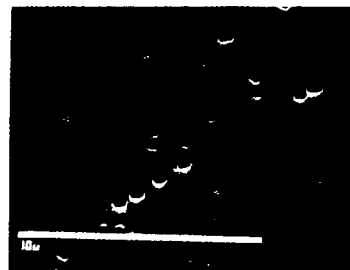
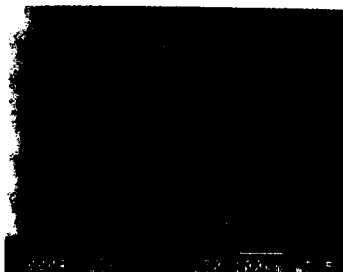
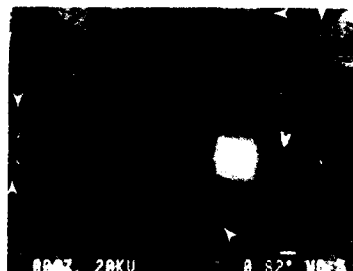
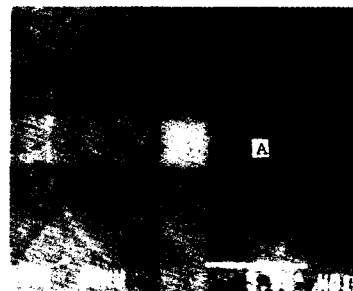


FIGURE 2: Electron channeling
pattern of (a) bulk Si as
compared with (b) ZMR SOI and
(c) ISE SOI material. Back-
scattered electron images of
(b) ZMR SOI and (c) ISE SOI
surfaces are also shown.



The crystalline orientation of the ISE SOI layer and across the defect trails was further examined by synchrotron radiation double crystal diffraction and topography. These experiments were performed at the white radiation topography station at the SRS, Daresbury UK. For the station, the topography image resolution limit depends on specimen-film distance (b), the resolution of the detector (d), and the geometry of the reflection[13]. The topography station has an exceptionally long columnnating length of $a=80\text{m}$ with a small source, $h=0.3\text{mm}$, giving an ultimate uncertainty and detection limit of orientation of 0.0002° [14]. Deviations of $50\mu\text{m}$ can easily be detected on an image (the resolution of the plates and films used was 0.5 to $2.0\mu\text{m}$), so that the choice of film-specimen distance of $b=300\text{mm}$ yielded an angular resolution of 0.01° . The spatial resolution of the technique (hb/a) is $1\mu\text{m}$.

Rocking curves and transmission topographic images were taken for a series of ISE SOI layers ranging from $0.75\mu\text{m}$ to $2.5\mu\text{m}$ thick[15]. Once a double crystal rocking curve is obtained for a particular wafer, a topograph from $\sim 5\text{arcsec}$ width of that curve may be obtained. With the SRS running at 2GeV and approximately 200mA , a 7 minute exposure time gave a good topographic image of the isolated silicon layer from which the orientation homogeneity could be obtained.

Figure 3 shows the double crystal x-ray diffraction obtained for a $0.75\mu\text{m}$ thick ISE SOI layer. Shown are two peaks which compare the substrate FWHM and the isolated layer FWHM. The latter is measured at 2° arcsec as compared to the bulk substrate which is measured at 9° arcsec. This corresponds to an overall layer orientation homogeneity of within 0.006° .

Confirmation that the orientation is preserved across the dislocation trails themselves was provided by double crystal X-ray topography. Figure 4 shows the topograph obtained from the peak position of the ISE SOI

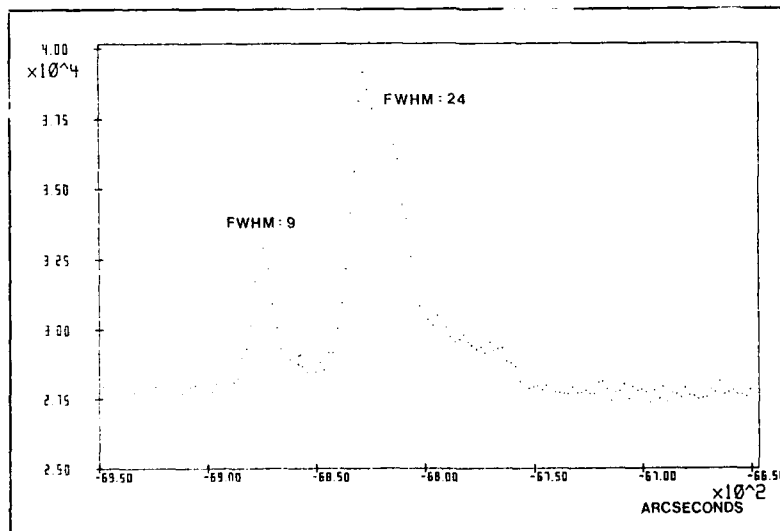


FIGURE 3: Double crystal x-ray diffraction of $0.75\mu\text{m}$ film

rocking curve shown in Figure 3. The symmetrical (+,-) setting is used. The white areas are Bragg contours and can be found to cross many dislocation trails. The latter can be clearly viewed in the image. The displacement across each trail is shown to be extremely small (0.003°) indicating no significant orientation change across the boundaries.

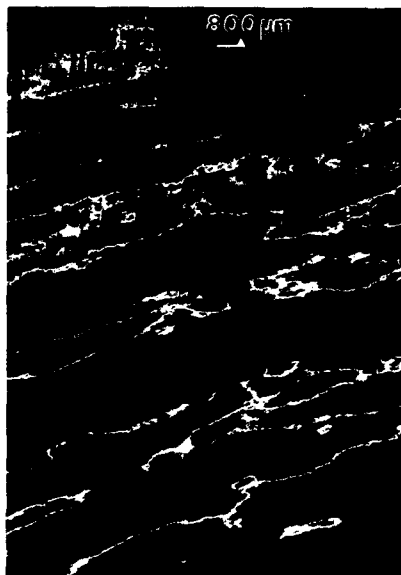


Figure 4: Double crystal x-ray topograph taken from rocking curve of ISE SOI layer (see Figure 3)

DISCUSSION and CONCLUSION

This study of ISE SOI material has examined the crystallinity of the isolated Si layer across 5" wafers as well as across the remaining defects. The resolution limit of electron channeling patterns to detect any orientation dispersion across the defect trails has been reached. In addition, double crystal x-ray diffraction shows the orientation within the isolated Si layer of the ISE SOI material to be within 0.006° . The iso-Bragg contours from the double crystal x-ray topography show the image of the dislocation trails and the continuity of the Bragg contours across them. The orientation across the isolated defect trails has been calculated to remain homogenous to 0.0027° . The layer is shown to be single crystalline. Future work will concentrate on the eradication of the remaining defects in ISE SOI material.

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CREATION OF INTERFACE STATES AT THE SILICON/SILICON DIOXIDE INTERFACE BY UV LIGHT WITHOUT HOLE TRAPPING

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ABSTRACT

Photoinjection of electrons into silicon dioxide in metal-oxide-semiconductor (MOS) capacitors with 3.5 eV light is shown to create interface states with no apparent hole trapping precursor. The creation rate of these interface states depends strongly upon whether injection is from the gate metal or the silicon substrate, and on the forming gas annealing sequence used to passivate growth-induced interface states. A mechanism involving electron-induced release of hydrogen in the oxide is consistent with some aspects of the data.

INTRODUCTION

Extremely defect free Si/SiO₂ interfaces are required for the operation of high efficiency concentrator solar cells of the "point contact" type [1]. In these devices most of the front and back cell surfaces are covered with thermally grown SiO₂ and carrier extraction occurs at small n⁺ and p⁺ "wells". Minority carrier recombination velocities less than 10 cm/sec at the passivated surfaces are necessary to maintain cell efficiencies above 25%. These low velocities are possible if the Si/SiO₂ interface state density is below $2 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$, a number attainable by careful post-growth anneals in hydrogen rich ambients. Recently, Gruenbaum et al. [2] demonstrated that the efficiency of point contact solar cells is degraded by exposure to ultraviolet (UV) light which has insufficient energy to create electron-hole pairs in the oxide or inject holes from the Si substrate. Concurrent increases in the surface recombination velocity implicated interface state build-up as the cause of the degradation. Hole trapping in the oxide is thought to be the normal precursor to radiation-induced interface states, and thus this degradation represents an "anomalous" interface state creation process. Pang et al. [3] and Mikawa et al. [4] have claimed that electron photoinjection into SiO₂ is capable of creating interface states, and it is possible that the UV exposures carried out by Gruenbaum et al. [2] could result in considerable photoinjection. In this paper we shall describe the results of experiments where electron photoinjection from both the Si substrate and various metal gates was performed on oxides processed with a variety of protocols. These data will be compared to prior results in an attempt to shed light on the physics of the interface state creation process.

EXPERIMENTAL DETAILS

The Si used for these experiments was [100] oriented, n-type, 0.8 to 1.2 $\Omega\text{-cm}$ material oxidized using rapid thermal processing techniques [5]. After a standard RCA clean [6], oxidation was carried out for 4 minutes at 1075°C, followed by an in-situ post-oxidation anneal (POA) in pure N₂ for 1 minute at 1150°C. Some of the samples had Al (15 nm) or Au (22.5 nm) front contacts evaporated immediately after the POA, followed by a post-metallization anneal at 450°C for 30 minutes in forming gas (FG). Other samples received the FG anneal before the gate metallization. Back contacts with negligible resistance were formed by using n⁺ implanted layers and evaporated Al metallization. Oxide thicknesses, charge densities, and interface state

spectra were obtained with a combination of high and low frequency capacitance-voltage (C-V) measurements [7]. Typical resolution of D_{it} (interface state density) was 2 to 4 $\times 10^9 \text{ eV}^{-1} \text{ cm}^{-2}$. Oxide thicknesses were 20 to 22 nm, with fixed charge densities less than $2 \times 10^{10} \text{ cm}^{-2}$ for the capacitors which had a FG anneal after gate metallization and 1 to 2 $\times 10^{11} \text{ cm}^{-2}$ for those annealed before gate deposition. D_{it} values were usually less than $2.5 \times 10^{10} \text{ eV}^{-1} \text{ cm}^{-2}$, and the normal "U-shaped" energy dependence of the interface state distribution was always observed in unirradiated capacitors.

An Ar ion laser operating with two major lines at 334 and 351 nm was used to irradiate the MOS capacitors through the semi-transparent metal gates. A glass filter with a hard cutoff wavelength of 300 nm insured that any weak, higher energy light from the laser discharge would not cause hole injection in our samples. Incident laser power densities of up to 0.1 watts/mm² could be used on the 0.6 mm² capacitors without significant sample heating. During injection the impressed oxide fields were 1 to 2 MV/cm, and the photon intensity and photocurrents were monitored continuously.

RESULTS

Figure 1 illustrates how the interface state distribution increases as a function of UV exposure when electrons are photoinjected from Al MOS capacitor gates (at negative gate bias). Initially the "U-shaped" curves rise rather uniformly at all energies. Eventually a broad maximum appears roughly centered around midgap in samples receiving the FG anneal before the gate metallization. Accompanying these increases were small but noticeable positive midgap voltage shifts (determined from the C-V curves), indicating some electron trapping in the oxide; this effect was also noted by Pang et al. [3]. A weak correspondence was observed between the amount of electron trapping and the magnitude of the D_{it} build-up.

Oxides which had a FG anneal before gate metal deposition show a larger D_{it} increase at equivalent injected electron fluence than those having the more conventional post-metallization anneal (PMA) protocol. The response difference between these two sample groups was quite repeatable. Because both types of samples showed similar photocurrents for the same incident photon flux, we cannot attribute this result to differences in this quantity. However, if direct photon absorption plays a role, we cannot rule out the possibility that the different FG anneal sequence might alter the sub-gap absorption coefficient of the oxide.

The electron fluence dependence of the increase in interface states for these two groups of samples is shown in Fig. 2. Pang et al. [3] report slopes much like those displayed by this data. One of their curves for gate injection at -1 MV/cm is shown in Fig. 2 (they plot total D_{it} integrated from -0.35 to +0.35 V, so that a direct comparison with our midgap values is inappropriate).

If photoinjection of electrons from the Si substrate (positive gate bias) is performed on similar MOS capacitors, no consistent difference is seen between the capacitors metallized before or after the FG anneal. This rather surprising result is shown in Fig. 3. In the case of substrate injection, the combined effects of lower UV intensity at the substrate and a smaller density of occupied electron states in the Si conduction band results in much lower injected electron fluences for equivalent incident photon fluxes. These lower fluences (typically a factor of 300) are reflected in the range of abscissa values in Fig. 3. Despite these lower fluences, the UV-induced interface state densities are quite similar to those in Fig. 2; thus, injection from the substrate is 2 to 3 decades more efficient in damaging the MOS capacitor. Pang et al. [3] claim to see no difference with gate bias polarity, although no substrate injection data is shown in reference [3], and a different light source was apparently used in this case [8]. At present we have no explanation for this disagreement.

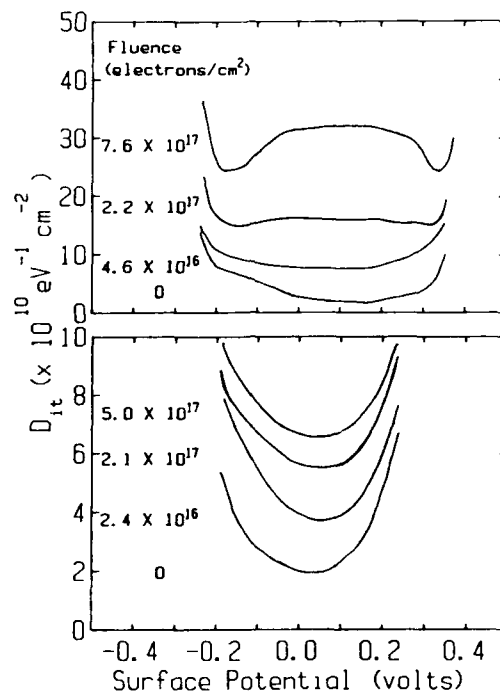


Figure 1. Interface state density versus surface potential for two n-type capacitors photoinjected at -1 MV/cm at various injected electron fluences. The upper data is for a device which had gate metal deposition after a FG anneal; the lower data is for a capacitor having a post deposition anneal. The oxide thickness was 21 nm and the capacitor area was 0.6 mm².

One surprising feature of the data in Figs. 2 and 3 was noted early along in this set of experiments. If the positive and negative gate polarity data for the capacitors metallized before the FG anneal is plotted versus photon fluence (not shown), the data are almost coincident. This observation was made before the other capacitors (metallized after the FG anneal) were fabricated. This coincidence suggested that photon flux, not injected electron fluence was the key parameter, and prompted us to try injection of capacitors with Au gates. Au has a 4.1 eV work function which means that exposure to our laser light with negative gate bias should produce a much smaller density of injected photoelectrons while maintaining roughly equivalent photon densities in the oxide. Data for gate injection into both Au and Al capacitors is shown in Fig. 4. Comparable laser exposure times were used to reach the largest fluences for each type of capacitor, and the photon intensity was actually 5 to 10 times larger at the Au/oxide interface due to the differences in optical constants of Au and Al. These data are consistent with electron fluence being the controlling parameter and

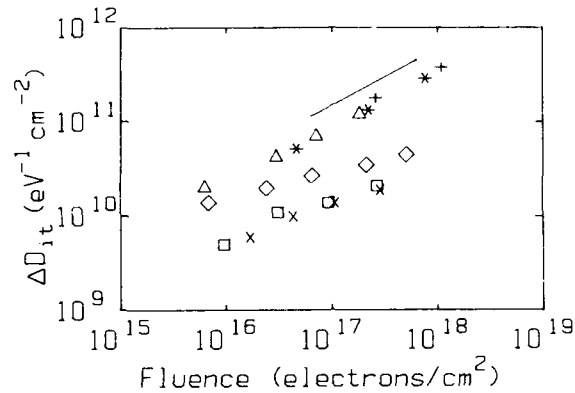


Figure 2. The change in midgap interface state density versus injected electron fluence for Al capacitors photoinjected at -1 MV/cm (gate injection). Δ , +, and * are data from capacitors having FG anneals before the gate metallization. \square , \diamond , and x are for capacitors having a post metallization anneal. The line is -1 MV/cm data of Pang et al. [3] (this is plotted as total interface state density integrated over the middle 0.7 eV of the Si bandgap).

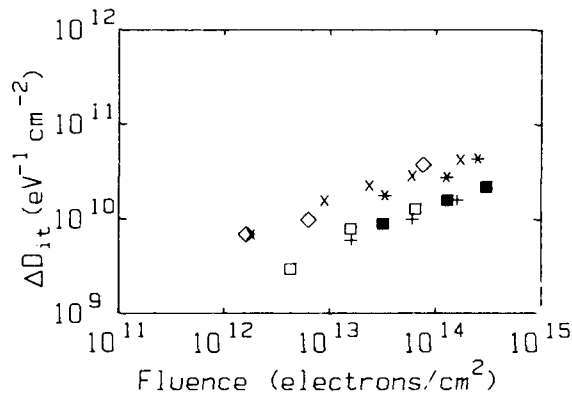


Figure 3. The change in midgap interface state density versus injected electron fluence for capacitors photoinjected at +1 MV/cm (substrate injection). + and * are data from Al capacitors having FG anneals before gate metallization; x, \diamond , and \square are for Al capacitors having a post-metallization anneal. \blacksquare are data from a Au capacitor FG annealed before metallization.

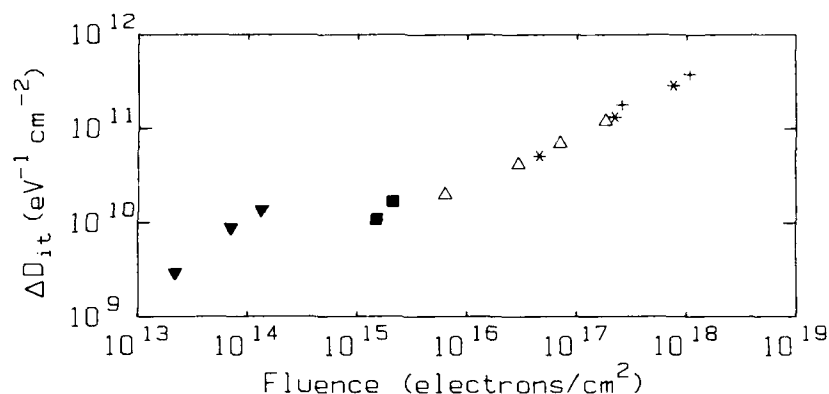


Figure 4. The change in midgap interface state density versus injected electron fluence for gate injection in Au and Al capacitors. *, +, and Δ are data from Al capacitors; ■ and ▼ are data from Au capacitors. All data here are for samples with FG anneals done before metal deposition.

would not fit on a single, metal-independent response curve if plotted versus photon fluence. For substrate injection, there is a similar coincidence of the Al and Au capacitor data on an injected fluence plot (Fig. 3). Note that for both bias polarities the voltage on the Au gate was adjusted (because of the work function difference) to produce the same 1 MV/cm oxide field present in the Al capacitors. We also note, as can be seen from examination of Figs. 2 to 4, that there was some scatter in the UV response of oxides grown in separate runs. One particular oxide growth run yielded capacitors which had almost no degradation at all for long laser exposures! At present, we have no explanation for this observation, but it clearly indicates that the degradation process involves electron-induced conversion of oxide defects or impurities.

The effects of several other parameters were examined during the course of these experiments. Fields were varied from 1 to 2 MV/cm for both substrate and gate injection, and Al gate samples were exposed to photon fluxes ranging from 0.03 to 0.1 watts/mm². The effects of changing either parameter did not exceed the typical capacitor to capacitor dot scatter on a D_{it} versus electron fluence plot. Because of its relevance to solar cell operation, we also made some measurements of the surface recombination velocity and carrier lifetimes in the near surface region of the Si using the Zerbst method [9]. These data showed a rapid rise of the recombination velocity with UV exposure but no detectable change in bulk lifetime.

DISCUSSION

In the measurements reported here and in the work of Pang et al. [3], care was taken to exclude photons energetic enough to inject holes into the oxide; in fact, in both these studies, no evidence for trapped positive charge was ever seen. It thus appears that trapped positive charge is not always the precursor for interface state production as required in the model recently proposed by Chang et al. [10]. Despite the apparent coincidence of

gate and substrate injection data at equal photon fluences for some of our Al capacitors, our experiments with Au gates suggest that electron injection, not just photon absorption alone, is required to see the creation of interface states. We should point out that our results to date cannot rule out the possibility of completely different mechanisms being operative in our various types of samples, but this seems unlikely. While Pang et al. [3] report that their data is relatively insensitive to oxide processing, our results indicate that the way in which the final hydrogen anneal of the interface is performed has a large effect on the UV sensitivity of our devices. Pang [8] reported a smaller enhancement (a factor of 2) for similar alterations in the FG anneal sequence. All of these observations may indicate that the amount and/or location of hydrogen in the oxide is crucial in the degradation process. For instance, electron initiated release of H followed by migration to the interface and H₂ creation at a Si-H bond could create an electrically active Si dangling bond.

While more experiments on MOS structures are clearly desirable to elucidate the physics of this process, attention must also be paid to duplicating the conditions experienced by actual solar cells where the oxide is electrically floating. Pang et al. [3] reported that the degradation is less for thinner oxides; the oxides described here are 2 to 3 times thinner than those of reference [3] and appear to show even less D_{it} buildup (Fig. 2). This may indicate that ultrathin passivating layers may be the key to controlling this effect.

ACKNOWLEDGEMENTS

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DEEP LEVEL TRANSIENT SPECTROSCOPY OF DEFECTS INDUCED BY THE COMBINATION OF CF_4 REACTIVE ION ETCHING AND OXIDATION IN METAL-OXIDE-SILICON CAPACITORS.

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ABSTRACT.

Metal-Oxide-silicon (MOS) capacitors have been fabricated on CF_4 reactive ion etched silicon (n and p types) in order to study the defects at the Si-SiO₂ interface and in the bulk of the substrate, produced by the combination of reactive ion etching (RIE) and oxidation. Bulk defects and fast interface states are analysed by Deep Level Transient Spectroscopy (DLTS) and the slow interface states in the oxide layer near the interface are probed by Tunnel-DLTS. A density of fast interface states in the range 10^{10} - 10^{11} cm⁻²eV⁻¹ is observed for capacitors (both n and p types) fabricated with either dry or wet oxidations, and is probably due to disrupted or strained bonds at the Si-SiO₂ interface. The observation of bulk defects in the wet-RIE oxide samples but not in the dry-RIE oxide samples may be related to the shorter oxidation time for wet oxides (31mn) compared to dry oxides (190mn) and explained by a greater annealing of RIE induced defects during the dry oxidation. The bulk traps are identified to be related to carbon contamination, in SiC form, introduced during RIE. Finally, an increase of the slow interface states density is observed for the n-type dry oxide samples.

INTRODUCTION.

Despite the progress made in earlier studies [1,2], a microscopic understanding of the defects produced by the combination of RIE and oxidation is still incomplete. A useful method for characterizing defects, both in Si and at the Si-SiO₂ interface is Deep Level Transient Spectroscopy (DLTS). Therefore, MOS capacitors fabricated on reactive ion etched silicon were characterized by DLTS, in an effort to identify the defects resulting from the oxidation of reactive ion etched silicon. It is shown that Si bulk defects, probably due to carbon contamination in SiC form, result after wet oxidation. A density of fast interface state in the range 10^{10} - 10^{11} cm⁻²eV⁻¹ result after either a wet or dry oxidation of reactive ion etched Si, probably due to disrupted or strained bonds at the Si-SiO₂ interface. It is proposed that the disrupted or strained bonds result from the implanted impurities and/or lattice defects from RIE, that accumulate at the interface during the oxidation process. The slow interface states in the strained layer of the SiO₂ near the interface are probed by Tunnel-DLTS [3], and it is shown that the slow state density increases more strongly than the fast interface state density after a dry oxidation.

EXPERIMENT.

Starting wafers were p and n type on <100>, 0.8-3.5 Ω.cm, Czochralski-grown Si substrates. MOS capacitors were fabricated on substrate with and without RIE. The CF_4 RIE was performed for 5mn in an asymmetric diode reactor made of stainless steel with a Si cathode and a perforated Al

anode. The total pressure, RF power (13.56 MHz) density, and DC self bias were 40 mTorr, 0.125 W/cm² and 280 V respectively. After RIE, a cleaning treatment effectively removes fluorocarbon films but does not remove implanted impurities or lattices defects that are deeper than 2 to 3 nm [4]. In particular, the RIE chamber used in the present study produces heavy metal contamination (nickel and iron) that is only partly removed by the cleaning treatment [5]. MOS capacitors were fabricated with either wet or dry oxidations. Wet oxides, 42 nm thick, were grown at 900°C for 31 mn. Dry oxides, 50 nm thick, were grown at 900°C for 190 mn. The furnace ambient contained 2% HCl during oxidation for both wet and dry oxides. Capacitors were metallized with evaporated Al and annealed at 400°C for 30 mn in an N₂/H₂ mixture.

MOS capacitors were first analysed by measuring the capacitance voltage (C-V) characteristics and the minority carrier generation lifetime. DLTS measurements were performed on 5 or 6 capacitors for each type of wafer. The temperature (T) was scanned from 100 to 250K which corresponds to an energy scan from 0.2 eV to 0.5 eV referenced to the band edges. An average value for the interface state capture cross-section of 10⁻¹⁶ cm² was used to calculate the energy distribution of the fast interface states from the DLTS temperature scan. The resolution of the fast interface state measurements is 2.5×10⁸ (250/T) cm⁻²eV⁻¹ and the error bars are 5%. The slow state density was measured at 150K by Tunnel-DLTS. The analysis of the filling kinetics of the slow states by tunnelling of electrons from the Si substrate is made from the time dependent behavior of the DLTS signal with an appropriate formalism [3].

FAST INTERFACE STATES.

For dry control oxides (p type Si), the interface states densities are low (10¹⁰ cm⁻²eV⁻¹) and vary little with energy (fig. 1). For dry-RIE

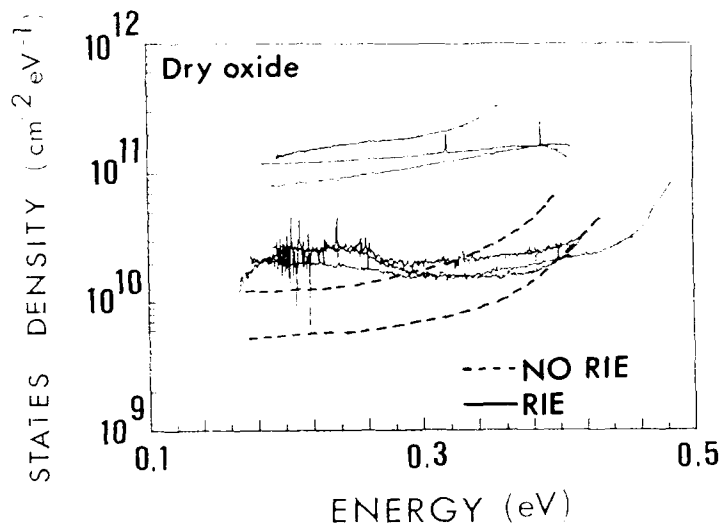


Fig. 1 Fast interface state density for dry-control (dashed lines) and dry-RIE (full lines) oxides measured by DLTS (p-type). Energy is referenced from the valence band edge.

oxides, two results are observed. For capacitors in one part of the wafer, the interface state density is increased by a factor of 10 at all energies, whereas for capacitors from a different part of the wafer, the interface state density increased by only a factor of 3 to 4 in an energy range from 0.2 to 0.35 eV. This indicates that the RIE process is nonuniform across the wafer. The results are rather similar for n type substrates. The interface state density is increased by a factor 2 to 5 (dry oxides).

Wet control oxides have a slightly higher interface state density (fig. 2) than the dry-control oxides. For wet-RIE oxides, the interface state densities are in the same range as for wet-control oxides but the shape of the energy distribution are different. The interface state density is relatively flat for wet-control oxides whereas it is U-shaped for wet-RIE oxides. In addition two bulk traps (BT1 and BT2) are superimposed on the interface state spectra (see next section).

For dry-RIE oxides, the peak in the interface state density at 0.20 to 0.35 eV is probably due to dangling bonds at the Si-SiO₂ interface which exhibit a positive to neutral charge state transition at this energy level [6]. Interestingly, dangling bonds are observed by Electron Spin Resonance (ESR) on Si surfaces after RIE [2]. The U-shaped distribution of fast states may be due to weak Si-Si or Si-O bonds at the interface [7]. The interface state density is generally higher for RIE oxides compared to the control oxides [1]. It was proposed that either fluorocarbon films, metallic contaminants, or lattice defects are responsible for the high interface state density [1]. The post-RIE cleaning treatment used in the present study effectively removes the fluorocarbon film but not the lattice defects or the implanted impurities (either metals or etch gas

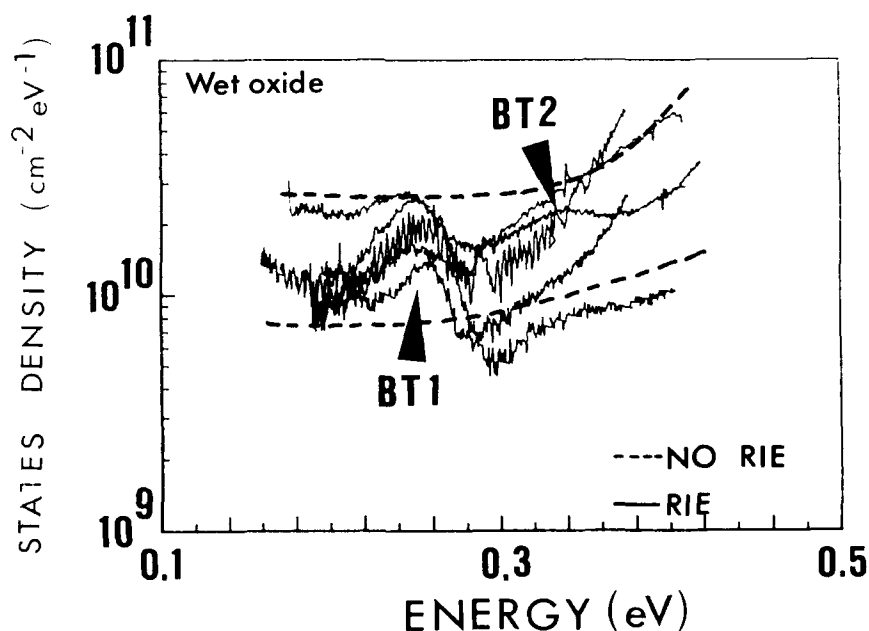


Fig. 2 Fast interface state densities for wet-control (dashed lines) and wet-RIE (full lines) oxides (p-type Si). Energy is referenced from the Si valence band edge.

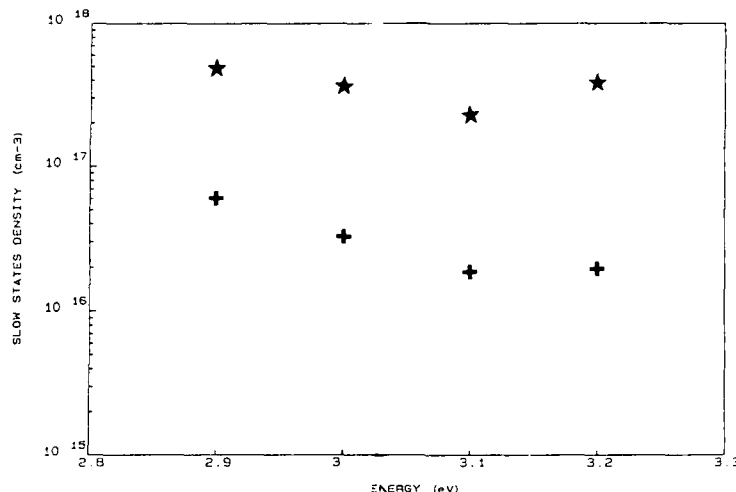


Fig. 3 Slow interface states in the strained SiO_2 layer at about 20 Å from the interface for dry-control (+) and dry-RIE (★) oxides (n-type Si) measured by Tunnel-DLTS.

species) [4,5]. Hence, lattice defects and/or implanted impurities, rather than fluorocarbon films, are responsible for the high state densities. Presumably, some lattice defects and/or implanted impurities accumulate at the Si-SiO₂ interface during oxidation. Their presence at the resulting interface is expected to increase the number of disrupted bonds, leading to a high interface state density.

SLOW INTERFACE STATES.

We have analysed the behavior of the slow states localized in the strained SiO₂ layer at about 20 Å from the interface and in front of the Si conduction band (from 2.9 to 3.2 eV below the SiO₂ conduction band edge) [3]. These near interfacial oxide traps interact with the free carriers of the substrate by tunneling, and can be also characterized by DLTS. Fig. 3 show the energy distribution of the slow states for the dry-control oxides and the dry-RIE oxides (n-type substrate). The energy profile is rather flat and the slow state density is increased by a factor of about 10 after the RIE treatment. This increase is 2 to 4 times greater than the fast interface states (fig. 2). This is explained by impurities and/or lattice defects incorporated in the surface layer of the silicon substrate during the RIE diffusing into the SiO₂ during the oxidation. We also notice that the defects introduced by RIE are concentrated in the consumed Si layer during the oxidation and therefore are preferentially incorporated in the oxide during the oxidation process. In the present case, the total charge in the oxide determined from the shift of the C-V characteristics is not changed significantly after the RIE, and the drastic decrease of the breakdown field (4.3 MV/cm for the RIE oxides compared to 11 MV/cm for the control oxides) can be associated with the important increase of the slow state density.

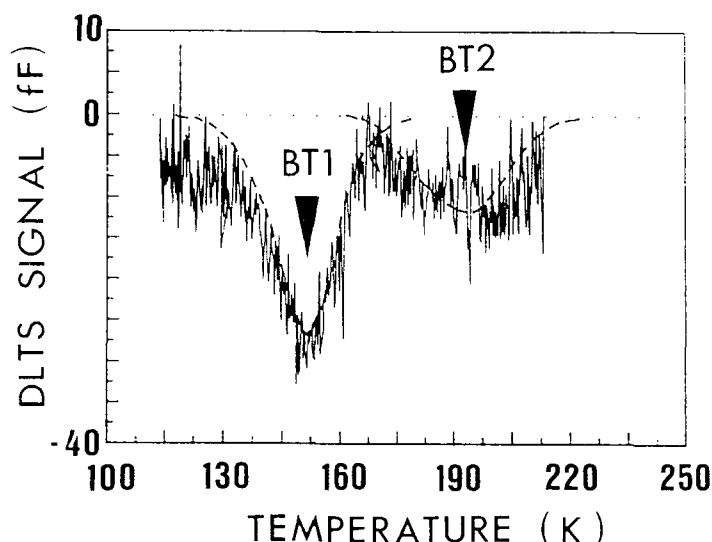


Fig. 4 Deep depletion mode DLTS spectrum for the bulk traps in the wet-RIE oxides (p-type Si). Only bulk traps contribute to the DLTS signal.

SILICON BULK TRAPS.

For the wet-RIE oxides (p-type substrate) there are two bulk traps BT1 and BT2 (fig. 4). Signals from these traps are detected even using deep depletion mode DLTS, indicating they are bulk Si hole traps rather than interface states. The activation energies are 0.23 eV and 0.29 eV respectively for BT1 and BT2. Depth profile measurements [8] indicate that they are present up to 0.7 μm in the Si.

These two hole traps were not detected in a previous DLTS work on RIE damage in Si [9]. In general, CF_4 RIE introduces point defects and implants carbon into Si [10]. In addition, for the reactor used in this study, nickel and iron from the stainless steel walls or the low purity Al anode are inadvertently sputtered into the wafers. Numerous hole traps have been observed in Si intentionally contaminated with nickel or iron [11]. However, from a careful study of the literature, we conclude that the 0.21 and 0.29 eV levels observed in this study do not correspond to nickel and iron impurities [12]. It is assumed that iron and nickel observed by SIMS in our samples have precipitated at stacking faults and are not electrically active [5]. Stacking faults are in fact observed by etch pit delineation in our samples with wet-RIE oxides.

Carbon is the only impurity or defect that is expected to be present in the wet-RIE oxides samples, and that produces hole traps with energy levels similar to those of BT1 and BT2. In particular a close correlation is found with the work of Endrös et al. [13]. They have observed hole traps at 0.22 and 0.29 eV in Si contaminated with carbon in SiC form and annealed at 870°C for 30 mn. The observation of similar traps in wet-RIE oxides but not in dry-RIE oxides may be related to the shorter oxidation time for wet oxides compared to dry oxides. Endrös et al. observed

that the traps were absent after long annealing times at 870 °C. Thus our results are correctly explained by the increased annealing of RIE induced defects during the dry oxidation. The presence of Si bulk traps in wet-RIE oxides may be partly correlated with the low generation lifetimes observed in these MOS capacitors [12]. However, the stacking faults that are also present in these samples are probably the main cause of the low generation lifetime [5].

SUMMARY AND CONCLUSIONS.

MOS capacitors have been fabricated on CF_4 reactive ion etched Si in order to study defects at the Si-SiO₂ interface and in the bulk of the Si substrate, produced by the combination of RIE and oxidation. A density of fast interface state in the range 10^{10} - $10^{11}\text{cm}^{-2}\text{eV}^{-1}$ is observed for capacitors fabricated with either dry or wet oxidations, and is probably due to implanted impurities and/or lattice damage. The density of slow interface states, localized in the strained layer of the SiO₂ near the interface, is more strongly increased by the RIE treatment than the fast state density. Capacitors fabricated with a wet oxidation on CF_4 etched Si contain bulk traps in the Si, which may be partly responsible for the low minority carrier lifetimes observed for these samples. These bulk traps are probably related to carbon contamination, under SiC form, introduced during RIE.

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Molecular Beam Epitaxy on the $(\text{NH}_4)_2\text{S}_x$ -Treated Surface of GaAs

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Abstract

We have found that treatment with a solution of ammonium sulfide containing excess sulfur $[(\text{NH}_4)_2\text{S}_x]$ produced a stabilized surface of GaAs. The treated surface is covered with a monomolecular layer of sulfur, and oxygen atoms are prohibited from adsorbing chemically on this surface. We checked the durability of the treated surface to heat treatment to find that it was stable up to more than 500 °C. Epitaxial growth of an Al film was demonstrated on the $(\text{NH}_4)_2\text{S}_x$ -treated surface. The presence of sulfur atoms at the interface by this treatment was found to suppress the chemical reaction between the metal and GaAs. Low temperature GaAs epitaxy was demonstrated on the sulfide treated surface without conventional heat treatment. The surface treatment correlates with changes in Schottky barrier height with various metals, which suggests that the surface states of GaAs are decreased remarkably.

§ 1. Introduction

Recently, sulfide treatments have been reported to be effective in the surface passivation of GaAs [1]. Among them, we have found that the $(\text{NH}_4)_2\text{S}_x$ treatment produced a well stabilized GaAs surface which was formed by two processes; (i) removal of the native oxide and (ii) passivation and protection of the surface by a monomolecular sulfur layer [2-6]. Here, we investigate the interface behavior which dramatically affects the epitaxial and electronic properties of GaAs. First, the epitaxial growth of Al on the $(\text{NH}_4)_2\text{S}_x$ -treated GaAs was compared with that on the as-etched GaAs. One monolayer of sulfur on GaAs prevents the surface from oxidation. Secondly, it was demonstrated that GaAs grew epitaxially directly on the sulfide-treated surface without the conventional heat treatment. Finally, it was shown that the sulfur layer passivated the GaAs surface and released the Fermi-level pinning.

§ 2. Experimental

The investigation was mainly performed on the (100) surfaces of GaAs. The specimens were fabricated from a HB crystal with an electron concentration of $1 \times 10^{18} \text{ cm}^{-3}$. The wafer was etched in a $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (3:2:45) solution at 40 °C for 1 min, and then rinsed in deionized (DI) water. The etched sample was dipped into an aqueous solution of $(\text{NH}_4)_2\text{S}_x$ (so-called "ammonium sulfide, yellow", $x \sim 2$, containing 8~9 % NH_3 and about the same percentage of sulfur) at 60 °C for 2 h. After a blown-dry process, the sample was loaded in a vacuum chamber. In the following, "as-etched" means the treatment of the etching and rinsing in DI water, and "as-treated" corresponds to the sulfide treatment following the etching process.

Deposition of Al was done after reducing the background pressure in the low 10^{-10} Torr range by extensive liquid nitrogen cooling, in order to avoid possible contamination during the deposition. The growth is monitored by reflection

high-energy electron diffraction (RHEED). After deposition and RHEED observation, the sample was studied by Auger electron spectroscopy (AES) and x-ray diffraction. The Al metal was deposited at the rate of $0.2 \mu\text{m/h}$ at room temperature (RT).

The epitaxy of GaAs on the as-treated surface was performed by migration-enhanced epitaxy (MEE) techniques [7], where the Ga and As shutters are opened alternately and the GaAs layer was grown at about 350°C at the rate of 3000 \AA/h .

The evaluation of surface properties was performed by current-voltage (I-V) and capacitance-voltage (C-V) measurements of the Schottky barrier height (SBH) and C-V measurement on MIS structures for interface state density.

§ 3. Results and Discussions

3.1 Epitaxy of Al on $(\text{NH}_4)_2\text{S}_x$ -treated GaAs

Figure 1 shows the changes in RHEED patterns along the [011] azimuth by deposition of Al at RT, on (100) GaAs surfaces which were prepared with two different treatments. For the first group, (a), (b) and (c), Al was deposited on the as-etched GaAs and for the second group, (d), (e) and (f), Al was deposited on the $(\text{NH}_4)_2\text{S}_x$ -treated surface. The RHEED pattern with no metal deposition for the as-etched surface (Fig.1(a)) indicates a spotty x1 structure due to the presence of oxide on the surface, while that for the as-treated surface (Fig.1(d)) becomes a streaky x2 structure by heating at about 350°C . This phenomenon on the $(\text{NH}_4)_2\text{S}_x$ -treated surface is caused by (i) an etching effect of oxide and GaAs and (ii) surface reconstruction involving sulfur atoms. After deposition of Al, the patterns on the as-etched surfaces are always concentric circles, indicating a polycrystalline film of Al. On the as-treated GaAs, however, the RHEED pattern for Al of 20 Å (Fig.1(e)) exhibits diffuse spots, typical of three-dimensional (3D) Al (110) epitaxial growth with

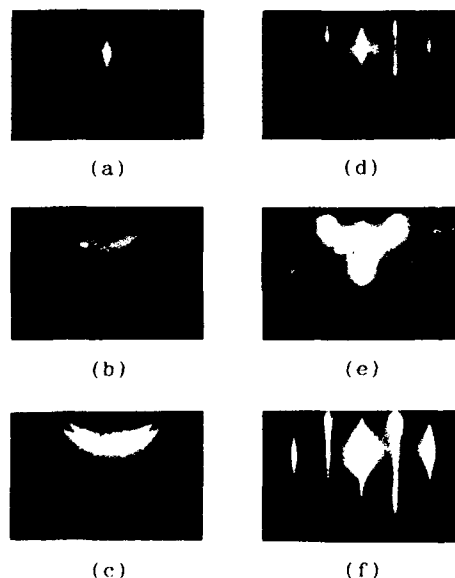


Fig.1. RHEED patterns along [011] GaAs azimuth on the (100) surfaces: (a)-(c) as-etched and (d)-(f) as-treated. The thicknesses of deposited Al film were (a) and (d) 0 Å (no metal deposition), (b) and (e) 20 Å, and (c) and (f) 2000 Å.

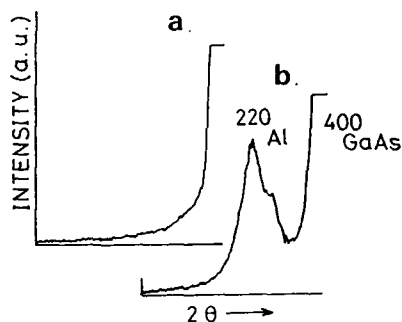


Fig.2. X-ray diffraction profiles of deposited Al film (2000 Å) on the (a) as-etched and (b) as-treated GaAs using a non-monochromatic Cu K source.

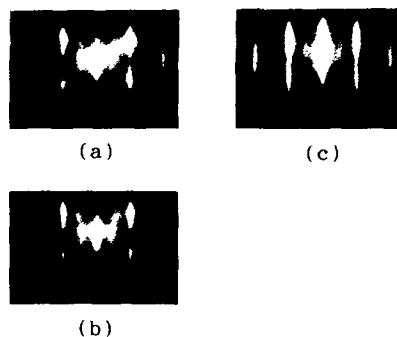


Fig.3. RHEED patterns along the $[011]$ azimuth on the $(\text{NH}_4)_2\text{S}_x$ -treated (100) GaAs surface during the successive heat treatments at (a) 350, (b) 580 and (c) 650 °C.

an orientation $[001]\text{Al}/[0\bar{1}1]\text{GaAs}$. With increasing Al coverage (Fig.1.(f)), the pattern of Al (110) is observed to change from spotty (3D growth) to streaky (2D). X-ray diffraction experiments were performed to study the crystalline quality of the Al film, as shown in Fig.2. Figure 2 presents the x-ray diffraction profile of 2000 Å of Al film deposited on the (a) as-etched and (b) as-treated surface. The Al (220) lines composed of both $\text{Cu } K\alpha_1$ and $K\alpha_2$ are observed on the as-treated GaAs, implying an establishment of good crystalline quality of the Al film, while no diffraction pattern was observed on the as-etched surface.

In order to study chemical reactions at the Al and GaAs interface treated with $(\text{NH}_4)_2\text{S}_x$, we investigated the AES spectra after the deposition of 20 Å of Al on the as-treated substrate and the as-grown surface which was prepared by MBE just before Al deposition. When those samples were exposed to air, the oxidation of Ga atoms on the as-grown surface was induced via the oxidation of Al metal, since the GaAs surfaces were covered with Al completely. In contrast to the as-grown surface, there is no evidence of oxidation of Ga atoms on the as-treated surface, which indicates that on the as-treated surface, the oxidation of Ga was effectively suppressed by the presence of sulfur at the interface.

3.2 Epitaxial Growth of GaAs

We attempted the regrowth of GaAs on the as-treated GaAs (100) substrate by MEE. The structures on the as-treated surface during the successive heat treatments are shown in Fig.3. Figure 3 (a), (b) and (c) show the RHEED patterns along the $[011]$ azimuth after heating with As_4 flux at 350, 580 and 650 °C, respectively. The (2x1) pattern in Fig.3 (a) remains unchanged up to 520 °C as well as the coverage ratio of sulfur atoms [4]. At 580 °C the sulfur atoms begin to desorb, and the complex pattern which is probably related to both sulfur and arsenic atoms at the surface appears. When the sample was heated at 650 °C corresponding to the temperature for thermal cleaning of GaAs,

the [011] pattern turns to the usual 2x structure of GaAs.

MEE technique was employed for low temperature epitaxial growth of GaAs. In this epitaxial process, the substrate temperature did not exceed 350 °C including the surface cleaning process. The RHEED pattern shows that 3D-like growth occurs initially, but the GaAs islands eventually coalesce to form a continuous layer with a (2x4) surface structure. This behavior might be due to the lattice mismatch between GaAs and S on GaAs.

3.3 Reduction of Fermi-level Pinning

The SBH of Al/n-GaAs (100) of the as-etched surface is 0.77 eV, while that of the as-treated surface is 0.45 eV which is approaching the calculated value assuming no pinning traps. According to the unified defect model, this change in electric properties is attributable to the difference of the number of defects in GaAs which is generated by the adsorption of foreign atoms [8]. This means that the sulfur-terminated surface by the $(\text{NH}_4)_2\text{S}_x$ treatment suppresses the creation of defects in GaAs [9]. Figure 4 (a) and (b) shows the experimental results of SBH for n-GaAs and p-GaAs, respectively. Open and solid circles are for the $(\text{NH}_4)_2\text{S}_x$ -treated and as-etched samples, respectively. The ideality factor (or n-value) was less than 1.1 for all n-type specimens. Apparently, for both n- and p-type GaAs the dependence of SBH on the work function of metals on the as-treated surfaces is larger than that on the as-etched surfaces. The interface state density was reduced from 10^{14} to 10^{13} cm^{-2} by this treatment [3]. Concerning the thermal stability of Schottky contacts, as-treated samples were almost the same as as-etched. For example, the SBH for Al and Au metals degrades at 450 and 200 °C, respectively.

It should be pointed out that the etching effect of GaAs by $(\text{NH}_4)_2\text{S}_x$ solution plays an important role for realizing the lower interface state density. The $(\text{NH}_4)_2\text{S}_x$ solution can etch the (100) GaAs surfaces at the rate of 80 Å/h at 60 °C, while $(\text{NH}_4)_2\text{S}$ can not. The difference in etching rate of GaAs can be the reason for the difference between 0.45 and 0.60 eV in the SBH for Al contacts on the respective $(\text{NH}_4)_2\text{S}_x$ - and $(\text{NH}_4)_2\text{S}$ -

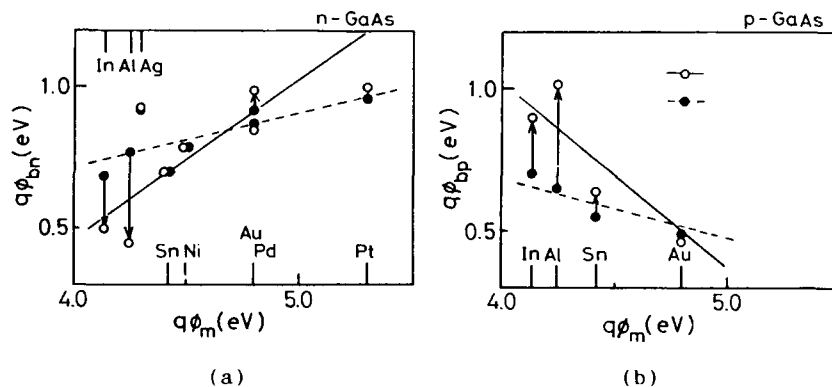


Fig.4. Dependence of SBH on the work function of metals on the (100) GaAs surfaces: (a) n-type and (b) p-type substrates. ○ and ● correspond to the SBH on the as-treated and as-etched samples, respectively.

treated n-GaAs, since both solutions provide the same oxygen-free and sulfur-passivated surfaces of GaAs. We also observed the dependence of SBH on the orientations of GaAs, which may be attributable to a difference in the etching rate. Table I shows SBH for Al/n-GaAs with (100), (111)A, (111)B and (110) planes; (a) as-etched and (b) $(\text{NH}_4)_2\text{S}_x$ -treated. The amount of change in the SBH between (a) and (b) apparently depends on the etching rate of GaAs. The SBH on the (100) and (110) are decreased by 0.3 eV with the sulfide treatment, while those on the (111)A and (111)B are decreased by 0.15 eV. This may be attributable to the fact that the etching rates on (100) and (110) are much larger than that on (111)A and (111)B.

Figure 5 shows C-V characteristics of metal-insulator-semiconductor (MIS) structure fabricated by an electron beam deposition of SiO_2 on the $(\text{NH}_4)_2\text{S}_x$ -treated surface of n-GaAs. Curve (a) and (b) were measured at quasi-static condition and 1 MHz, respectively. The interface state density N_{ss} was estimated to be $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at the main pinning levels near 0.6 eV below the conduction band minimum, from 1 MHz C-V characteristics by Terman's method [2]. This value is in a fair agreement with that derived from measurement of SBH. Significantly, MIS

Table I. Difference of SBH for Al/n-GaAs with the orientations of (100), (111)A, (111)B and (110).

orientation	as-etched $\phi_{\text{bn}}(\text{eV})$	$(\text{NH}_4)_2\text{S}_x$ -treated $\phi_{\text{bn}}(\text{eV})$	etching rate of GaAs at RT by $(\text{NH}_4)_2\text{S}_x$ (A/h)
(100)	0.77	0.45	7
(111)A	0.84	0.69	---
(111)B	0.72	0.59	---
(110)	0.77	0.49	2

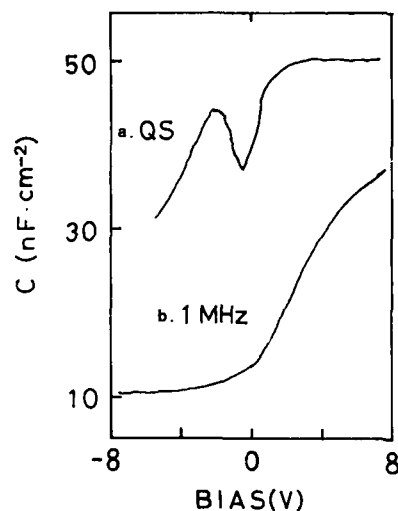


Fig.5. C-V plots of the MIS structure fabricated on the $(\text{NH}_4)_2\text{S}_x$ -treated (100) GaAs surface. Curves (a) and (b) were measured at RT for quasi-static mode and 1 MHz, respectively.

C-V curve at quasi-static mode clearly shows the formation of an inversion layer of holes.

§ 4. Summary

Epitaxial growth of an Al film was observed on the $(\text{NH}_4)_2\text{S}_x$ -treated surface without thermal treatment. The low temperature growth of GaAs on the as-treated surface was performed by MEE technique. In this process, the substrate temperature did not exceed 350 °C including the surface cleaning process. The SBH of Al contacts on the treated surface is smaller than that on the as-etched surface. It is considered that the sulfur layer on the as-treated surface hinders the chemical reaction between Al atoms and GaAs. This interfacial behavior should suppress the creation of defects at the interface. This is supported by the fact that the SBH on the $(\text{NH}_4)_2\text{S}_x$ -treated surface is strongly dependent on the work function of deposited metals, indicating the unpinning of the surface Fermi level. Furthermore, we demonstrated excellent properties in the MIS C-V characteristics by this treatment; that is, formation of an inversion layer of holes. It was also revealed that the difference in SBH between $(\text{NH}_4)_2\text{S}_x$ and $(\text{NH}_4)_2\text{S}$ treatments was due to the difference of etching rate of GaAs.

Acknowledgments

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DX CENTER IN GaAs-GaAlAs SUPERLATTICES SUPPRESSION AND IDENTIFICATION

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ABSTRACT

The DX center has been studied by Deep Level Transient Spectroscopy in series of GaAs-Ga_{1-x}Al_xAs ($x = 0.3$) and GaAs-AlAs short period superlattices. The existence or not of this center can be understood if its energy level is linked to the L miniband. This suggests a possible way to suppress them by using specific superlattices.

I. INTRODUCTION

When a localized state associated with a defect is placed in a well or a barrier of a heterostructure, its electronic structure is not perturbed as long as the extension in space of the associated wave function is small compared to the well or barrier width [1]. As a result, the defect energy level E_T remains linked to the band structure of the material which composes the well or the barrier. Thus, in a periodic heterostructure in which electrons are delocalized, i.e. when the original band structure is replaced by a series of superlattice minibands, electron emission from the localized level occurs [1] into the bottom of the first miniband with an activation energy SE_T such that (see fig. 1) :

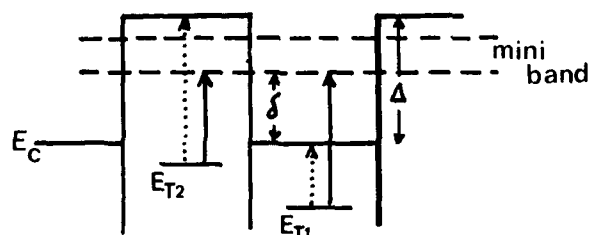


Fig. 1 - Change of emission rate for a defect of level E_T placed in the well (1) or in the barrier (2) of a superlattice (solid arrows) as compared to the case of bulk material (dotted arrows).

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$$SE_{T1} = E_{T1} + \delta \quad (1)$$

(where δ is the position of the first miniband above the bottom of the conduction band of the well) when the defect lies in a well; or when the defect lies in a barrier

$$SE_{T2} = E_{T2} - \Delta + \delta \quad (2)$$

(where Δ is the conduction band offset).

The aim of this communication is to understand the behavior of the DX center in superlattices in the light of these simple considerations. DX centers are introduced by doping $Ga_{1-x}Al_xAs$ barriers of GaAs-GaAlAs superlattices with a n-type dopant when the alloy composition x is larger than ~ 0.20 (for a review on DX centers see ref. [2]). In principle, DX centers can be detected in a superlattice using Deep Level Transient Spectroscopy in an homogeneous material when the electric field is applied perpendicular to the growth direction [3]. We shall see that this study provides a way to suppress DX centers, whose presence is often detrimental for device behavior. Moreover, such study brings some fundamental information on the nature of this type of defect.

II. SAMPLE DESCRIPTION

The heterostructures used in this study are short period GaAs- $Ga_{1-x}Al_xAs$ superlattices with $x = 0.3$ and 1. The ratios of the well to barrier widths for the GaAs-AlAs are chosen so that the average value of the alloy composition is close to $\bar{x} = 0.3$. The following well-barrier widths have been studied : i) 20 - 20 Å, 30 - 30 Å, 40 - 40 Å, 40 - 20 Å and 50 - 50 Å for the GaAs-GaAlAs superlattices; ii) 45 - 12 Å and 35 - 17 Å for the GaAs-AlAs superlattices. They are grown by molecular beam epitaxy on n^+ Si doped buffers over n^+ substrates and uniformly doped at a few times 10^{16} cm^{-3} with Si. The thickness is of the order of 1 - 2 μm . The top layer is a GaAs layer. In the case of the GaAs-AlAs superlattices a 100 Å thick GaAs layer having the same doping is used as encapsulant.

Capacitance-voltage measurements performed on Schottky barriers deposited by gold or Al evaporation on top of the layers show that all these structures behave as if they were homogeneously doped with a free electron concentration of the order of the doping concentration adjusted during the growth [3].

The GaAs-GaAlAs ($x = 0.3$) superlattices have a first miniband which is located at values of $\delta = 128, 113, 96, 74$ and 79 meV above the Γ conduction bands of the GaAs wells for the 20 - 20, 30 - 30, 40 - 40, 40 - 20 and 50 - 50 Å structures, respectively. These values, as well as the band offset $\Delta = 280 \text{ meV}$ used to calculate them, have been experimentally verified using electron irradiation induced defects as probes [4]. As to the GaAs-AlAs superlattices, the electronic structure is more complicated since the bottoms of the GaAs and AlAs conduction bands have a different character. As shown in figure 2 the first miniband, labelled Γ_m , has a Γ character while the second one, L_m , has an L character. Their energy positions, relative to the Γ and X conduction bands of GaAs and AlAs, calculated using a widely accepted value $\Delta = 180 \text{ meV}$, are indicated in the figure.

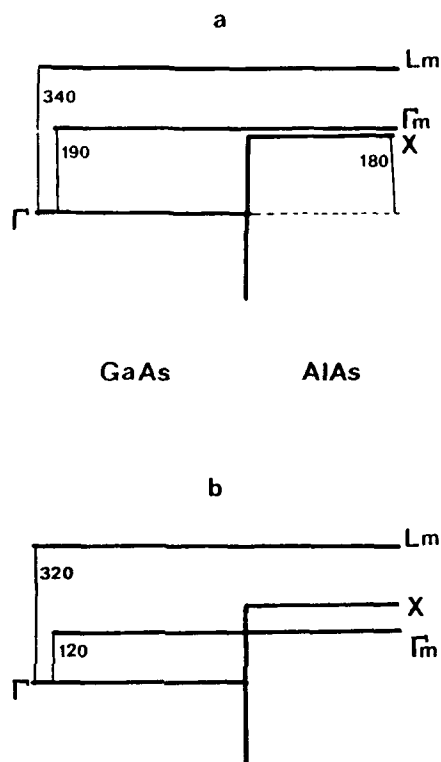


Fig. 2 - Band structure of the 35 - 17 (a) and 45 - 12 (b) Å GaAs-AlAs superlattices.

III. RESULTS

The DLTS performed in the range 4 - 350 K does not detect any peak for the GaAs-GaAlAs ($x = 0.3$) superlattices series except in the case of the 40 - 20 and 50 - 50 Å structures [5]. The DLTS spectrum obtained with a 50 - 50 Å structure exhibits at low temperature a series of peaks which are attributed to the electronic localization induced by the electric field present in the junction [6] because the width of the miniband becomes smaller than the energy drop between two adjacent wells in a part of the space charge region. Above typically 100 K, the DLTS spectrum exhibits several large peaks (see fig. 3) whose amplitudes are considerably larger than the amplitudes of the peak in the low temperature part of the spectrum. One of these peaks, indicated in the figure, is associated with the DX center: the signature (variation of the emission rate with temperature) and

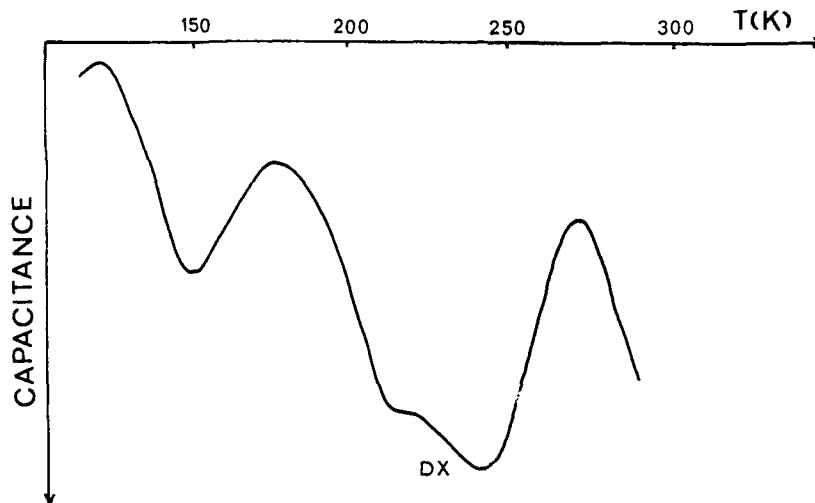


Fig. 3 - High temperature part of the DLTS spectrum obtained on the 50 - 50 Å structures.

filling characteristics are the same as for DX centers in GaAsAs layers of identical alloy composition. In the 40 - 20 Å structures a similar spectrum is observed but with a considerably lower amplitude, indicating that electron localization occurs only in a very small part of the space charge region.

The DLTS spectra of the GaAs-AlAs superlattices both contain the DX center. As shown in figure 4 the amplitude of the DX center is considerably larger in the 35 - 17 Å structures than in the 45 - 12 Å ones.

IV. DISCUSSION

Consider first the case of the GaAs-GaAlAs superlattices. In the GaAlAs ($x = 0.3$), which compose the barriers, the DX level is located at $E_T = 50$ meV below the bottom of the (Γ) conduction band. It is known [2] that, for Si doping, electron emission from this level into the band is characterized by an ionization energy E_i of ~ 0.41 eV, the difference between E_i and E_T being due to the existence of a barrier associated with the capture (~ 0.36 eV for $x = 0.3$). As a result, if the DX center is a deep defect it must remain linked to the Γ band of GaAlAs in the superlattice and thus its level must be at $\Delta - E_T = 0.23$ eV above the conduction band of the GaAs wells. This level is therefore higher in energy than the minimum δ of the first miniband (which ranges from 128 to 74 meV). As a result, electron emission from the DX level cannot be observed. It is only observed when electronic localization has been induced by the electric field which has suppressed the miniband.

In AlAs layers the DX level is also located near $E_T = 50$ meV below the bottom of the conduction band, which has now an X character. Electron emission still occurs with the same ionization energy as in GaAlAs layers:

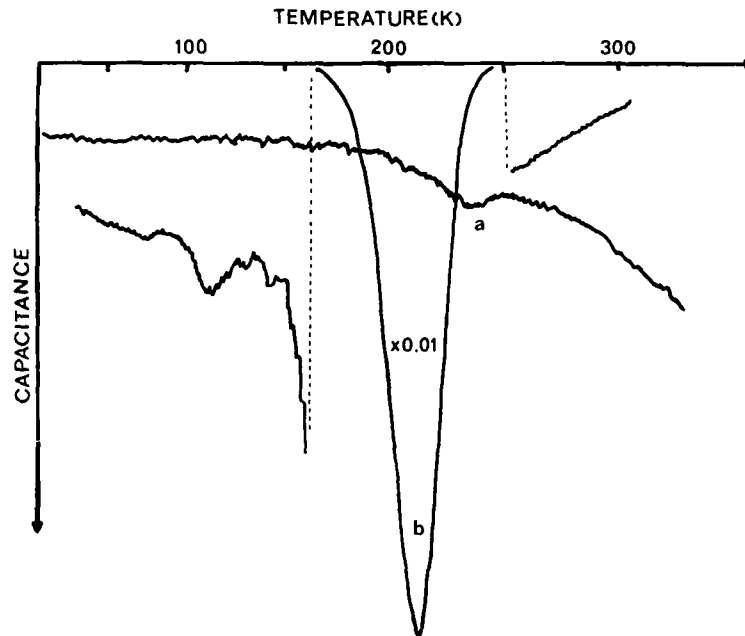


Fig. 4 - The DLTS spectrum in the 45 - 12 (a) and 35 - 17 (b) Å GaAs-AlAs superlattices.

this has been directly verified by performing DLTS measurements in Si doped AlAs layers. Thus in the GaAs-AlAs superlattices the DX level remains located below the bottom of the first conduction miniband (Γ_m) as it can be seen in figure 2 (at 20 and 60 meV respectively in the 45 - 12 and 35 - 17 Å structures). It is therefore not surprising that the DX center is then detected. The amplitude of the DX peak is weak in the 45 - 12 Å structures because E_T is located at only 20 meV from Γ_m and a large fraction of the centers cannot be filled at equilibrium.

In GaAs-AlAs superlattices the bottom of the barrier conduction band has been changed from an X to a Γ character. However, the DX ionization energy E_i remains the same as in AlAs layers. Moreover, although the DX level moves from 20 meV to 60 meV (an energy shift larger than the experimental accuracy) from one type of superlattice to the other, E_i is not changed. However, if electron emission was occurring from E_T into the bottom of the conduction band, we should expect the same shift in E_i . Because the L band of AlAs is replaced by an L miniband located for both types of superlattices practically at the same energy, within the experimental accuracy (20 meV), the fact that E_i remains constant (within 20 meV) is an evidence that electron emission occurs directly into the L band. This demonstrates that the DX level is linked to the L band a fact already suggested by several observations (for a discussion see ref. [7]).

V. CONCLUSION

The study of the variation of the concentration of DX centers with the miniband structure of n-type doped GaAs-GaAlAs and GaAs-AlAs superlattices has shown that the DX centers are present only when the L miniband is practically at the same energy position than the L band in GaAlAs or AlAs, independent of the nature and position of the first miniband. This result therefore strongly emphasizes that the energy level associated with DX center is linked to the L band and, consequently, illustrates a possible way to suppress it.

ACKNOWLEDGMENTS

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EPR STUDIES OF DX CENTER RELATED PARAMAGNETIC STATES
IN $\text{Ga}_{0.69}\text{Al}_{0.31}\text{As:Sn}$

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ABSTRACT

The electron paramagnetic resonance study of the DX center in Sn doped direct gap $\text{Ga}_{0.69}\text{Al}_{0.31}\text{As}$ shows the existence of a shallow effective mass like excited configuration of this defect. The photoexcitation spectrum for this transformation has a threshold at 0.8 eV; the photoionization of the DX center is not a transition to the lowest Γ conduction band as previously assumed. After photoexcitation additional paramagnetic defects are observed.

INTRODUCTION

Whereas doping of GaAs with the simple donors of group 4 (Si, Sn) or group 6 (S, Se, Te) leads to the formation of a shallow effective mass like donor with ionization energies of ~ 5 meV, in the case of the ternary alloy system $\text{Ga}_{1-x}\text{Al}_x\text{As}$ for $x \geq 0.20$, these dopants give rise to a deep donor defect, the so-called DX center [1,2]. The main characteristics of the DX center are a high barrier for electron capture, the value of which varies strongly with the alloy composition, an emission energy independent of x and a photoionization spectrum with an onset at $h\nu \approx 0.8$ eV, which varies only very little with x . An important aspect for the understanding of the DX center is the coexistence of both deep and shallow electronic states, which are separated from each other by a thermal barrier. They have been observed in optical absorption [3,4] and Hall effect measurements [5]. There have been several attempts to interpret the properties of the DX center and generally three basic problems are treated: a) the origin of the shallow-deep transition, b) the large or small lattice relaxation associated with the deep state, and c) the microscopic model of the DX center. The present understanding of this defect has been reviewed recently by different authors [6,7]. In summary, a Jahn Teller effect [8], a negative U character [9,10] and intervalley mixing effect [11,12] have been evoked as possible origin of the shallow-deep instability and both large [1,2], small [13] as well as mixed [4] lattice relaxation models have been proposed.

In this paper we report results of electron paramagnetic resonance studies on the Sn related DX center in $\text{Ga}_{1-x}\text{Al}_x\text{As}$ material in the direct gap alloy composition range. The EPR technique is particularly suited for the study of the microscopic structure of point defects and was applied by us to probe both the ground state and the shallow excited states of this defect. Additionally, the information on the paramagnetic or diamagnetic character of the ground state decides whether negative and positive U models are valid in this case.

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The paramagnetic character of the Si related DX center has been studied before by EPR [14,15] and in particular by optically detected magnetic resonance (ODMR) [13,16] but only in indirect gap material ($x \geq 0.35$). Both techniques have observed a donor resonance, characterized by a slightly anisotropic g-value with $\langle g \rangle \sim 1.95$. This anisotropy has been related to stress in the GaAlAs/GaAs heterostructures giving rise to a valley repopulation effect [17]. The resonance is generally ascribed to the X conduction band related shallow donor state [14]. No magnetic resonance studies on the Sn related DX center have been reported up to now.

EXPERIMENTAL

Ga_{1-x}Al_xAs layers of 32 μm thickness were grown on semi-insulating (100) oriented GaAs wafers in a vertical MOVPE reactor. The layers were Sn doped with concentration of $2 \times 10^{18} \text{ cm}^{-3}$. The alloy composition has been determined by double X-ray diffraction to $x = 0.31$. The doped Ga_{1-x}Al_xAs layer was separated from the GaAs substrate by a 0.5 μm thick undoped Ga_{0.5}Al_{0.5}As buffer layer. The photo EPR measurements were performed with a X-band spectrometer in the 4 to 300 K temperature range. The samples were optically excited by monochromatic light in the 0.5 eV ... 2.0 eV spectral range with a constant photon flux.

RESULTS

Under thermal equilibrium conditions, that is when the sample has been cooled down to 4 K in the dark, no paramagnetic signal was observed. The sample presented only a large cyclotron resonance band extending over the whole field range ($\omega_{\text{CRT}} \ll 1$). This indicates the presence of free carriers in the Γ conduction band, the lowest in direct gap material, due to the thermal barrier for electron capture on the DX center.

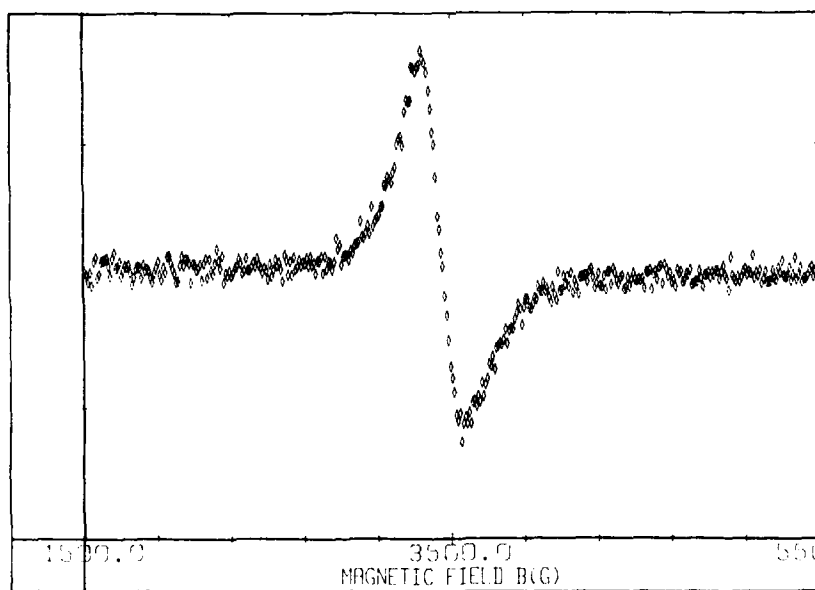


Fig. 1 : EPR spectrum under photoexcitation.

For photoexcitation with energies $h\nu \leq 0.8$ eV no effect has been observed. Under photoexcitation with $h\nu \geq 0.9$ eV both the cyclotron resonance decreases in intensity and a paramagnetic spectrum is created; thus optical excitation with $h\nu \geq 0.9$ eV leads to a transfer of free electrons to the DX center at temperatures $T < 30$ K. The EPR spectrum consists of one line, the shape, width and g-factor of which vary with the defect concentration (fig. 1).

For high concentrations the line-shape is broadened in the wings and close to Lorentzian with a peak to peak width of ~ 200 G. The Landé g-factor is isotropic and $g = 1.95 \pm 0.01$. The defect concentration is estimated to $1 \cdot 10^{18} \text{ cm}^{-3}$ assuming a spin $S = \frac{1}{2}$ system. When the photoexcitation is cut off the paramagnetic spectrum decreases slowly in intensity with an average time constant of ~ 1 hour ($T = 4$ K). The line-shape changes to Gaussian, the linewidth increases up to 600 G and the g-factor decreases down to ~ 1.84 (fig. 2). It is possible to simulate the total line-shape by a superposition of one dominant Lorentzian line and a sum of Gaussians with g values between $1.95 \leq g \leq 1.84$. The different parts of the spectrum decrease with different time constants, the low field Lorentzian decreasing fastest.

From the temperature dependence of the time constants with which the EPR intensity declines after the photoexcitation in the 4 K to 20 K temperature range an activation energy of ~ 10 meV is estimated.

We have equally determined the spectral dependence of the photoexcitation spectrum. Due to the strong and non-monotonic base-line variations under optical excitation, the initial rise method, which in its simplest form when photoionization from the valence band to the defect level as well as recapture can be neglected, gives directly the optical cross-section σ_n by :

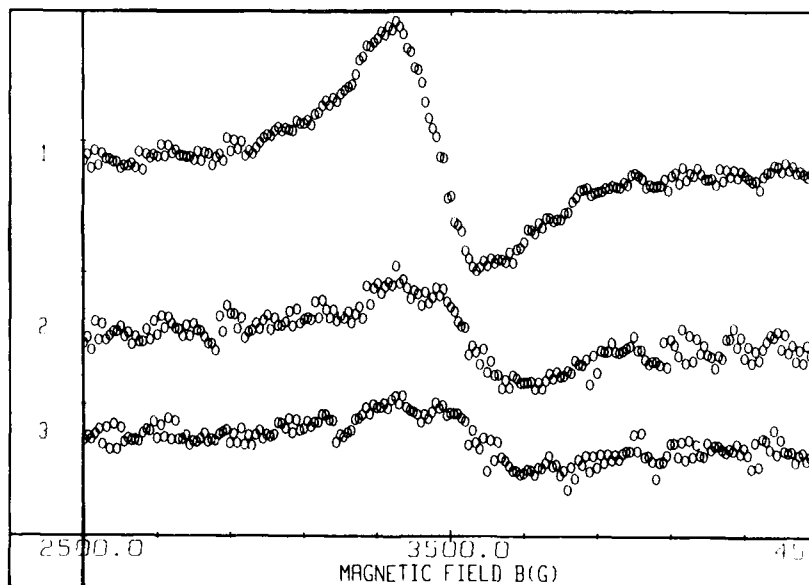


Fig. 2 : EPR spectra under (1) and after (2,3) photoexcitation.

$$\frac{dN_T}{dt} = -k \sigma_n N_T \phi$$

with N_T the concentration of the paramagnetic state and ϕ the photon flux could not be applied. We therefore determined the spectral dependence of the saturation value of the defect concentration for a constant photon flux (fig. 3). It is characterized by a threshold at 0.8 eV, a maximum at ~ 1.5 eV and a slow decrease for higher energies.

DISCUSSION

The first result is the non observation of a paramagnetic ground state under thermal equilibrium conditions. This result is in agreement with the predictions of the negative U -model of Chadi et al. [9] and Khachatryan et al [10]. Nevertheless, it cannot be excluded *a priori* that the non observation is due to an insufficient signal to noise ratio due to linewidths higher than ~ 1 kG. Indeed, the Lorentzian line-shape for the photoexcited state indicates the importance of motional narrowing effects, which reduces the linewidth of this delocalized state to ~ 200 G and thus allows its observation. Given that for lower concentrations the linewidth increases up to 600 G and that for the deep DX ground state no impurity band formation is expected for the dopant concentrations used linewidths of ≥ 1 kG can indeed not be excluded for the DX ground state.

Our results after photoexcitation show that the DX center has a metastable excited, effective mass like state. As in EPR, contrary to ODMR and optical absorption absolute defect concentration can be determined, its concentration of $\sim 1 \times 10^{18} \text{ cm}^{-3}$ demonstrates that this state is a different configuration of the DX center and not due to the presence of a different low concentration defects. The condition for the observation of

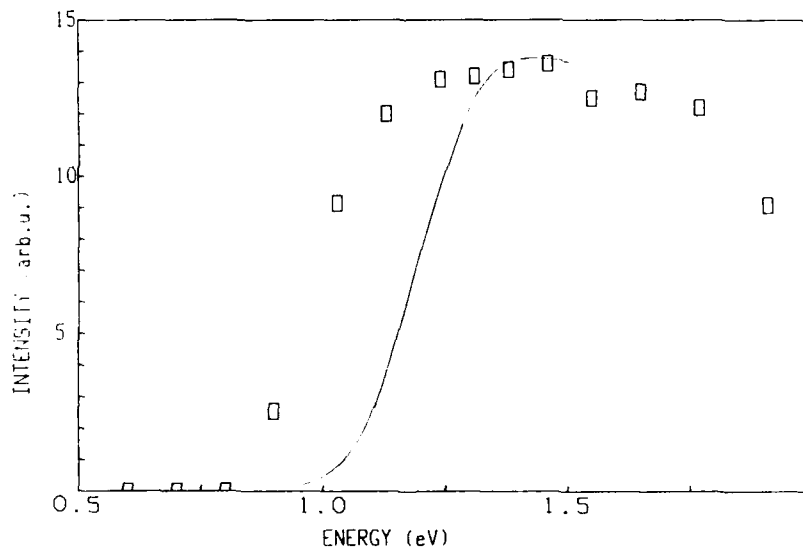


Fig. 3 : EPR photoexcitation spectrum (\circ) and photoionization spectrum (line).

the shallow donor state in direct gap material is obviously a low compensation ratio ($N_D \gg N_A$) and a small free hole concentration under optical excitation ($N_h \ll N_D$). A very similar donor resonance with g values in the 1.92 ... 1.96 range and linewidths varying between 100 and 250 G has been reported before for alloy compositions $x \geq 0.35$ [13,15,16]. In indirect gap material with a lowest X conduction band minimum this resonance is observed under thermal equilibrium conditions; from its correlation with the Si concentration [14] it has been attributed to the T_2 ground state [17] of the X-band related donor. We can thus conclude that the photoexcitation transfers the DX center from its deep ground state to the X band donor state which is separated from the first one by a thermal barrier of ~ 10 meV. This barrier height is of the same order as that deduced from Hall measurements (14 meV) [5] and the optical absorption measurements [4,6].

The deexcitation reveals the existence of additional paramagnetic states with g -factors decreasing at least down to 1.84. From analogy with the L band related donor states observed in Ge doped with group V donors [18], g -values inferior to 2 and of the order of ~ 1.6 would be expected for an effective mass like donor coupled to the L conduction band in non strained GaAlAs sample. In the presence of strain, they will be modified and g -factors varying between ~ 1.9 and ~ 0.9 can be expected; this is not incompatible with our observations.

Finally, we compare the photoexcitation spectrum, which we have determined by photo EPR, with the photoionization spectrum measured by photocapacitance techniques. Unfortunately, the spectrum for the same donor type, Sn, the same alloy composition $x = 0.31$ and temperature $T = 4$ K is not available. In figure we have compared our results with those obtained for Sn, $x = 0.4$, $T = 80$ K by Lang et al. [19]. Intracenter transitions should in principle not be observable by photocapacitance spectroscopy. However, if the excited state is close to a conduction band, such that kT is comparable to the thermal ionization, they can be observed. The two spectra have a very similar line-shape (Lucovsky type) but the photoionization spectrum is shifted by 0.2 eV to higher energies. The origin of this shift may be attributed to the different methods used (initial rise/saturation method) as well as a slight alloy shift. It follows thus that the photoionization threshold at 0.8 eV is not the threshold for a direct photoionization of the DX center to the lowest Γ conduction band as has been previously assumed in the large lattice relaxation models; it is a transition which transfers the DX center from the deep into a metastable shallow configuration. However, if this excitation is performed at temperature $T \geq 30$ K thermal ionization of the shallow state leads to an efficient transfer of electrons into the lowest Γ conduction band and persistent photoconductivity is observed.

In conclusion, we have observed that the DX center in $\text{Ga}_{0.69}\text{Al}_{0.31}\text{As}$ has an excited metastable state, which can be filled by the photoexcitation spectrum previously assigned to the photoionization to the lowest conduction band. During the thermal deexcitation of the excited state additional paramagnetic spectra with g -values lower than $g \approx 1.94$ and linewidths $\Delta B \geq 600$ G are observed.

ACKNOWLEDGMENTS

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EXPERIMENTAL CONFIRMATION OF THE DONOR-LIKE NATURE OF DX IN AlGaAs

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ABSTRACT

Transient decay of persistent photoconductivity (TDPPC) is employed to assess the donor- or acceptor-like nature of the DX defect in AlGaAs. The TDPPC data is analyzed in terms of the non-equilibrium capture kinetics of DX and a variation in the mobility due to ionized impurity scattering as calculated by the Brooks-Herring equation. TDPPC measurements show DX to be donor-like.

INTRODUCTION

There is presently a controversy in the literature regarding the nature of the DX center in AlGaAs, i.e., whether it is donor-like or acceptor-like [1-6]. This controversy is due to conflicting photo-Hall measurements reported by various researchers; some workers report a decrease [1] in the Hall mobility concomitant with persistent photoconductivity (PPC) while others report an increase [3-6]. Since the mobility is dominated by ionized impurity scattering at the measurement temperatures, acceptor-like or donor-like traps are invoked to explain the respective decrease or increase in mobility concomitant with PPC.

We have employed an alternative technique, transient decay of persistent photoconductivity (TDPPC), rather than photo-Hall measurements to determine the donor-like or acceptor-like nature of DX. Essentially, the TDPPC measurement consists of monitoring the small-signal conductance transient after termination of illumination which induces PPC. The measured conductance transient is analyzed in terms of the non-equilibrium capture kinetics of DX and a variation in the mobility due to ionized impurity scattering as calculated by the Brooks-Herring equation. TDPPC measurements show DX to be donor-like. A more detailed account of the experimental technique, the TDPPC theory, and a critique of photo-Hall measurements may be found elsewhere [7].

EXPERIMENTAL TECHNIQUE

The $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ samples used in this work were grown by molecular beam epitaxy (MBE) on an undoped, semi-insulating GaAs substrate. All of the results reported in this paper refer to a $2\text{ }\mu\text{m}$ thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ n-type active layer doped with silicon ($N_{\text{Si}} = 1 \times 10^{18} \text{ cm}^{-3}$). Care was taken to avoid the formation of a two-dimensional electron gas (2DEG) through the use of a compositionally graded buffer layer. Ohmic contacts were fabricated by evaporating AuGeNi dots through a shadow mask in a vacuum evaporator and annealing at $400\text{ }^{\circ}\text{C}$ in forming gas.

Measurements of the TDPPC were performed using an automated system based on Hewlett-Packard equipment. The temperature was controlled using a closed cycle helium cryostat. The light source consisted of a tungsten lamp, Jarrell-Ash monochromator, and appropriate filters and lenses.

The TDPPC measurement is performed as follows. The sample is initially cooled in the dark to the desired measurement temperature of $80\text{--}100\text{ K}$. The sample is then illuminated with sub-bandgap, monochromatic light until the photoconductance reaches steady state. The light source is turned off at $t = 0$ and the conductance transient is monitored via a capacitance meter. The experimental results were then fit to theoretical curves based on either a

donor-like or acceptor-like center. The quality of the fit was found to establish whether DX was donor- or acceptor-like.

An example of a TDPPC curve is shown in Fig. 1. The same curve is indicated in Fig. 2 when the normalized inverse conductance is plotted as the dependent variable. A plot of the normalized inverse conductance versus time proved to be a better means of comparing the experimental results with the theoretical fit.

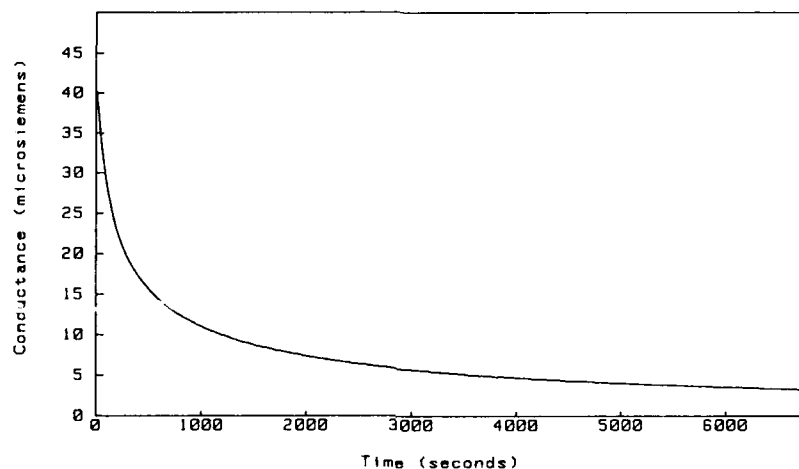


Figure 1. TDPPC curve at 85 K.

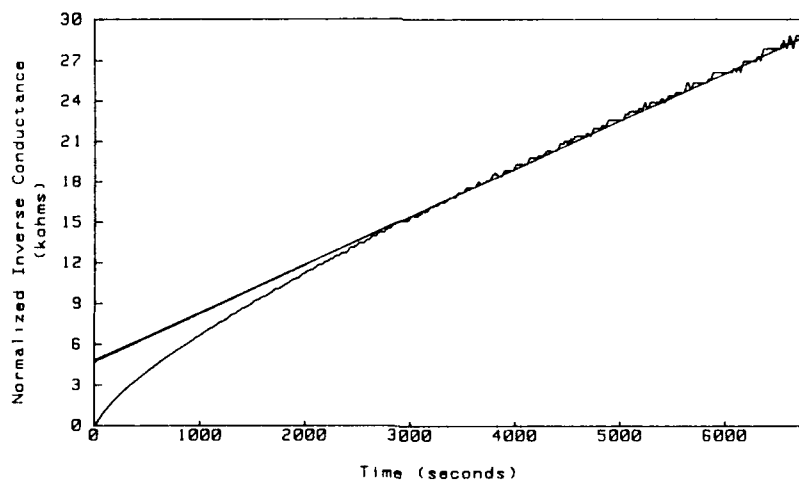


Figure 2. Inverse TDPPC curve at 85K. The straight line fit illustrates the linearity of the curve at long times.

TDPPC THEORY

TDPPC in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ with $x > 0.2$ can be explained in terms of the non-equilibrium capture kinetics of electrons from the conduction band into the DX center and the concomitant change in the mobility due to ionized impurity scattering. The general shape of the TDPPC curve is predicted to be significantly different, depending on whether DX is donor- or acceptor-like.

A brief description of the TDPPC theory is given as follows for the case of a donor-like DX center. See reference 7 for a more complete account of the TDPPC theory. In silicon-doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ with $x > 0.2$, the concentration of electrons in the conduction band, n , is controlled by the ionization state of the deep level, DX. If DX is assumed to be donor-like, charge balance ensures that

$$n = \left[N_{\text{DX}}^+(\text{eq}) - N_{\text{SA}}^- \right] + \Delta N_{\text{DX}}^+ \quad (1)$$

where N_{SA}^- is the net concentration of shallow acceptors while $N_{\text{DX}}^+(\text{eq})$ and ΔN_{DX}^+ are the respective equilibrium and nonequilibrium concentrations of ionized DX [7]. The differential equation for the decay of photoionized electrons when the illumination is turned off is given by

$$\frac{dn}{dt} = -c_n N_{\text{DX}}^+ + \left(e_n^t + e_n^o \right) N_{\text{DX}}^o \quad (2)$$

where

$$N_{\text{DX}} = N_{\text{DX}}^o + N_{\text{DX}}^+ \quad (3)$$

and where N_{DX} , N_{DX}^o , and N_{DX}^+ are the total, neutral, and ionized concentrations of DX, respectively. Also, c_n , e_n^o , and e_n^t are the electron capture rate, electron optical emission rate, and electron thermal emission rate, respectively. Since the TDPPC transient occurs at low temperature and in the dark, $c_n \gg e_n^t, e_n^o$. The electron capture rate is given by

$$c_n = v_{\text{th}} \sigma_n n \quad (4)$$

where v_{th} is the thermal velocity and σ_n is the electron capture cross-section which in the case of DX is thermally activated

$$\sigma_n = \sigma_\infty \exp(-E_{\text{cap}}/k_B T) \quad (5)$$

σ_∞ is the high-temperature capture cross-section, E_{cap} is the capture barrier, and k_B is Boltzmann's constant. Thus, Eq. (2) becomes

$$\frac{dn}{dt} = -c_n \left[n - N_{\text{DX}}^+(\text{eq}) + N_{\text{SA}}^- \right] \quad (6)$$

At the temperatures used in this study (80-100 K) and with the high concentration of impurities incorporated into the sample ($N_{\text{Si}} = 1 \times 10^{18} \text{ cm}^{-3}$), the mobility is dominated by ionized impurity scattering. Since the capture of electrons into the DX center represents a change in the charge state of the dominant level (i.e., $N_{\text{DX}} \gg N_{\text{SA}}$), the mobility can change dramatically during the TDPPC; this change is expected to be different depending on whether

DX is donor- or acceptor-like. The Brooks-Herring equation for the mobility due to ionized impurity scattering is given by [8]

$$\mu_{ii} = \frac{128\sqrt{2}\pi \epsilon^2 (k_B T)^{3/2}}{q^3 m_e^{1/2} N_{ii} \ln(b/n)} \quad (7)$$

where

$$b = \frac{96 \pi^2 m_e \epsilon (K_B T)^2}{q^2 h^2} \quad (8)$$

m_e is the electron conductivity effect mass and ϵ is the dielectric constant. N_{ii} is the total concentration of ionized impurities which is given by

$$N_{ii}(\text{donor-like}) = \Delta N_{DX}^+ + N_{DX}^+(\text{eq}) + N_{SA}^- \quad (9)$$

Equation (9) can be rewritten in terms of the free electron concentration through the use of Eq. (1) to yield

$$N_{ii} = n + 2 N_{SA}^- \quad (10)$$

The theoretical TDPPC equation is given by

$$G(t) = q n(t) \mu_{ii}(t) \quad (11)$$

Equations (6), (7), (10), and (11) comprise the set of equations necessary for determination of a theoretical TDPPC curve for a donor-like DX center. Equation (6) is solved numerically; the theoretical TDPPC curve is then generated using Eqs. (6)-(11) and compared to the experimental data.

RESULTS AND DISCUSSION

A TDPPC simulation based on a donor-like center is compared to experimental data at 85 K as shown in Fig. 3. Note that the fit is quite good. The following model values were employed in the simulation: $N_{SA}^- = 2.4 \times 10^{16}/\text{cm}^3$, $N_{DX}^+(\text{eq}) = 2.9 \times 10^{16}/\text{cm}^3$, $n(0) = 5.0 \times 10^{17}/\text{cm}^3$, $\sigma_\infty = 5 \times 10^{-15} \text{ cm}^2$, and $E_{\text{cap}} = 0.24 \text{ eV}$. Of these parameters, E_{cap} was determined experimentally, σ_∞ was obtained from the literature, and N_{SA}^- and $N_{DX}^+(\text{eq})$ were chosen to be temperature-independent constants [7]. The temperature independence of $N_{DX}^+(\text{eq})$ is justified by experimental data (e.g., Fig. 3 of reference [5]) which indicates that the apparent (Hall) electron concentration is approximately constant over the range of temperature relevant to the TDPPC measurement. Thus, $n(0)$ is the only parameter adjusted as temperature is changed.

For a simulation based on an acceptor-like DX center, it was not possible to obtain a reasonable fit with any choice of parameters, reasonable or unreasonable. An example of attempts to fit the 85 K curve is shown in Fig. 4. Note that the nature of the curvature of the experimental data could never be accounted for when DX was assumed acceptor-like.

The TDPPC simulations clearly demonstrate that DX is donor-like.

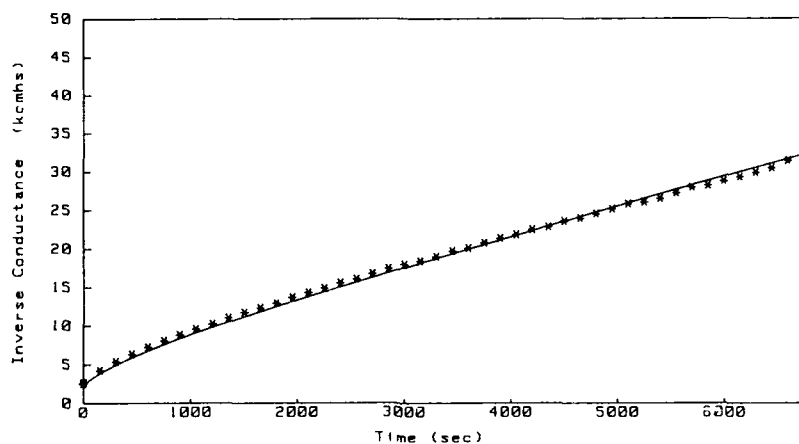


Figure 3. Donor-like simulation of the TDPPC curve at 85 K.

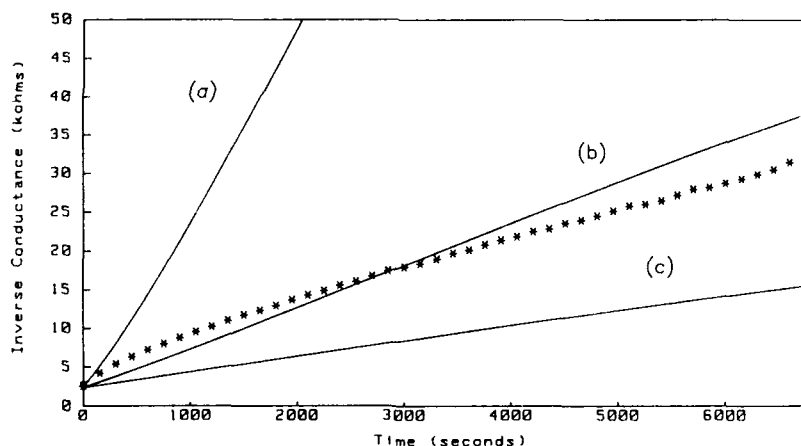


Figure 4. Acceptor-like simulations of the TDPPC curve at 85 K.

CONCLUSIONS

Transient decay of persistent photoconductivity (TDPPC) measurements are analyzed in terms of a model in which the free carrier concentration decays by thermally activated capture of electrons into DX and a change in the mobility associated with a modification of the ionized impurity density concomitant with electron capture. The experimental data could only be explained, in terms of this model, when DX was assumed to be donor-like. If

INTERACTION OF OXYGEN WITH NATIVE CHEMICAL DEFECTS IN CuInSe_2 THIN FILMS

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ABSTRACT

We formulate a consistent defect chemical model of the effect of air/ O_2 anneals on CuInSe_2 polycrystalline thin films. The model centers on O^{2-} induced neutralization of (near) surface donor states in CuInSe_2 grains. The simplest identification of these states is with ionized Se vacancies, due to coordinatively unsaturated In on grain surfaces and boundaries.

INTRODUCTION

Thin-film solar cells of CdS/CuInSe_2 have achieved efficiencies approaching 12% (1). To reach this efficiency, the as-fabricated device must be annealed in air (or oxygen) at 200°C for about 30 minutes. It has also been discovered that treating the device in an aqueous solution of hydrazine, which is a known oxygen scavenger, significantly reduces its performance parameters (i.e., open-circuit voltage, short-circuit current and fill factor). Re-annealing the device in air, however, restores the performance parameters to their original values (2). This process is reversible and clearly suggests a direct interaction between the CuInSe_2 film and oxygen (2).

Good cell performance is also correlated with the stoichiometry of the CuInSe_2 material. Optimum device performance is obtained when the film composition is off-stoichiometric (3) and is approximately 23.0-24.0 at.% Cu, 26.0-27.0 at.% In, and 49.5-51.0 at.% Se. In this letter, a model is presented to describe the interaction of oxygen with the native defect(s) in the CuInSe_2 film and the influence of this interaction on the electrical properties of the film.

RESULTS AND DISCUSSION

There are two kinds of non-stoichiometry in ionic ternary compounds such as CuInSe_2 . The first kind is deviation from molecularity, which involves no departure from normal valency, and the second is valence non-stoichiometry, which involves an excess or a deficiency of electrons compared with the number needed to fill the octet around the (formerly divalent) anion (Se^{2-}). A comprehensive description of the defect chemistry in ternary compounds can be found in Pamplin et al. and Cahen (4,5). A number of defect pairs can be expected, for the films of the above-given composition.

V_{Cu} , h^+ (Cu vacancy): acceptor, p-type material
 In_{Cu} , e^- (In-on-Cu antisite): donor, n-type material
 V_{Se} , e^- (Se vacancy): donor, n-type material
 In_i , e^- (In interstitial): donor, n-type material
 V_{Cu} , In_{Cu} : compensation.
 V_{Cu} , V_{Se} : (acceptor-donor pair)

In_i is unlikely to occur here, however, because of the relatively large heat of formation required for this defect (6), and also because of the larger radius of the tetrahedrally coordinated In(III) compared with that of Cu(I) (7). Because the material, as produced, is p-type, V_{Cu} partially

compensated by In_{Cu} , is the most likely dominant defect. However, it is evident from the list of defects that the material can be highly compensated, and the net conductivity is dictated by N_a/N_d , where N_a and N_d are the net acceptor and donor concentrations, respectively. $N_a/N_d = 1$ implies fully compensated material, and any change in either the donor or acceptor concentrations will result in a change in this compensation ratio.

Table I shows the variation in the resistivity and conductivity type of CuInSe_2 films of a given composition when they are subjected to the hydrazine/air anneal treatment cycle. In addition, the effective majority-carrier concentration of these films (p-type) changes from about 10^{14} to 10^{16} cm^{-3} after the air anneal. It is not likely that oxygen will act as an acceptor, even though a V_{Se} defect might exist. Thermally stimulated capacitance measurements (8) and transient capacitance studies (9,10) show that a reduction in the density of donors occurs that changes the compensation ratio N_a/N_d , but there is no actual increase in the density of acceptors.

TABLE I. Resistivity and conductivity type of thin-film CuInSe_2 as a function of reduction/oxidation treatment.

Cu/In/Se (at. %)	As-fabricated		Reduced		Oxidized	
	$\rho(\Omega\text{-cm})$	Type	$\rho(\Omega\text{-cm})$	Type	$\rho(\Omega\text{-cm})$	Type
25.2/24.9/49.9	0.1	p^+	0.2	p^+	0.1	p^+
24.0/26.5/49.5	1000	p^-	1200	p^-	680	p
21.1/29.3/49.6	$>10^4$	S^a	$\sim 10^4$	n^-	5×10^3	p^-

^a S is semi-insulating.

The effect of oxygen on the electrical properties of CuInSe_2 films was also evident in electron-beam-induced current (EBIC) measurements (11) on a CdS/CuInSe_2 heterojunction device. The electron beam acts as a local source of generation of electron-hole pairs in semiconducting materials. Scanning the electron beam normal to the device cross section allows the electrical junction to be located. In a n/p heterojunction device, the material on one side of the EBIC signal maximum will be n-type and the other p-type. Figure 1 shows a sequence of EBIC line scans recorded normal to the junction (after a cleave). An initial (i) and final (f) line scan are shown; the final line scan is usually four to six scans after the initial one. The EBIC line scans are for both an as-fabricated (a) and an air-annealed device at 200°C (b). Note that the EBIC signal maximum occurs in the CuInSe_2 , and not at the CdS/CuInSe_2 heterojunction. However, the signal maximum shifts appreciably toward the heterojunction after air annealing. This EBIC peak shift away from the heterojunction between the initial and final scans suggests that there is an interaction between the CuInSe_2 material and the probing electron beam. That the junction according to EBIC is in the CuInSe_2 implies both that it is a homojunction and that the CuInSe_2 layer close to the CdS is n-type. When the device is treated in hydrazine to remove the oxygen and then placed quickly in vacuum, a very weak signal is displayed with a maximum deep in the CuInSe_2 (c). The signals shown in (d) were recorded for a device treated in hydrazine and then immediately annealed in air. The EBIC maximum for this device is at the heterojunction and does not shift in subsequent line scans, indicating that the CuInSe_2 material is now stable toward the electron beam and is now also p-type. This series of experiments suggests that the electron beam dislodges oxygen from the

CuInSe₂, hence changing its electrical properties (11). The oxygen can be restored upon annealing in air. This is similar to the hydrazine/air anneal treatment described in Table I.

The presence of oxygen in the films was probed by a secondary ion mass spectroscopy depth profile using a Cs⁺ sputter beam. The relative oxygen level of the air-annealed films was much greater than that of the hydrazine-treated films. The chemical environment of oxygen and the chemical nature of the oxygen-defect interaction was clearly revealed by infrared absorption (IR) spectroscopy and soft x-ray photoemission. The IR measurement showed evidence of In-O bonding at medium-strength bands of 600, 570, and 420 cm⁻¹, and weak bands at 1150 and 540 cm⁻¹. These absorption modes are similar to some of the absorption modes in In₂O₃ (12). All of these absorption bands disappear in a hydrazine sample, but they reappear after a few hours of exposure to air.

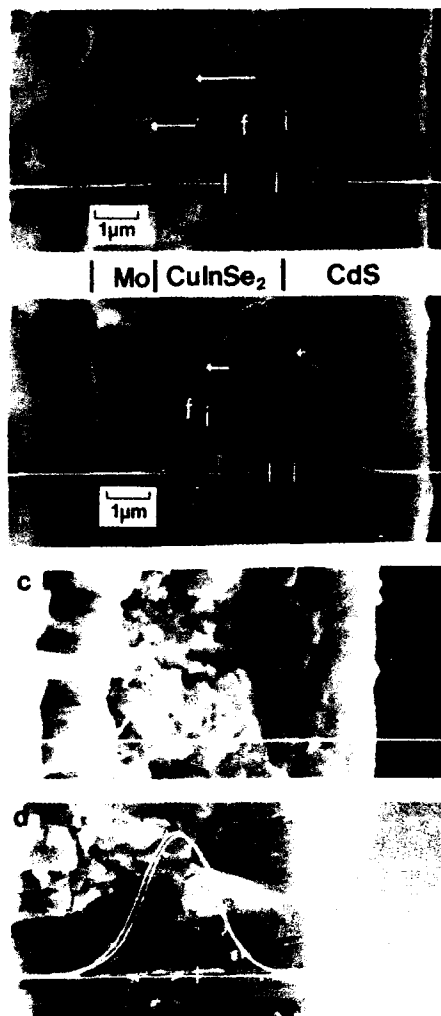
Soft X-ray photoemission experiments showed that reduction (by hydrazine) of CuInSe₂ films led to formation of reduced In, identified as In⁺ (13). These results are consistent with the shifts in In photoelectron binding (Auger-electron kinetic) energies to higher (lower) values upon air anneal of CuInSe₂ crystals (14).

All these results can be interpreted in terms of the model shown in Fig. 2. The figure illustrates defect chemical processes a and b that represent what can happen upon air oxidation at the surface of CuInSe₂ grains (a) or close to it (b). Common to all is the reduction of oxygen, involving withdrawal (localization) of conduction band electrons.

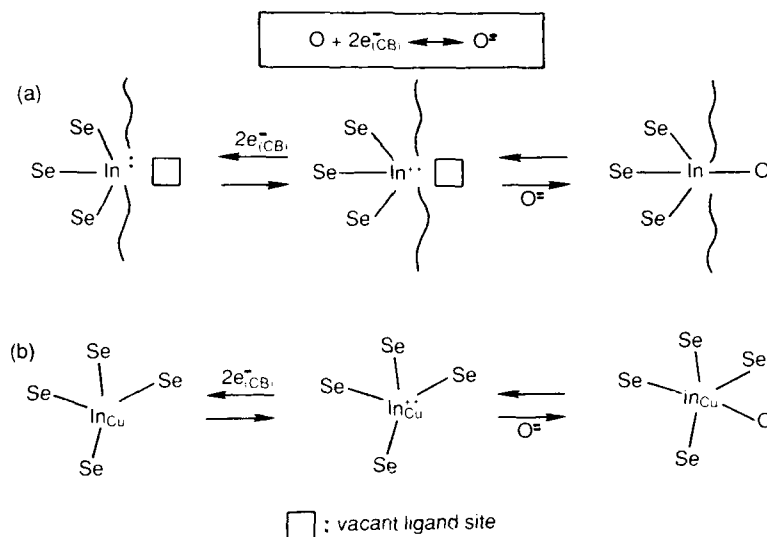
Process a: At the surface of grains whose average size is between 0.5 - 1.0 μm some (bi-or) tri-coordinated In will be present, i.e., coordinatively unsaturated In. This implies that one or more "surface" Se-vacancies, V_{Se} , exist there. In their non-ionized state charge neutrality is preserved by one (or more) lone pair(s) of electrons on the In. V_{Se} can ionize by donating one or both of the electrons to the conduction band of CuInSe₂. Oxygen, some of which may already be physisorbed on the grain surface (*vide infra*) can pick up electrons from the conduction band while reacting chemically with the In to form an In-O bond (chemisorption), thus neutralizing the V_{Se} donor. We treat V_{Se} here as a donor defect, in accordance with the Kröger-Vink model of point defects for ionic solids (5,15).

Process b: If In_{Cu} defects are involved then the interaction with O may occur even within the grain, though probably still close to the surface, because of O-diffusion limitations (*vide infra*). It is possible, as has been suggested earlier (2), that no V_{Se} are involved as illustrated in Fig. 1b. This implies the formation of penta-coordinated In. In the low temperature form of In₂Se₃ half of the In has such coordination (with Se) (16) and in AlInSe₃ only penta-coordinated In is present (17).

The assumption that air anneal of CIS affects mainly the surface of CuInSe₂ grains warrants some further scrutiny. We find that CIS cells containing denser packed CuInSe₂ films or those made using CuInSe₂ crystals are less affected or not at all, by air anneal and hydrazine reduction. Thus, the actual exposed surface area of the CuInSe₂ film is important (see Fig. 1 for porosity of films). A rough calculation shows that for a film composed of spherical 0.5 μm diameter grains, the incorporation of 0.1 at.% O in CuInSe₂ corresponds to roughly $5 \cdot 10^{19}$ oxygen atoms/cm². Thus at such a concentration only a small fraction of the surface oxygen needs to be involved in reactions of the type shown in Fig. 1 to account for the observed increase in net acceptor concentration (N_a) upon air anneal.



1. EBIC line scans for a CdS/CuInSe₂ device: (a) as fabricated, (b) after air annealing, (c) after treatment in hydrazine, and (d) treated in hydrazine followed by air annealing. The initial line scan is denoted by i and the final one by f.



2. Suggested defect chemical reactions in/on CuInSe_2 film, accompanying the air anneal in CdS/CuInSe_2 cells. (a): reaction on grains surface and on (high angle) grain boundary; (b): reaction that can occur also inside grain. (CB = conduction band).

Although we have applied the interaction model presented here, specially to CuInSe_2 , it may apply to other semiconductor chalcogenides in general, and warrants serious consideration for any electronic device using these materials.

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